Service Guide

Agilent Technologies 8562E and Agilent Technologies 8562EC Spectrum Analyzers

Agilent Technologies

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Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory.
Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

General Safety Considerations

The following safety notes are used throughout this manual. Familiarize yourself with these notes before operating this instrument.

WARNING   **Warning denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.**

CAUTION   Always use the three-prong AC power cord supplied with this product. Failure to ensure adequate grounding may cause product damage.

CAUTION	Caution denotes a hazard. It calls attention to a procedure that, if not correctly performed or adhered to, could result in damage to or destruction of the instrument. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

WARNING	**This is a Safety Class 1 Product (provided with a protective earth ground incorporated in the power cord). The mains plug shall be inserted only in a socket outlet provided with a protected earth contact. Any interruption of the protective conductor inside or outside of the product is likely to make the product dangerous. Intentional interruption is prohibited.**

WARNING	**No operator serviceable parts inside. Refer servicing to qualified personnel. To prevent electrical shock do not remove covers.**

WARNING	***Before this instrument is switched on,*** **make sure it has been properly grounded through the protective conductor of the ac power cable to a socket outlet provided with protective earth contact.**
	Any interruption of the protective (grounding) conductor, inside or outside the instrument, or disconnection of the protective earth terminal can result in personal injury.
	If this instrument is used in a manner not specified by Agilent Technologies, the protection provided by the instrument may be impaired.
	There are many points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Any adjustments or service procedures that require operation of the instrument with protective covers removed should be performed only by trained service personnel.

CAUTION	*Before this instrument is switched on,* make sure its primary power circuitry has been adapted to the voltage of the ac power source.
	Failure to set the ac power input to the correct voltage could cause damage to the instrument when the ac power cable is plugged in.
	This product conforms to Enclosure Protection IP 2 0 according to IEC-529. The enclosure protects against finger access to hazardous parts within the enclosure; the enclosure does not protect against the entrance of water.

Warranty

This Agilent Technologies instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Agilent Technologies will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies. Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instructions when properly installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error-free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. AGILENT TECHNOLOGIES SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

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1 General Information

Introduction

This *8562E and 8562EC Spectrum Analyzer Service Guide* contains information required to adjust and service the 8562E and 8562EC to the assembly level.

How to Use this Guide

Chapters 1 through 6 contain adjustments and parts information that can be used to adjust your spectrum analyzer and to help you fix problems.

Chapter 7, "General Troubleshooting," can be used to identify the location of a problem to a board or functional area in the spectrum analyzer.

Chapters 8 through 14, which cover functional areas, can then be used to help you localize the problem further.

Conventions used in this guide:

Screen Text	This font indicates text displayed on the screen
Key	This font indicates a softkey or a hardkey
8562E/EC	This term is used to refer to both 8562E and 8562EC instruments

Documentation Outline

8560 E-Series and EC-Series Spectrum Analyzers Calibration Guide

- Tells you how to run verification software.
- Tells you what your spectrum analyzer's specifications are.
- Tells you how to test your spectrum analyzer.

8560 E-Series and EC-Series Spectrum Analyzer User's Guide

- Tells you how to make measurements with your spectrum analyzer.
- Tells you how to install your spectrum analyzer.
- Tells you how to program your spectrum analyzer.

8560 E-Series and EC-Series Spectrum Analyzers Quick Reference Guide

- Is an abbreviated version of the *8560 E-Series and EC-Series Spectrum Analyzers User's Guide*.
- Provides you with a listing of all remote programming commands.

8560 E-Series Spectrum Analyzer Component Level Information

- Provides schematics and parts lists for the instrument.

Differences Between 8560 EC-Series and E-Series Spectrum Analyzers

Features	8560 EC-Series	8560 E-Series
Display	— LCD display — color — display not adjustable — backlight bulbs are replaceable (replace both bulbs when display is dim) — requires A17 LCD driver board	— CRT display — monochrome — display adjustable for intensity, focus, and quadrature — requires high voltage module (HVM), which is located in the A6 power supply — requires A17 CRT driver board
Fast ADC sweep times (FADC) enables sweep times of 30 ms to 50 μs	— FADC is standard — FADC circuitry integrated into A2 controller board	— FADC is available as an option (Option 007) — separate A16 FADC board required
VGA port	— located on rear panel — always active — does not require user interface	Not available

In all other operational respects the EC-series and E-series are identical. Unless otherwise noted, the information in this manual applies to all 8562EC and 8562E instruments.

NOTE   FADC is a standard feature, and not an option in 8560 EC-series instruments. However, it is still necessary that option "007" be in the instrument's serial ID string. For this reason, if you press the **Datecode &Options** key, the message shown on the display will indicate that option 007 is present. In addition, a statement on the rear panel of the instrument reads "Option 007 must be in serial ID string."

NOTE   Diagrams that illustrate features common to E-series and EC-series instruments are shown with E-series instruments. Where there are differences between E-series and EC-series features, separate diagrams are provided.

Instrument Variations

There are options available to the 8562E and 8562EC. The following table lists these options and identifies the assemblies which are unique to them.

Table 1-1   Instrument Variations

Option	Added	Deleted
8562E/EC Option 001 (2nd IF Output)	W19 Cable Assembly Rear-Panel J10	
8562E/EC Option 005 (Add Alternate Sweep Output)	W58 Cable Assembly	
8562E Option 007 (Fast ADC) - Fast ADC is available as an option for 8562E instruments -Fast ADC is a standard feature in 8562EC instruments and does not require additional assemblies	A16 Fast ADC Assembly A3 Interface Assembly (Opt 007) W20 Cable Assembly (Opt 007) W59 Cable Assembly	A3 Interface Assembly (Std) W20 Cable Assembly (Std)
8562E/EC Option 008 (SIG ID)	A15 RF Assembly (Opt 008)	A15 RF Assembly (Std)
8562E/EC Option 103 (Delete OCXO)	A15 RF Assembly (Opt 103)	A15 RF Assembly (Std) W49 Cable Assembly W50 Cable Assembly A21 OCXO
8562E/EC Option 104 (Delete 85620A)		85620A Mass Memory Module
8562E/EC Option 327 (Delete IF Input and Video Output)		W24 Cable Assembly W36 Cable Assembly Front-panel J3 Rear-panel J4

Serial Numbers and Repair Information

Agilent Technologies makes frequent improvements to its products to enhance performance, usability, or reliability. Agilent Technologies service personnel have access to complete records of design changes to each type of equipment, based on the equipment serial number. Whenever you contact Agilent Technologies about a product, have the complete serial number available to ensure obtaining the most complete and accurate information possible.

The serial number label is usually attached to the rear of the product. The serial number has two parts: the prefix (two letters and the first four numbers), and the suffix (the last four numbers).

Figure 1-1　　　**Serial Number Label Example**
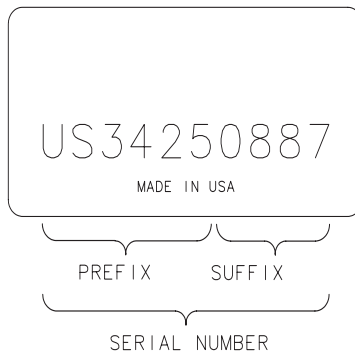
The two letters identify the country in which the unit was manufactured. The four numbers of the prefix are a code identifying the date of the last major design change incorporated in your Agilent Technologies product. The four-digit suffix is a sequential number and, coupled with the prefix, provides a unique identification for each unit produced. Whenever you list the serial number or refer to it in obtaining information about your Agilent Technologies product, be sure to use the complete number, including the full prefix and the suffix.

Units which were produced before the serial number format was changed may also be covered by this documentation. On earlier serial number labels, the prefix consists of the first four numbers and a single letter. The suffix is a five-digit sequential number.

Figure 1-2   **Earlier Serial Number Label Example**

```
3425A00564
        MADE  IN USA

    PREFIX      SUFFIX

        SERIAL NUMBER
```
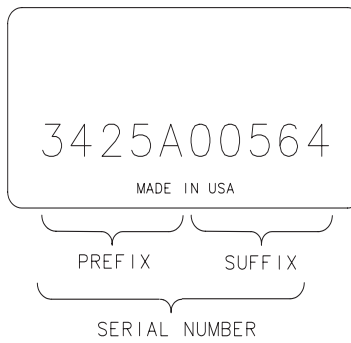
sz156e

The new serial number format (US00000000) is always considered "above" the earlier format (0000A00000) when you encounter change information such as "….serial prefix 3425A and above" or "….serial number 3425A00564 and above."

85629B Test and Adjustment Module

When attached to the rear panel of the spectrum analyzer, the 85629B test and adjustment module (TAM) provides diagnostic functions for the 8562E/EC. The TAM is accessed by a computer running interface software; this software can be downloaded from www.agilent.com/find/8560_software. The TAM measures voltages at key points in the circuitry and flags a failure whenever the voltage falls outside the limits. The TAM locates the failure to a small functional area, which can then be examined manually. See Chapter 7 , "General Troubleshooting," for a complete description of how to use the TAM and its interface software.

Service Kit

The spectrum analyzer service kit (part number 08562-60021) contains service tools required to repair the instrument. Refer to Table 1-2 on page 31 for a list of items in the service kit.

Table 1-2   **Service Kit Contents**

Description	Quantity	Part Number
Cable Puller	1	5021-6773
PC Board Prop	1	5021-7459
Line Filter Assembly	1	5061-9032
Line Switch Cable	1	5062-0728
Extender Cable	1	5062-0737
BNC to SMB (snap-on) Cable	2	85680-60093
Connector Extractor Tool Kit	1	8710-1791

Electrostatic Discharge

Electrostatic discharge (ESD) can damage or destroy electronic components. Therefore, all work performed on assemblies consisting of electronic components should be done at a static-free workstation. Figure 1-3 on page 32 is an example of a static-safe workstation using two kinds of ESD protection:

- Conductive table mat and wrist-strap combination

- Conductive floor mat and heel-strap combination

These methods may be used together or separately.

Figure 1-3   **Example of a Static-Safe Workstation**
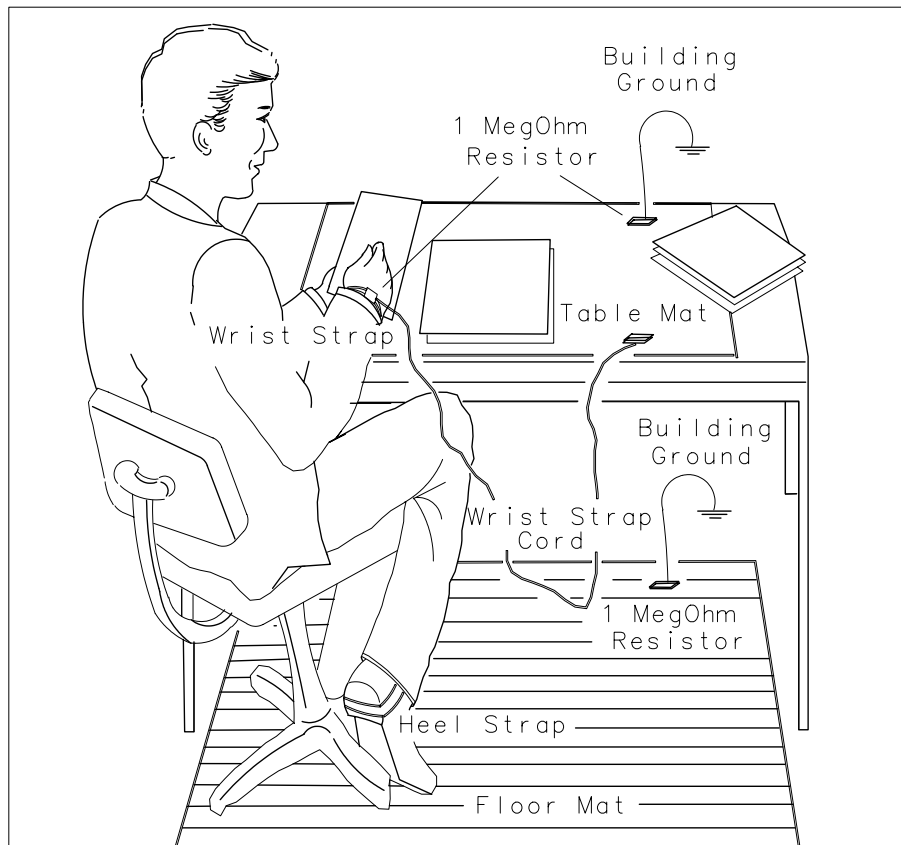
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Reducing Potential for ESD Damage

The suggestions that follow may help reduce ESD damage that occurs during instrument testing and servicing.

- Before connecting any coaxial cable to an spectrum analyzer connector for the first time each day, momentarily ground the center and outer connectors of the cable.

- Personnel should be grounded with a resistor-isolated wrist strap before touching the center pin of any connector and before removing any assembly from the unit.

- Be sure all instruments are properly earth-grounded to prevent build-up of static discharge.

Static-Safe Accessories

Table 1-3   **Static-Safe Accessories**

Part Number	Description
9300-0797	Set includes: 3M static control mat 0.6 m × 1.2 m (2 ft × 4 ft) and 4.6 cm (15 ft) ground wire. (The wrist-strap and wrist-strap cord are not included. They must be ordered separately.)
9300-0980	Wrist-strap cord, 1.5 m (5 ft).
9300-1383	Wrist-strap, color black, stainless steel, without cord, four adjustable links and 7 mm post-type connection.
9300-1169	ESD heel-strap (reusable 6 to 12 months).

Returning Instruments for Service

Service Tag

If you are returning the instrument to Agilent Technologies for servicing, fill in and attach a blue service tag. Service tags are supplied in the back of this chapter.

Please be as specific as possible about the nature of the problem. If you have recorded any error messages that appeared on the screen, or have completed a performance test record, or have any other specific data on the performance of the spectrum analyzer, please send a copy of this information with the unit.

Original Packaging

Before shipping, pack the unit in the original factory packaging materials if they are available. If the original materials are unavailable, identical packaging materials may be acquired through any Agilent Technologies Sales and Service Office. Descriptions of the packaging materials are listed in Figure 1-4 on page 36.

Other Packaging

CAUTION
Spectrum analyzer damage can result from using packaging materials other than those specified. Never use styrene pellets in any shape as packaging materials. They do not adequately cushion the equipment or prevent it from shifting in the carton. They cause equipment damage by generating static electricity and by lodging in the spectrum analyzer fan.

Repackage the spectrum analyzer in the original packaging materials or with commercially available materials described in steps 4 and 5, below.

1. Attach a completed service tag to the instrument.

2. Install the front-panel cover on the instrument.

3. Wrap the instrument in antistatic plastic to reduce the possibility of damage caused by electrostatic discharge.

4. Use the original materials or a strong shipping container that is double-walled, corrugated cardboard carton with 159 kg (350 lb) bursting strength. The carton must be both large enough and strong enough to accommodate the spectrum analyzer and allow at least 3 to 4 inches on all sides of the spectrum analyzer for packing material.

5. Surround the equipment with at least 3 to 4 inches of packing material, or enough to prevent the equipment from moving in the carton. If packing foam is unavailable, the best alternative is SD-240 Air Cap™ from Sealed Air Corporation (Commerce, CA 90001). Air Cap looks like a plastic sheet covered with 1-1/4 inch air-filled bubbles. Use the pink-colored Air Cap to reduce static electricity. Wrap the equipment several times in this material to both protect the equipment and prevent it from moving in the carton.

6. Seal the shipping container securely with strong nylon adhesive tape.

7. Mark the shipping container "FRAGILE, HANDLE WITH CARE" to assure careful handling.

8. Retain copies of all shipping papers.

Figure 1-4   **Spectrum Analyzer Shipping Container and Cushioning Materials**
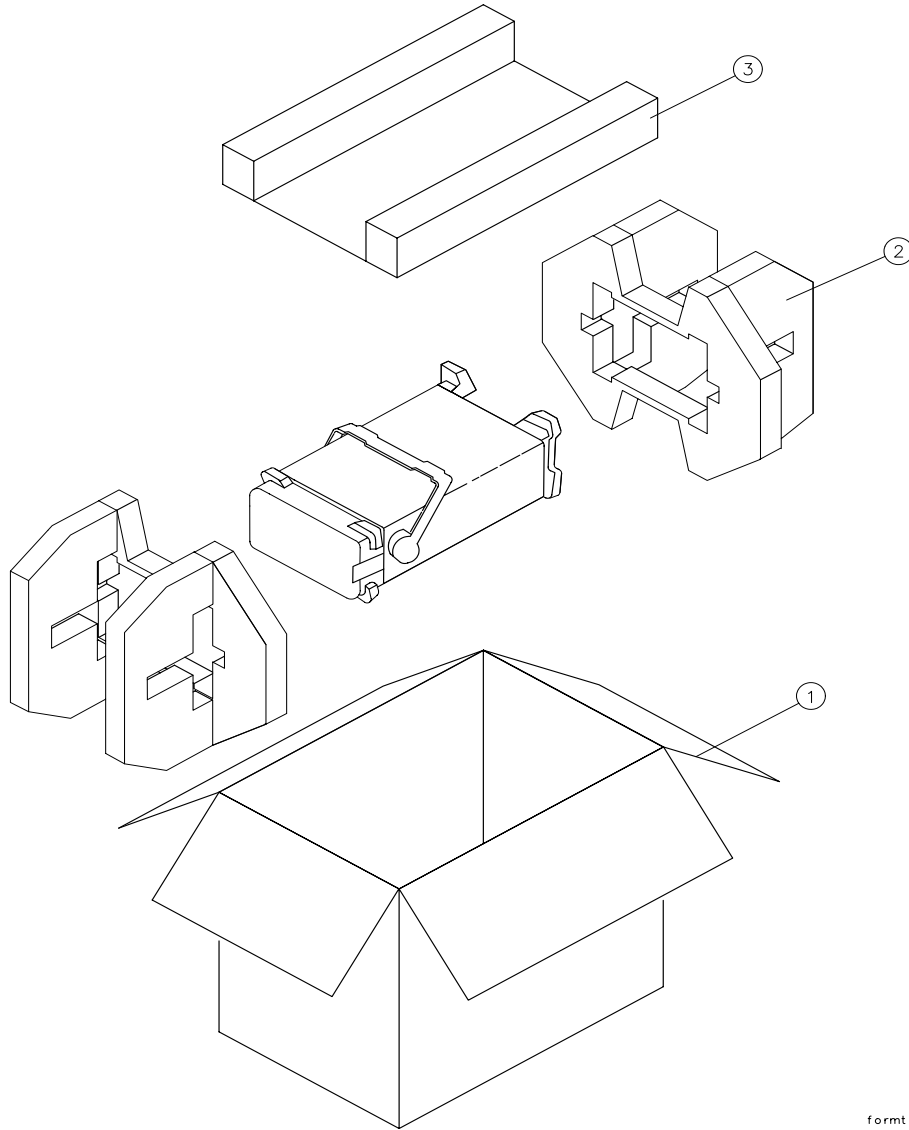
formt112

Table 1-4   **Static-Safe Accessories**

Item	Description	Part Number
1	9211-6969	Outer Carton
2	9220-5073	Pads (2)
3	9220-5072	Top Tray

Recommended Test Equipment

lists the recommended test equipment required for operation verification, performance tests, adjustments, troubleshooting, and the Test and Adjustment Module. Any equipment that meets the critical specifications given in the table can be substituted for the recommended model(s). Operation verification, and the performance tests are located in the calibration guide.

Table 1-5 **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use
Sources			
Synthesized sweeper *(two required)*	Frequency range: 10 MHz to 13.2 GHz Frequency accuracy (CW): $\times 10^{-9}$/day Leveling modes: Internal &External Modulation modes: AM &Pulse Power level range: −80 to +16 dBm	8340A/B* 83630A Option 001, 008	P,A,T, M,V
Synthesizer/ level generator	Frequency range: 200 Hz to 80 MHz Frequency accuracy: 1×10^{-7}/month Flatness: ±0.15 dB Attenuator accuracy: <±0.09 dB External 10 MHz reference input Frequency resolution: 1 Hz	3335A*, †	P,A,T, M,V
Synthesized signal generator	Frequency range: 100 kHz to 2.5 GHz Residual SSB phase noise at 1 GHz: <−73 dBc/Hz at 10 Hz offset <−107 dBc/Hz at 1 kHz offset <−124 dBc/Hz at 10 kHz offset <−124 dBc/Hz at 100 kHz offset	8663A	P,V
Pulse/ function generator	Frequency range: 10 kHz to 50 MHz Pulse width: 200 ns Output amplitude: 5 V peak-to-peak Functions: pulse &triangle Pulse rise time: <100 ns TTL sync output	8116A	P,A
AM/FM signal generator	Frequency range: 1 MHz to 200 MHz Frequency modulation mode Modulation oscillator frequency: 1 kHz FM peak deviation: 5 kHz	8640B 8642A	A

* Part of microwave workstation,

† If an 3335A is not available, see chapter 2a for performance tests using alternate equipment.

P = performance tests
A = adjustments
M = test & adjustment module
T = troubleshooting
V = operation verification

Table 1-5 **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use
Counters			
Frequency standard	Output frequency: 10 MHz Accuracy: $<1 \times 10^{-10}$	5061B	P,A
Microwave frequency counter	Frequency range: 9 MHz to 7 GHz External frequency reference input Timebase accuracy (aging): $<5 \times 10^{-10}$/day	5343A *OR* 5350B* (Option 001)	P,A,T, M,V
Universal counter	Modes: TI A→B, frequency count	5334A/B	P
	Time interval measurement range: 100 ns to 120 s		
	Frequency count range: 400 Hz to 11 MHz		
	Frequency resolution: 1 mHz		
	Timebase accuracy (aging): $<3 \times 10^{-7}$/month		
	External 10 MHz reference input		
Receivers			
Spectrum analyzer	Frequency range: 300 kHz to 7 GHz	8566B*	A,T
	Amplitude range: −70 dBm to +20 dBm		
Measuring receiver	Compatible w/power sensors	8902A*	P,A,T,
	dB relative mode		M,V
	Resolution: 0.01 dB		
	Reference accuracy: $<\pm 1.2\%$		
Sensors			
Power sensor	Frequency range: 10 MHz to 13.2 GHz	8481A*	P,A,T,
	Maximum SWR:		M,V
	1.40 (10 to 30 MHz)		
	1.18 (30 to 50 MHz)		
	1.10 (50 MHz to 2 GHz)		
	1.18 (2 to 13.2 GHz)		
Power sensor	Frequency range: 250 MHz to 350 MHz	8481D	P,A
	Power range: 100 nW to 10 μW		
	Maximum SWR: 1.15 (250 to 350 MHz)		

* Part of microwave workstation

P = performance tests
A = adjustments
M = test & adjustment module
T = troubleshooting
V= operation verification

Table 1-5   **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use

Power sensor	Frequency range: 100 kHz to 2.9 GHz
	
	Maximum SWR:
	
	  1.1 (1 MHz to 2.0 GHz)
	
	  1.30 (2.0 GHz to 2.9 GHz)
		8482A*	P,A,T,
			
			M,V

Other Equipment			
Controller	Required to run operation verification software. No substitute.	9816A, 9836A/C, 310, 320 332, 360	V
Oscilloscope	Bandwidth (3 dB): dc to 100 MHz Two channels Minimum vertical deflection factor: ≤5 mV/div Minimum timebase setting: <100 ns Digitizing display with time cursors Delta-t cursor accuracy in 500 ns/Div: <0.1 μs	54501A*	P,A,T
Amplifier	Frequency range: 2.0 to 8.0 GHz Minimum output power (leveled) 2.0 to 8.0 GHz: +16 dBm Output SWR (leveled): <1.7	11975A	P
Power supply	Output voltage: ≥24 Vdc Output voltage accuracy: <±0.2 V	6114A	A
Signature multimeter	Clock frequency >10 MHz Time interval function	5005A/B	T
Digital voltmeter	Range: −15 Vdc to +120 Vdc Accuracy: <±1 mV on 10 V range Input impedance: ≥1 M Ω	3456A*	A,T
Probes			
DVM test leads	≥36 inches, alligator clips, probe tips	34118A	A,T
High frequency probe	No substitute	85024A	T
* Part of microwave workstation P = performance tests A = adjustments M = test & adjustment module T = troubleshooting V= operation verification			

Table 1-5   **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use
Accessories			
Directional bridge	Frequency range: 1 to 80 MHz Coupling: 6 dB (nominal) Maximum coupling deviation: <1 dB (nominal) Directivity: 40 dB minimum Impedance: 50 Ω (nominal)	8721A	P
Directional coupler *(two required)*	Frequency range: 2.0 to 8.1 GHz Coupling: 16.0 dB (nominal) Maximum coupling deviation: ±1 dB (nominal) Directivity: 14 dB minimum Flatness: 0.75 dB maximum VSWR: <1.45 Insertion loss: <1.3 dB	0955-0098	P
10 dB step attenuator	Attenuation range: 30 dB Frequency range: dc to 80 MHz Connectors: BNC(f)	355D	P,V
1 dB step attenuator	Attenuation range: 12 dB Frequency range: dc to 80 MHz Connectors: BNC(f)	355C	P,V
20 dB fixed attenuator	Frequency range: dc to 13.2 GHz Attenuation accuracy: <±1 dB Maximum SWR: 1.2 (dc to 2.9 GHz)	8491B Option 020	P,V
10 dB fixed attenuator	Frequency range: dc to 13.2 GHz Attenuation accuracy: <±0.6 dB Maximum SWR: 1.2 (dc to 2.9 GHz)	8491B Option 010	P,V
Reference attenuator	Supplied with 8481D	11708A	P,A
Termination	Frequency range: dc to 13.2 GHz Impedance: 50 Ω Maximum SWR: <1.10 Connector: Type N(m)	909A	
* Part of microwave workstation P = performance tests A = adjustments M = test & adjustment module T = troubleshooting V= operation verification			

Table 1-5   **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use
Low-pass filter	Cutoff frequency: 50 MHz	0955-0306	P,M,V
	Rejection at 65 MHz: >40 dB		
	Rejection at 75 MHz: >60 dB		
Low-pass filter (two required)	Cutoff frequency: 1.8 GHz	0955-0491	P
	Rejection at >3 GHz: >45 dB		
	0.1 dB ripple		
Low-pass filter (two required)	Cutoff frequency: 4.4 GHz	11689A	P
	Rejection at 5.5 GHz: >40 dB		
Power splitter	Frequency range: dc to 13.2 GHz	11667B	
	Output tracking: <0.25 dB		
	Insertion loss: 6 dB (nominal)		
	Equivalent output SWR: <1.22		
Service accessory kit	No substitute	08562-60021	A,T
Tuning tool	No substitute	8710-1010	A
Cables			
Test cable	Connectors: BNC(m)-to-SMB(f)	85680-60093	A,M
	Length: ≥61 cm (24 in.)		
Cable, RG-214/U	Connectors: Type N(m)	11500A	P,V
	Length: ≥91 cm (36 in.)		
Cable	Connectors: SMA(m)	8120-1578	P
	Length: 24 to 36 inches		
Cable, 50 Ω coaxial (five required)	Connectors: BNC(m)	10503A	P,A,V
	Length: ≥ 122 cm (48 in.)		
Cable (two required)	Frequency range: 30 Hz to 26.5 GHz	8120-4921	P,A,M,V
	Maximum SWR: <1.4 at 26.5 GHz		
	Maximum insertion loss: 3 dB		
	Connectors: APC 3.5(m), both ends		
	Length: ≥ 61 cm (24 in.)		

* Part of microwave workstation

P = performance tests
A = adjustments
M = test & adjustment module
T = troubleshooting
V= operation verification

Table 1-5 **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model	Use
Cable, GPIB *(eight required)*	Required w/operation verification software	10833B	P,A,M
	Required w/85629B test & adjustment module		
	Length: 2 m (6.6 ft.)		
Adapters			
Adapter	Type N(f)-to-BNC(m)	1250-1477	P,A
Adapter *(three required)*	Type N(m)-to-BNC(f)	1250-1476	P,A,V
Adapter	Type N(f)-to-BNC(f)	1250-1474	P,V
Adapter	Type N(m)-to-N(m)	1250-1475	P
Adapter	Type N(f)-to-APC 3.5(m)	1250-1750	A
Adapter *(two required)*	Type N(m)-to-APC 3.5(m)	1250-1743	P,M,V
Adapter	Type N(m)-to-APC 3.5(f)	1250-1744	P,V
Adapter	Type N(m)-to-BNC(m)	1250-1473	P
Adapter	Type N(m)-to-N(f)	1250-1472	P
Adapter *(two required)*	Type N(f)-to-APC 3.5(f)	1250-1745	P,V
Adapter *(two required)*	Type N(m)-to-SMA(f)	1250-1250	P,V
Adapter	Type N(f)-to-SMA(f)	1250-1772	P
Adapter	BNC(f)-to-BNC(f)	1250-0059	A
Adapter	BNC tee(f)(m)(f)	1250-0781	P,A,M,V
Adapter	BNC(f)-to-SMA(m)	1250-1200	P,A,V
Adapter	BNC(f)-to-dual banana plug	1251-2816	A,T
Adapter *(two required)*	APC 3.5(f)-to-APC 3.5(f)	5061-5311	P,M,V
Adapter *(two required)*	APC 3.5(m)-to-APC 3.5(m)	1250-1748	P,V
Adapter	2.4 mm(f)-to-2.4 mm(f)	11900B	P,A,T,V
Adapter	APC 3.5(f)-to-2.4 mm(f)	11901B	P
Adapter	APC 3.5(m)-to-2.4 mm(f)	11901D	P
Adapter	Type N(f)-to-2.4 mm(f)	11903B	P,A,T,V
Adapter	Type N(f)-to-2.4 mm(m)	11903C	P
* Part of microwave workstation			
P = performance tests A = adjustments M = test & adjustment module T = troubleshooting V= operation verification			

Sales and Service Offices

NOTE Within the USA, a toll-free phone number is available for ordering replacement parts. Refer to "Ordering Information" on page 245 for the phone number and more information.

Agilent Technologies has sales and service offices around the world providing complete support for Agilent Technologies products. To obtain servicing information, or to order replacement parts, contact the nearest Agilent Technologies Sales and Service Office listed in Table 1-6 on page 45. In any correspondence, be sure to include the pertinent information about model numbers, serial numbers, and assembly part numbers.

Table 1-6   **Agilent Technologies Sales and Service Offices**

UNITED STATES		
Instrument Support Center Agilent Technologies (800) 403-0801		
EUROPEAN FIELD OPERATIONS		
Headquarters Agilent Technologies S.A. 150, Route du Nant-d'Avril 1217 Meyrin 2/ Geneva Switzerland (41 22) 780.8111	France Agilent Technologies France 1 Avenue Du Canada Zone D'Activite De Courtaboeuf F-91947 Les Ulis Cedex France (33 1) 69 82 60 60	Germany Agilent Technologies GmbH Agilent Technologies Strasse 61352 Bad Homburg v.d.H Germany (49 6172) 16-0
Great Britain Agilent Technologies Ltd. Eskdale Road, Winnersh Triangle Wokingham, Berkshire RG41 5DZ England (44 118) 9696622		
INTERCON FIELD OPERATIONS		
Headquarters Agilent Technologies 3495 Deer Creek Rd. Palo Alto, CA 94304-1316 USA (415) 857-5027	Australia Agilent Technologies Australia Ltd. 31-41 Joseph Street Blackburn, Victoria 3130 (61 3) 895-2895	Canada Agilent Technologies (Canada) Ltd. 17500 South Service Road Trans-Canada Highway Kirkland, Quebec H9J 2X8 Canada (514) 697-4232
Japan Agilent Technologies Japan, Ltd. Measurement Assistance Center 9-1, Takakura-Cho, Hachioji-Shi, Tokyo 192-8510, Japan TEL (81) -426-56-7832 FAX (81) -426-56-7840	Singapore Agilent Technologies Singapore (Pte.) Ltd. 150 Beach Road #29-00 Gateway West Singapore 0718 (65) 291-9088	Taiwan Agilent Technologies Taiwan 8th Floor, H-P Building 337 Fu Hsing North Road Taipei, Taiwan (886 2) 712-0404
China China Agilent Technologies 38 Bei San Huan X1 Road Shuang Yu Shu Hai Dian District Beijing, China (86 1) 256-6888		

2   Adjustment Procedures

Introduction

This chapter contains information on automated and manual adjustment procedures. Perform the automated procedures using the 85629B test and adjustment module (TAM). Never perform adjustments as routine maintenance. Adjustments should be performed after a repair or performance test failure. Refer to Table 2-1 on page 50 to for which adjustments to perform.

NOTE   Before performing any adjustments, allow the spectrum analyzer to warm up for at least 5 minutes.

Safety Considerations

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to prevent damage to the instrument. Service and adjustments should be performed only by qualified service personnel.

WARNING

Adjustments in this section are performed with power supplied to the instrument and protective covers removed. There are voltages at many points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Adjustments should be performed only by trained service personnel.

Power is still applied to this instrument with the LINE switch in the off position. Before removing or installing any assembly or printed circuit board, remove the line-power cord.

Capacitors inside the instrument may still be charged, even if the instrument has been disconnected from its source of supply.

Use a nonmetallic adjustment tool whenever possible.

Which Adjustments Should Be Performed?

Table 2-1 on page 50 lists the manual adjustments that should be performed when an assembly is repaired or changed. It is important to perform the adjustments in the order indicated to ensure that the instrument meets its specifications.

Test Equipment

The equipment required for the manual adjustment procedures is listed in Table 1-5 on page 38. Any equipment that satisfies the critical specifications given in the table may be substituted for the preferred test equipment.

If an 3335A is not available for performance tests, tests using alternate test equipment are available. See Chapter 2a, "Adjustment Procedures: 3335A Source Not Available."

Adjustable and Factory-Selected Components

Table 2-2 on page 52 lists the adjustable components by reference designation and name. For each component, the table provides a description and lists the adjustment number.

Refer to Table 2-3 on page 55 for a complete list of factory-selected components used in the instrument along with their functions. Factory-selected components are identified with an asterisk on the schematic diagrams.

Adjustment Tools

For adjustments requiring a nonmetallic tuning tool, use fiber tuning tool, part number 8710-0033.

Two different tuning tools may be necessary for IF bandpass adjustments, depending upon the type of tuning slug used in the slug-tuned inductors. If the tuning slug requires a slotted tuning tool, use part number 8710-1010. If the tuning slug requires a forked tuning tool, use part number 8710-0772.

Never try to force an adjustment control. This is especially critical when tuning variable capacitors or slug-tuned inductors. Required service accessories, with part numbers, are listed under "Service Kit" on page 31.

Instrument Service Position

Refer to Chapter 4 , "Assembly Replacement," for information on removing the spectrum analyzer cover assembly and accessing all internal assemblies.

Table 2-1   **Related Adjustments**

Assembly Changed or Repaired	Perform the following related adjustments in the order listed	Adjustment Number
A1A1 keyboard	No related adjustment	
A1A2 RPG	No related adjustment	
A2 controller	16 MHz PLL adjustment	17
	Display adjustment (8562E only)	2
	If EEROM from old A2 controller could not be used in new A2 or if EEROM must be replaced, also perform the following adjustments:	
	LO distribution amplifier adjustment	8
	External mixer amplitude adjustment	15
	YIG-tuned filter/mixer adjustment	16
	Frequency response adjustment	9
A3 interface	Display adjustment (fast zero span) - (8562E only)	2
	Frequency response adjustment	9
A4 log amp/cal osc	Display adjustment (Fast Zero Span) - (8562E only)	2
	Demodulator adjustment	13
	IF amplitude adjustment	4
	DC log amplifier adjustment	5

Table 2-1   **Related Adjustments**

Assembly Changed or Repaired	Perform the following related adjustments in the order listed	Adjustment Number
A5 IF	IF bandpass adjustment	3
	IF amplitude adjustment	4
A6 power supply	High voltage supply adjustment (8562E only)	1
	Display adjustment (8562E only)	2
A6A1 HV module	High voltage supply adjustment (8562E only)	1
	Display adjustment	2
A7 switched LO distribution amplifier	LO distribution amplifier adjustment	8
	Frequency response adjustment (or perform the frequency response performance test in the *8560 E-Series and EC-Series Spectrum Analyzer Calibration Guide*. The adjustment must be performed if the performance test fails).	9
A8 low band mixer	Frequency response adjustment	9
A9 input attenuator	Frequency response adjustment (or perform the frequency response performance test in the *8560 E-Series and EC- Series Spectrum Analyzer Calibration Guide*. The adjustment must be performed if the performance test fails).	9
A10 RYTHM	YIG-tuned filter/mixer (RYTHM) adjustment	16
	Frequency response adjustment	9
A11 YTO	YTO adjustment	7
A13 2nd converter	Frequency response adjustment	9
A14 frequency control	Display adjustment (fast zero span)	2
	YTO adjustment	7
	LO distribution amplifier adjustment	8
	Frequency response adjustment	9

Table 2-1   **Related Adjustments**

Assembly Changed or Repaired	Perform the following related adjustments in the order listed	Adjustment Number
A15 RF	10 MHz reference adjustment (TCXO, Option 103)	12
	600 MHz reference adjustment	18
	Calibrator amplitude adjustment	10
	External mixer bias adjustment	14
	Sampling oscillator adjustment	6
	External mixer amplitude adjustment	15
	Frequency response adjustment	9
A15U100 sampler	Sampling oscillator adjustment	6
A17 CRT driver	Display adjustment (8562E only)	2
A18V1 CRT	Display adjustment (8562E only)	2
A19 GPIB	No related adjustment	
A21 OCXO	10 MHz reference adjustment (OCXO)	11

Table 2-2   **Adjustable Components**

Reference Designator	Adjustment Name	Adjustment Number	Description
A2R152	16 MHz PLL ADJ	17	Adjusts the free-running frequency of the 16 MHz CPU clock.
A2R206	DGTL X GAIN	2	Adjusts the horizontal gain in the X line generator.
A2R209	SWEEP OFFSET	2	Adjusts the beginning of the trace to the left-most vertical graticule line in fast-analog zero-span mode.
A2R215	DGTL Y GAIN	2	Adjusts the vertical gain in the Y line generator.
A2R218	VIDEO OFFSET	2	Adjusts the vertical position in fast-analog zero span to match the digital zero-span input.
A2R262	STOP BLANK	2	Adjusts the blanking at the end of a vector on the display.
A2R263	START BLANK	2	Adjusts the blanking at the start of a vector on the display.

Table 2-2   Adjustable Components

Reference Designator	Adjustment Name	Adjustment Number	Description
A2R268	VIDEO GAIN	2	Adjusts the vertical gain in fast-analog zero span to match with the digital zero-span input.
A2R271	SWEEP GAIN	2	Adjusts the end of the trace to the right-most vertical-graticule line in fast-analog zero-span mode.
A4C707	FM DEMOD	13	Adjusts the FM demodulation for a peak response.
A4R445	LIMITER PHASE	5	Adjusts Limiter Phase for peak response.
A4R531	LOG AMP TOS	5	Minimizes error to Top of Screen.
A4R544	LIN FIDELITY BOW	5	Minimizes Linearity Fidelity error.
A4R826	CAL OSC AMPTD	4	Sets calibration oscillator output power (nominally –35 dBm). This power is injected into the IF during the AUTO IF ADJUST routines.
A5L300	LC CTR 1	3	Adjusts center frequency of first stage of LC bandwidth filter to 10.7 MHz.
A5L301	LC CTR 2	3	Adjusts center frequency of second stage of LC bandwidth filter to 10.7 MHz.
A5L700	LC CTR 3	3	Adjusts center frequency of third stage of LC bandwidth filter to 10.7 MHz.
A5L702	LC CTR 4	3	Adjusts center frequency of fourth stage of LC bandwidth filter to 10.7 MHz.
A5R343	15 DB ATT	4	Adjusts the attenuation of the reference 15 dB attenuator for 15 dB between minimum and maximum attenuation.
A5T200	XTAL CTR 1	3	Adjusts center frequency of first stage of crystal bandwidth filter to 10.7 MHz.
A5T202	XTAL CTR 2	3	Adjusts center frequency of second stage of crystal bandwidth filter to 10.7 MHz.
A5T500	XTAL CTR 3	3	Adjusts center frequency of third stage of crystal bandwidth filter to 10.7 MHz.
A5T502	XTAL CTR 4	3	Adjusts center frequency of fourth stage of crystal bandwidth filter to 10.7 MHz.

Table 2-2   **Adjustable Components**

Reference Designator	Adjustment Name	Adjustment Number	Description
A6R410	HV ADJ	1	Adjusts the voltage between A6TP405 and A6TP401 to the voltage marked on the A6A1 high voltage module.
A14R42	6.01 GHz	7	Adjusts the main coil tune driver current at a YTO frequency of 6.01 GHz (near the upper YTO frequency limit).
A14R76	FM SPAN	7	Adjusts the FM span accuracy by affecting the sensitivity of the FM coil driver.
A14R93	3.2 GHz	7	Adjusts the main coil fixed driver current at a YTO frequency of 3.2 GHz (near the lower YTO frequency limit).
A15C100	SMPL MATCH	6	Transforms the sampler input impedance to 50 ohms over the 285 to 297.2 MHz range.
A15C210	VCO RANGE	6	Adjusts the VCO tank capacitance so that 21V on the VCO tune line equals 298 MHz VCO frequency.
A15C750	VCXO	18	Adjusts for maximum 600 MHz reference output.
A15C751	TRIPLER	18	Adjusts for maximum 600 MHz reference output.
A15U302	10 MHz ADJ	12	Adjusts frequency of the temperature compensated crystal oscillator (TCXO) to 10 MHz.
A15R561	CAL AMPTD	10	Adjusts amplitude of the 300 MHz calibrator signal to –10.0 dBm.
A15R926	EXT BIAS ZERO	14	Adjusts zero bias point of external mixer bias.
A17R4	Z GAIN	2	Adjusts maximum intensity.
A17R11	CUTOFF	2	Adjusts intensity to turn off blanked lines.
A17R21	Z FOCUS	2	Adjusts focus for lines of different brightness.
A17R26	X FOCUS	2	Adjusts focus at the left and right corners of the display.
A17R34	COARSE FOCUS	2	Adjusts focus at the center of the display.

Table 2-2   Adjustable Components

Reference Designator	Adjustment Name	Adjustment Number	Description
A17R55	X GAIN	2	Adjusts the horizontal-deflection amplifier gain.
A17R57	X POSN	2	Adjusts the CRT horizontal position.
A17R75	Y GAIN	2	Adjusts the vertical-deflection amplifier gain.
A17R77	Y POSN	2	Adjusts the CRT vertical position.
A17R90	TRACE ALIGN	2	Adjusts the display axis rotation.
A17R92	DDD	2	Adjusts focus of the center of the display.
A17R93	ASTIG	2	Adjusts for the spot roundness on the CRT display.

Table 2-3   Factory Selected Components

Reference Designator	Adjustment Number	Basis of Selection
A5C204	3	Selected to optimize center frequency of LC tank that loads the crystal.
A5C216	3	Selected to optimize center frequency of LC tank that loads the crystal.
A5C326	3	Selected to optimize LC pole center frequency.
A5C327	3	Selected to optimize LC pole center frequency.
A5C505	3	Selected to optimize center frequency of LC tank that loads the crystal.
A5C516	3	Selected to optimize center frequency of LC tank that loads the crystal.
A5C717	3	Selected to optimize LC pole center frequency.
A5C718	3	Selected to optimize LC pole center frequency.

Using the TAM

The 85629B TAM, in conjunction with the 8562E/TAM Interface Software (TAM I/F SW), can be used to perform approximately half of the spectrum analyzer adjustment procedures on 8562E and 8562EC instruments. Table 2-4 on page 57 lists the TAM adjustments and their corresponding manual adjustments. Refer to Chapter 7 , "General Troubleshooting," for information on loading and running the TAM I/F SW.

The TAM adjustments do not include procedures for choosing factory-selected components. If an adjustment cannot be made and a factory-selected component must be changed, refer to the corresponding manual adjustment.

To select an adjustment, press **MODULE** to display the TAM main menu, then press **ADJUST**. Position the pointer next to the desired adjustment using either the knob or step keys. Press **EXECUTE**, then follow the instructions displayed on-screen.

Test Equipment

During the TAM adjustments, instructions for setting test equipment controls are displayed.

Table 2-5 on page 58 lists the test equipment needed to perform each TAM adjustment. Required models must be used. Substitutions may be made for recommended models. Substitute sources must operate over the frequency ranges indicated. Recommended substitutes are listed in the configuration menu. If you must substitute the source with a user-defined model, the adjustments run faster using a synthesized source rather than an unsynthesized source.

NOTE   When connecting signals from the 8340A/B (or any microwave source) to the adjustment setup, use a high-frequency test cable with minimum attenuation to 26.5 GHz. part number 8120-4921 is recommended for its ruggedness, repeatability, and low insertion loss.

Adjustment Indicator

To aid in making adjustments, the TAM displays an "Analog Voltmeter Display Box" along the left-hand side of the display. A horizontal line moves inside the box to represent the needle of an analog voltmeter. A digital readout appears below the box. Tick marks are often displayed on the inside edges of the box indicating the desired needle position. (The tick marks and needle are intensified when the needle is within this acceptable region.) During some adjustments, an arrow appears along the right edge of the box. This arrow always indicates the highest position the needle has reached. The arrow is useful when a component must be adjusted for a peak response; if the peak is overshot, the arrow indicates where the peak was. The component can be readjusted until the needle is at the same position as the arrow.

Table 2-4   TAM Adjustments

TAM Adjustment	Corresponding Manual Adjustment	Adjustment Number
1. IF bandpass, LC poles	IF bandpass adjustment	3
2. IF bandpass, crystal poles	IF bandpass adjustment	3
3. IF amplitude	IF amplitude adjustment	4
4. Limiter phase	DC log amplifier adjustments, A4 limiter phase	5
5. Linear fidelity	DC log amplifier adjustments, A4 linear fidelity	5
6. Log fidelity	DC log amplifier adjustments, A4 log fidelity	5
7. Sampling oscillator	Sampling oscillator adjustment	6
8. YTO	YTO adjustment	7
9. LO distribution amplifier	First LO distribution amplifier adjustment	8
10. Low band flatness[*]	Frequency response adjustment	9
11. High band flatness and YTF[*]	Frequency response adjustment	9
	YIG-tuned filter/mixer adjustment	16
12. Calibrator amplitude	Calibrator amplitude adjustment	10
13. 10 MHz reference oscillator	10 MHz reference adjustment – TCXO (Option 103)	12
14. External mixer bias	External mixer bias adjustment	14
15. External mixer amplitude	External mixer amplitude adjustment	15

[*]These TAM adjustments are not compatible with the 8562E/EC. Either perform the manual adjustment, or use the frequency response adjustment software described in Chapter 3 , "Frequency Response Adjustment Software."

Table 2-5   **Required Test Equipment for TAM**

TAM	Adjustment	Equipment Used	Required Model	Recommended Model
1.	IF bandpass, LC poles	None		
2.	IF Bandpass, crystal poles	None		
3.	IF amplitude	Synthesizer/level generator Test cable (SMB to BNC) Manual probe cable	3335A 5001-8743	 85680-60093
4.	Limiter phase	Synthesizer/level generator Test cable BNC	3335A	 10503A
5.	Linear fidelity	Synthesizer/level generator Test cable BNC	3335A	 10503A
6.	Log fidelity	Synthesizer/level generator Test cable BNC	3335A	 10503A
7.	Sampling oscillator	Manual probe cable	5001-8743	
8.	YTO	Frequency counter (3 to 6.8 GHz)		5342A, 5343A
9.	LO distribution amplifier	Manual probe cable	5001- 8743	
10.	Low band flatness	Not applicable		Not Applicable
11.	High band flatness	Not applicable		Not Applicable
12.	Calibrator amplitude	Power meter Power sensor (300 MHz)	 8482A, 8481A	8902A, 436A, 438A
13.	10 MHz reference Oscillator	Frequency counter (9 to 11 MHz)		5342A, 5343A
14.	External mixer bias	Manual probe cable	5001- 8743	
15.	External mixer amplitude	Power meter Power sensor (310.7 MHz, −25 to −35 dBm) Source (310.7 MHz, −30 dBm)		8902A, 436A, 438A 8481D, 8484A 8340A/B

Front End Cal (adjustment)

This procedure automates two manual procedures: Frequency Response Adjustment, and YIG-Tuned Filter/Mixer (RYTHM) Adjustment. This procedure is described in Chapter 3 , "Frequency Response Adjustment Software."

1. High Voltage Power Supply Adjustment (8562E)

Assembly Adjusted

A6 power supply

Related Performance Test

There is no related performance test for this adjustment.

Description

The high voltage power supply is adjusted to the voltage marked on the A6A1 HV module. The A6A1 HV module is characterized in the factory to ensure that the display filament voltage is set to 6.0 V rms when the +110 Vdc (nominal) supply is set to the voltage marked on the HV module.

WARNING   **To minimize shock hazard, use a nonmetallic adjustment tool when adjusting the A6 power supply. The following procedure probes voltages that, if contacted, could cause personal injury or death.**

NOTE   Adjustment of the high voltage power supply should not be a routine maintenance procedure. Any adjustments should be done only if the A6 power supply, A6A1 HV module, or A18V1 CRT (display) is repaired or replaced.You must perform the display adjustments after this adjustment if either the display or HV module has been replaced.

Figure 2-1   **High Voltage Power Supply Adjustment Setup**
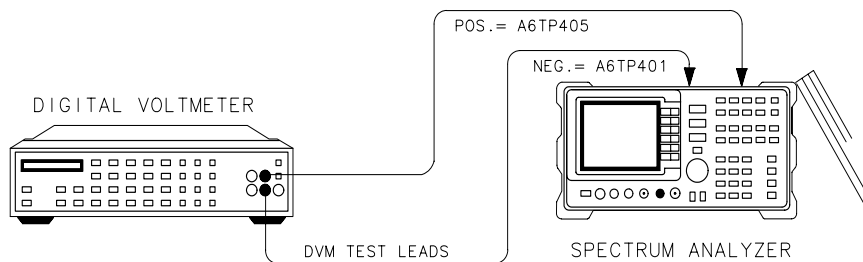
Equipment

Digital multimeter 3456A
DVM test leads 34118A

Procedure

After disconnecting the ac power cord, allow capacitors in the high voltage supply to discharge for at least 30 seconds before removing the protective cover from the A6 power supply.

1. Turn the spectrum analyzer off by pressing **LINE**. Disconnect the power cord and remove the spectrum analyzer cover. Fold down the A2 controller, A3 interface, A4 log amplifier/cal oscillator, and A5 IF assemblies. Remove the A6 power supply cover.

2. Position the spectrum analyzer as shown in Figure 2-1 on page 60. Connect the negative DVM lead to A6TP401 and the positive DVM lead to A6TP405. Place the positive DVM lead on the inductor (L401) lead which is adjacent to the label that reads "U401"; a white square outlines the area on the PC board where this lead is inserted into the A6 board.

3. Set the 3456A controls as follows:

   Function ....DC VOLTS
   Range .... 1000 VOLTS

4. Reconnect the power cord to the spectrum analyzer and press **LINE** to the on position.

5. Record the voltage marked on the A6A1 HV module.

   Voltage marked on A6A1 HV Module =_____ Vdc

6. Adjust A6R410 HV ADJ for a voltage equal to the voltage recorded in step 5.

7. Press **LINE** to turn the spectrum analyzer off and disconnect the power cord. Wait at least 30 seconds for the high voltage power supply capacitors to discharge.

8. Disconnect the DVM test leads from A6TP401 and A6TP405. Reinstall the power supply cover.

2. Display Adjustment (8562E)

Assembly Adjusted

A2 controller A17 CRT driver

Related Performance Test

Sweep Time Accuracy (Sweep Times <30 ms)

Description

Coarse adjustment of the deflection amplifiers, Z-axis amplifiers, and line generators is done using the CRT adjust pattern. Fine adjustments use the graticule. The fast zero-span amplitude adjustments correct for differences between analog and digital display modes. The displayed sweep time accuracy is adjusted in the fast zero-span sweep adjustments.

Figure 2-2   **Display Adjustment Setup**
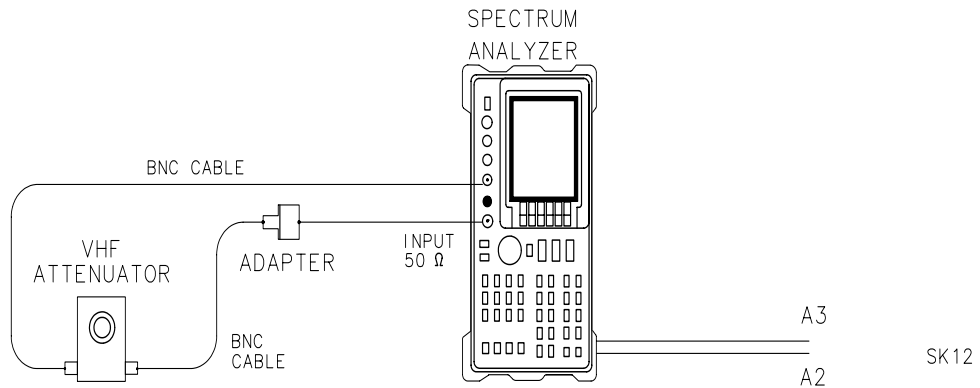
Equipment

10 dB VHF step attenuator 355D

Adapters

Type N (m) to BNC (f) 1250-1476

Cables

BNC, 122 cm **(2 required)** 10503A

Procedure

NOTE   Perform the 16 MHz PLL Adjustment in this chapter before proceeding with this adjustment.

1. Turn the spectrum analyzer off by pressing **LINE**. Remove the spectrum analyzer cover and fold out the A2 controller and A3 interface assemblies as illustrated in Figure 2-2 on page 62. Connect the CAL OUTPUT to the INPUT. Adjustment locations are shown on the CRT neck for A17 adjustments and in Figure 2-4 on page 66 for the A2 adjustments.

Preliminary Adjustments

1. Set A17R55 X GAIN, A17R75 Y GAIN, A17R92 DDD, A17R93 ASTIG, A2R206 DGTL X GAIN, A2R215 DGTL Y GAIN, A2R262 STOP BLANK, and A2R263 START BLANK to midrange. Also set the rear-panel X POSN, Y POSN, and TRACE ALIGN to midrange.

2. Set A17R21 Z FOCUS, A17R26 X FOCUS, and A17R11 CUTOFF to midrange.

3. Set A17R4 Z GAIN fully clockwise.

4. Turn the spectrum analyzer on and allow it to warm up for at least 3 minutes. Adjust A17R11 CUTOFF until the display is visible and A17R34 COARSE FOCUS for best possible focus.

Cutoff Adjustment

Press **PRESET**, **DISPLAY**, **INTENSITY**, 255 **ENTER**, **STORE INTENSITY**, **MORE 1 of 2**, **FOCUS**, 127 **ENTER**, **STORE FOCUS**, then **GRAT ON OFF** (OFF). Adjust A17R11 CUTOFF until the retrace line between the bottom of trace A and the annunciators at the bottom of the display just disappears.

Deflection Adjustments

1. Press **GRAT ON OFF** (ON), **MORE 2 of 2**, **INTENSITY**, 80 **ENTER**, **STORE INTENSITY**, **CAL**, **MORE 1 of 2**, and **CRT ADJ PATTERN**. Fold up the A3 interface assembly to access the adjustments on the A2 controller assembly.

2. Refer to Figure 2-3 on page 65 for locating the lines used for adjusting DGTL X GAIN and DGTL Y GAIN. Each of these lines is actually two lines adjusted for coincidence. The two lines will form an "X" if they are not adjusted properly.

3. Adjust A2R206 DGTL X GAIN until the two vertical lines near the left edge of the display converge to one single line.

4. Adjust A2R215 DGTL Y GAIN until the two horizontal lines near the top edge of the display converge to one single line.

5. Adjust A2R262 STOP BLANK and A2R263 START BLANK for the sharpest corners of the outer box in the test pattern. The intensity of the corners should be the same as the middle of the lines between the corners.

6. Adjust the rear-panel TRACE ALIGN until the left-most line of the test pattern is parallel with the CRT bezel. See Figure 2-3 on page 65.

7. Adjust the rear-panel X POSN and A17R55 X GAIN until the left-most "@" characters and the softkey labels appear just inside the left and right edges of the CRT bezel.

8. Adjust the rear-panel Y POSN and A17R75 Y GAIN until the softkey labels align with their appropriate softkeys.

9. Press **PRESET**. If necessary, readjust STOP BLANK and START BLANK for the best-looking intersection of the graticule lines. This will be most noticeable along the center vertical and horizontal graticule lines.

Figure 2-3   CRT Adjust Pattern

DEFLECTION ADJUSTMENTS

Adjust START BLANK
and STOP BLANK for
sharp corners

Adjust DGTL Y GAIN
until only one
line appears

Adjust
DGTL X GAIN
until only one
line appears

RECALL

SOFTKEY 1
SOFTKEY 2
SOFTKEY 3
SOFTKEY 4
SOFTKEY 5
EXIT

hp
856X

Adjust TRACE ALIGN
to place this line
parallel to left
edge of CRT bezel

Adjust MIN INTEN
until dots in these
areas just disappear

SK13

Intensity Adjustments

1. Press **AMPLITUDE** then set the **REF LVL** to −70 dB and the **LOG dB/DIV** to 1. This should almost completely fill the screen with the noise floor. Press **SGL SWP**. Adjust A17R4 Z GAIN until the intensity at the center of the screen is about medium. It should be fully illuminated, but not so bright that it burns the screen (15 NITs on a photometer/radiometer).

2. Press **CAL**, **MORE 1 of 2**, and **CRT ADJ PATTERN**. Locate the dot just below the HP logo. Adjust A17R93 ASTIG for the smallest round dot possible.

3. Adjust A17R34 COARSE FOCUS and A17R92 DDD for the best focus of the characters at the center of the screen.

4. Adjust A17R21 Z FOCUS for the best focus of the test pattern outside box.

5. Adjust A17R26 X FOCUS for best focus of the "@" characters at the corners of the test pattern.

6. Repeat steps 17 through 20 to obtain the best overall focus quality.

Figure 2-4   **A2 Display Adjustment Locations**
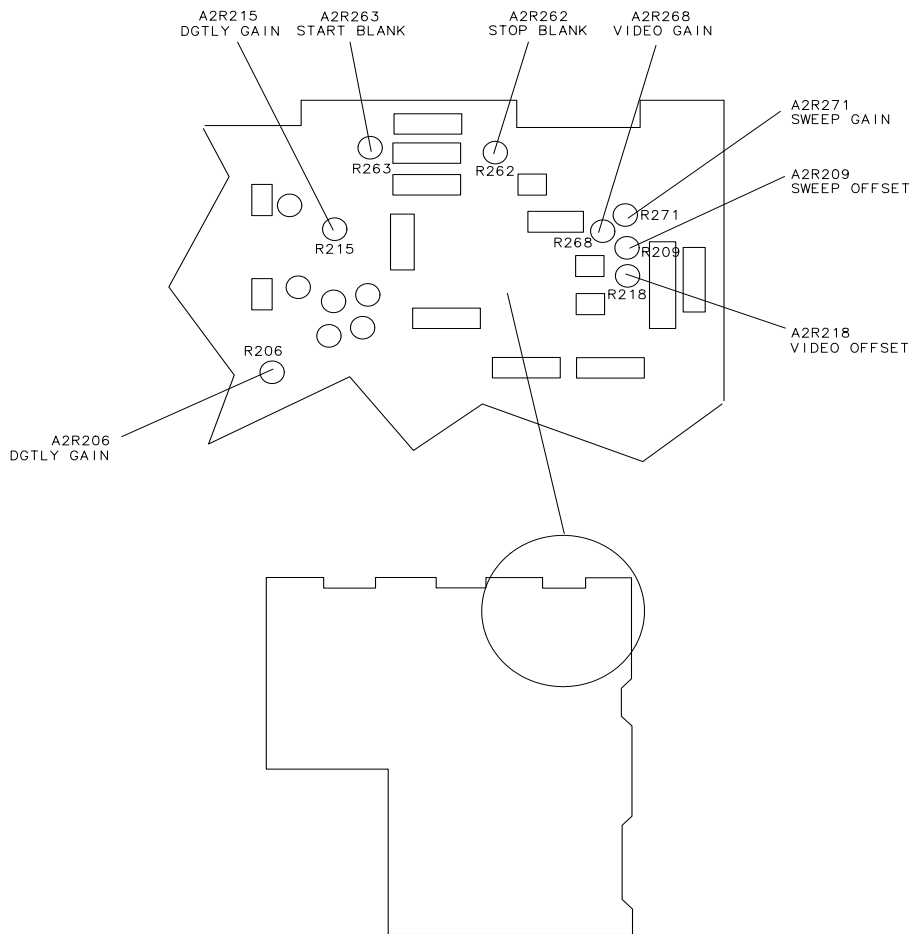
Fast Zero Span Adjustments

1. Set A2R209 SWEEP OFFSET, A2R218 VIDEO OFFSET, and A2R268 SWEEP GAIN to midrange. Adjustment locations are shown in for these A2 adjustments.

2. Set the 355D to 30 dB attenuation.

3. Press **PRESET** on the spectrum analyzer, and connect the equipment as shown in Figure 2-2 on page 62. Set the spectrum analyzer controls as follows:

> Center frequency .... 300 MHz
> Span ....0 Hz
> Reference level .... −40 dBm
> Resolution bandwidth .... 1 kHz
> Video bandwidth ....300 Hz
> Sweep time .... 50 ms

4. Press **MKR**, **MKR→**, **MARKER→ REF LVL**. If the marker is not at the top graticule, press **MARKER→ REF LVL** again.

5. Press **SAVE**, **SAVE STATE**, and **STATE 0**.

6. Set the sweep time to 10 ms.

7. Press **SAVE**, **SAVE STATE**, and **STATE 1**.

8. Adjust A2R209 SWEEP OFFSET to place the beginning of the trace at the left-most vertical graticule line.

9. Adjust A2R271 SWEEP GAIN to place the end of the trace at the tenth vertical graticule line (one division from the right edge of the graticule).

10. Press **AMPLITUDE** and press the ⇓ key seven times.

11. Press **SAVE**, **SAVE STATE**, and **STATE 2**.

12. Set the sweep time to 50 ms. Press **SAVE**, **SAVE STATE**, and **STATE 3**.

13. Press **RECALL**, **RECALL STATE**, and **STATE 1**.

14. Switch between **STATE 1** and **STATE 2**. Adjust A2R268 and A2R218 so that the trace in state 1 is lined up with the top line of the graticule and the state 2 trace is lined up with the eighth graticule down from the top (counting the top line). Repeat until the traces align to within ±0.2 divisions.

15. Adjust A2R209 and A2R271 until the start of sweep is aligned to the left-most vertical graticule line and the end of the sweep is aligned with the right most vertical graticule line.

16. Press **STATE 2** and **STATE 3**. The two traces should be aligned within ±0.1 divisions.

17. Press **STATE 0** and **STATE 1**. The two traces should be aligned within ±0.1 divisions.

3. IF Bandpass Adjustment

Assembly Adjusted

A5 IF assembly

Related Performance Test

Resolution bandwidth accuracy and selectivity

Description

The center frequency of each IF bandpass filter pole is adjusted by DAC-controlled varactor diodes and an inductor (for the LC poles) or a transformer (for the crystal poles). The inductors and transformers are for coarse tuning and the varactors are for fine tuning by the microprocessor. The inductors and transformers are adjusted such that the varactor diodes are biased near the middle of their capacitance range. The varactor diode bias is measured with the DVM.

NOTE   This procedure is not a routine adjustment. It should be performed only if repairs to the A5 IF assembly are made. If the entire A5 IF assembly is replaced, the assembly arrives pre-adjusted from the factory and requires no further adjustment.

Figure 2-5   **IF Bandpass Adjustment Setup**
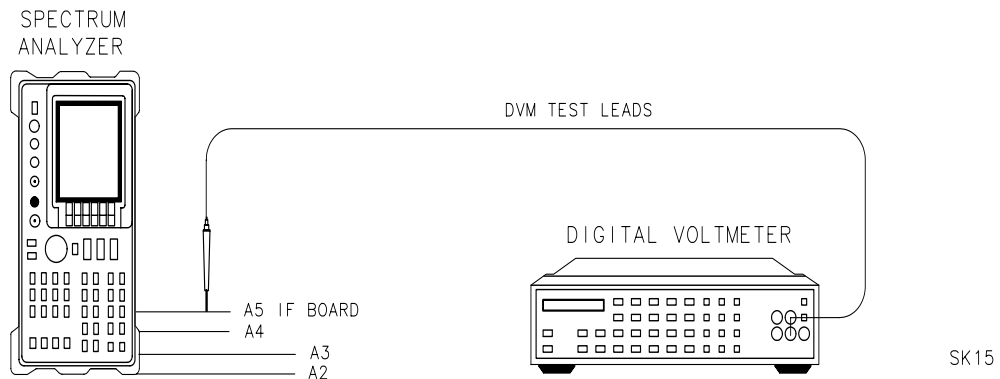
Equipment

Digital voltmeter 3456A
DVM test leads 34118A
Special tuning tool (for slot-type tuning slugs) 8710-1010
Special tuning tool (for fork-type tuning slugs) 8710-0772

Procedure

1. Turn the spectrum analyzer off by pressing **LINE**. Disconnect the power cord. Remove the spectrum analyzer cover and fold down the A2 controller, A3 interface, A4 log amp, and A5 IF assemblies. Reconnect the power cord. Turn the spectrum analyzer on and allow it to warm up for at least 30 minutes.

2. Connect the negative DVM lead to pin 6 of A5J6. See Figure 2-5 on page 68 and Figure 2-6 on page 69. Set the 3456A controls as follows:

    Function ....DC VOLTS
    Range ....10 V

3. On the spectrum analyzer press, **PRESET**, **SPAN**, **2**, **MHz**, **CAL**, and **IF ADJ ON OFF** so OFF is underlined.

Figure 2-6   **TAM Connector Pin Locations**


```
PIN 2 ● ● ● ● ● ● ● ● PIN 16
PIN 1 ■ ● ● ●   ● ● ●
```
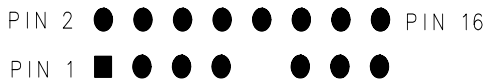
SP114E

LC Bandpass Adjustments

1. On the spectrum analyzer, press **ADJ CURR IF STATE**. Wait for the `IF ADJUST STATUS` message to disappear before continuing with the next step.

2. Read the voltage on A5TP5 (this is an empty-hole type of test point). If the voltage is less than +6.06 Vdc, turn A5L300 LC CTR 1 clockwise. If the voltage is greater than +6.26 Vdc, turn LC CTR 1 counterclockwise.

3. Repeat steps 4 and 5 until the voltage reads +6.16 Vdc ±100 mV.

NOTE   If the range for the LC CTR adjustment is insufficient, replace the appropriate factory-selected capacitor as listed in Table 2-6 on page 70. To determine the correct replacement value, center the LC CTR adjustment and press **ADJ CURR IF STATE**. After the `IF ADJUST STATUS` message disappears, read the DVM display. Choose a capacitor value from Table 2-7 on page 71, based on the DVM reading and the presently loaded capacitor value. Table 2-10 on page 73 lists a few capacitor part numbers.

CAUTION

Turn the spectrum analyzer off by pressing **LINE** to the off position before removing or replacing any shield.

4. Move the positive DVM lead to A5TP6.

5. Adjust A5L301 LC CTR 2 by repeating steps 4 through 6.

6. Move the positive DVM test lead to A5TP2 (this is a resistor-lead type of test point).

7. Adjust A5L700 LC CTR 3 by repeating steps 4 through 6.

8. Move the positive DVM test lead to A5TP1 (this is a resistor-lead type of test point).

9. Adjust A5L702 LC CTR 4 using the procedure in steps 4 through 6.

Table 2-6   **Factory-Selected LC Filter Capacitors**

LC CTR Adjustment	Fixed Factory Select Capacitor
A5L300 LC CTR 1	A5C326
A5L301 LC CTR 2	A5C327
A5L700 LC CTR 3	A5C717
A5L702 LC CTR 4	A5C718

Table 2-7 **LC Factory-Selected Capacitor Selection**

DVM Reading (V)	Currently Loaded Capacitor Value (pF)						
	Replace **6.8** with:	Replace **8.2** with:	Replace **10** with:	Replace **12** with:	Replace **15** with:	Replace **18** with:	Replace **20** with:
0 to 1.5	*	*	*	*	*	*	*
1.5 to 2.5	18	18	*	*	*	*	*
2.5 to 3.5	15	15	18	18	*	*	*
3.5 to 4.5	10	12	15	15	18	*	*
4.5 to 5.5	8.2	10	12	15	18	*	*
5.5 to 6.5	No change	No change	No change	No change	No change	No change	No change
6.5 to 7.5	No change	No change	No change	No change	No change	No change	No change
7.5 to 8.5	*	6.8	8.2	10	12	15	18
8.5 to 9.5	*	*	6.8	8.2	12	15	18
9.5 to 10	*	*	6.8	8.2	10	12	15
* Indicates a condition that should not exist; suspect broken hardware.							

XTAL Bandpass Adjustments

1. On the spectrum analyzer, press **SPAN**, 1, **MHz**, and **CAL**.

2. Move the positive DVM test lead to A5TP7.

3. On the spectrum analyzer, press **ADJ CURR IF STATE**. Wait for the IF ADJUST STATUS message to disappear before continuing to the next step.

4. Read the voltage displayed on the DVM. If the voltage is less than +6.06 Vdc, turn A5T200 XTAL CTR 1 clockwise. If the voltage is greater than +6.26 Vdc, turn XTAL CTR 1 counterclockwise.

5. Repeat steps 15 and 16 until the voltage reads +6.16 Vdc ±100 mV.

NOTE

If the range for the XTAL CTR adjustment is insufficient, replace the appropriate factory-selected capacitor as listed in Table 2-8 on page 72. To determine the correct replacement value, center the XTAL CTR adjustment, and press **ADJ CURR IF STATE**. After the IF ADJUST STATUS message disappears, read the DVM display. Choose a capacitor value from Table 2-9 on page 73, based on the DVM reading and the presently loaded capacitor value. Table 2-10 on page 73 lists a few capacitor part numbers.

CAUTION   Turn the spectrum analyzer off by pressing **LINE** to the off position
               before removing or replacing any shield.

6. Move the positive DVM test lead to A5TP8.

7. Adjust A5T202 XTAL CTR 2 using the procedure in steps 15 through 17.

8. Move the positive DVM test lead to A5TP3.

9. Adjust A5T500 XTAL CTR 3 using the procedure in steps 15 through 17.

10. Move the positive DVM test lead to A5TP4.

11. Adjust A5T502 XTAL CTR 4 using the procedure in steps 15 through 17.

Table 2-8   Factory-Selected XTAL Filter Capacitors

XTAL CTR Adjustment	Fixed Factory Select Capacitor
A5T200 XTAL CTR 1	A5C204
A5T202 XTAL CTR 2	A5C216
A5T500 XTAL CTR 3	A5C505
A5T502 XTAL CTR 4	A5C516

Table 2-9   **XTAL Factory-Selected Capacitor Selection**

DVM Reading (V)	Currently Loaded Capacitor Value (pF)					
	Replace **15** with:	Replace **18** with:	Replace **20** with:	Replace **22** with:	Replace **24** with:	Replace **27** with:
0 to 1.5	*	*	*	*	*	*
1.5 to 2.5	27	*	*	*	*	*
2.5 to 3.5	22	27	27	*	*	*
3.5 to 4.5	18	22	24	27	27	*
4.5 to 5.5	18	20	22	24	27	*
5.5 to 6.5	No change	No change	No change	No change	No change	No change
6.5 to 7.5	No change	No change	No change	No change	No change	No change
7.5 to 8.5	*	15	18	18	22	24
8.5 to 9.5	*	15	15	18	20	24
9.5 to 10	*	*	15	18	20	24
* Indicates a condition that should not exist; suspect broken hardware.						

Table 2-10   **Capacitor Part Numbers**

Capacitor Value (pF)	Part Number
6.8	0160-4793
8.2	0160-4792
10	0160-4791
12	0160-4790
15	0160-4789
18	0160-4788
20	0160-5699
22	0160-4787
24	0160-5903
27	0160-4786

4. IF Amplitude Adjustments

The IF amplitude adjustments consist of the cal oscillator amplitude adjustment and the reference 15 dB attenuator adjustment.

Assembly Adjusted

A4 log amp/cal oscillator A5 IF assembly

Related Performance Tests

IF Gain Uncertainty Scale Fidelity

Description

This adjustment sets the output amplitude of the A4 log amp/cal oscillator and the absolute amplitude of the reference 15 dB attenuator.

The output of the A4 log amp/cal oscillator is adjusted so that a −55 dBm signal applied to the 10.7 MHz IF input on the A5 IF assembly (A5J3) causes a displayed signal of −60 dBm. The effect of this adjustment is visible only after the **ADJ CURR IF STATE** sequence is complete. **ADJ CURR IF STATE** causes the IF gain adjustment to use the "new" output amplitude from the A4 log amp/cal oscillator.

This procedure also sets the attenuator of the reference 15 dB attenuator so that a source amplitude change of 50 dB combined with a spectrum analyzer reference level change of 50 dB displays an amplitude difference of 50 dB.

Figure 2-7   **IF Amplitude Adjustment Setup**
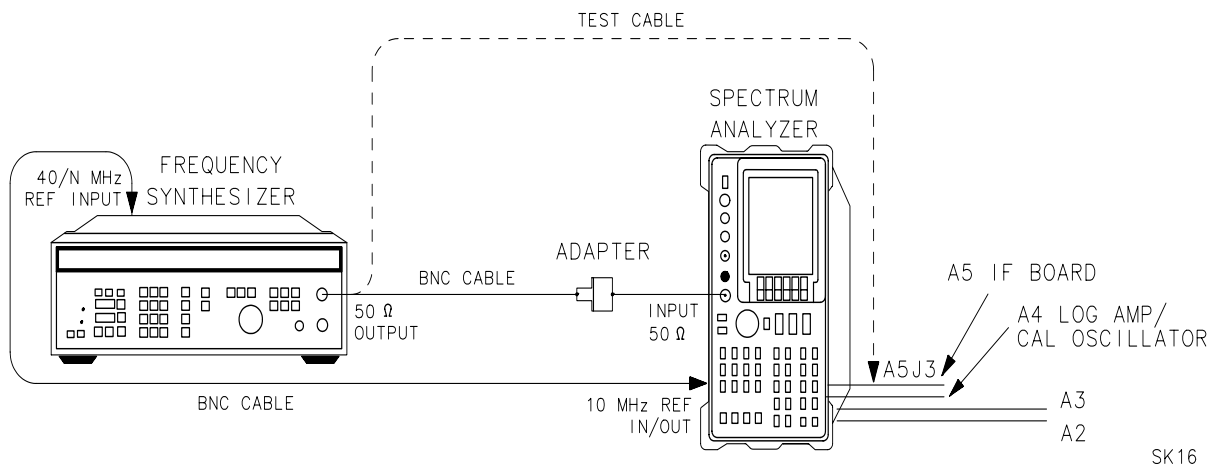
Equipment

Frequency synthesizer 3335A

Adapters

Type N (m) to BNC (f) 1250-1476

Cables
BNC, 122 cm (48 in) 10503A
Test cable 85680-60093

Figure 2-8   IF Amplitude Adjustment Locations
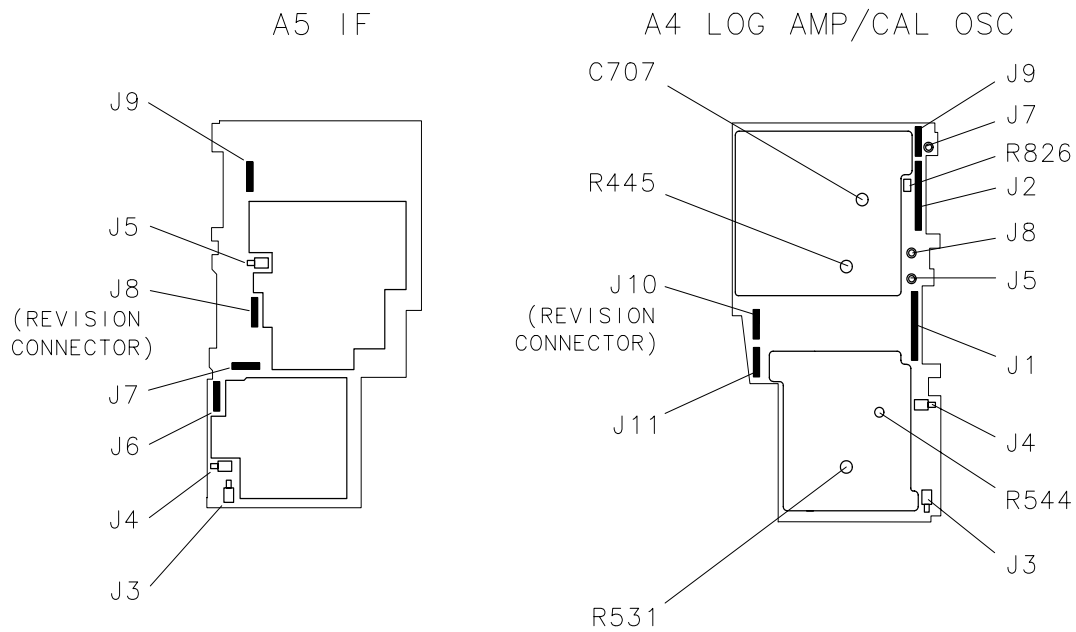
NOTE   The 15 dB reference attenuator adjustment is preset at the factory and need not be done if the entire A5 IF assembly is replaced.

Procedure

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in .

2. Disconnect W29, violet coax cable, from A5J3. Connect the test cable between A5J3 and the 50 Ω output of the 3335A. Press **LINE** to turn the spectrum analyzer on.

3. Set the spectrum analyzer controls as follows:

    > Center frequency .... 10.7 MHz
    > Span .... 200 kHz
    > Reference level .... –60 dBm
    > Attenuator .... 0 dB
    > dB/division .... 1 dB/DIV
    > Resolution bandwidth .... 300 kHz
    > Video bandwidth .... 100 Hz

4. On the spectrum analyzer, press **MKR**, **CAL**, and **IF ADJ ON OFF** so OFF is underlined.

5. Set the 3335A controls as follows:

    > Frequency .... 10.7 MHz
    > Amplitude .... –55 dBm

6. Note the marker value. Ideally it should read –60 dBm ±0.1 dB.

7. If the marker reads below –60.1 dBm, rotate A4R826 CAL OSC AMPTD one-third turn clockwise for every 0.1 dB below –60 dBm. If the marker reads above –59.9 dBm, rotate A4R826 CAL OSC AMPTD one-third turn counter clockwise for every 0.1 dB above –60 dBm. See for the location of A4R826. A change in the displayed amplitude will not be seen until **ADJ CURR IF STATE** is pressed.

NOTE   If A4R826 has inadequate range, refer to .

8. Press **ADJ CURR IF STATE**. After allowing the analyzer time to complete the adjustments, the displayed amplitude and marker reading should change.

9. Repeat steps 7 and 8 until the marker reads –60 dBm ±0.1 dB.

10. Disconnect the test cable from A5J3 and reconnect W29 to A5J3.

A5 Reference Attenuator Adjustment

1. Set the spectrum analyzer reference level to –60 dBm. If markers are displayed, press **MKR** and **MARKERS OFF**.

2. Set the 3335A **AMPLITUDE** to –60 dBm.

3. Connect a BNC cable between the 50 Ω output of the 3335A and the spectrum analyzer INPUT 50Ω .

4. On the spectrum analyzer, press **CAL** and **REF LVL ADJ**. Use the front-panel knob or step keys to place the peak of the displayed signal 3 dB to 5 dB below the reference level.

5. Press **PEAK SEARCH** and **MARKER DELTA** on the spectrum analyzer. Set the spectrum analyzer reference level to –10 dBm.

6. Change the 3335A **AMPLITUDE** to –10 dBm.

7. Press **CAL** on the spectrum analyzer.

8. Note the ΔMKR amplitude. Ideally, it should read 50.00 dB ±0.1 dB.

9. If the ΔMKR amplitude is less than 49.9 dB, rotate A5R343 15 dB ATTEN one-half turn counterclockwise for each 0.1 dB below 50.00 dB. If the ΔMKR amplitude is greater than 50.1 dB, rotate A5R343 15 dB ATTEN one-half turn clockwise for each 0.1 dB above 50.00 dB. Do not adjust A5R343 more than five turns before continuing with the next step.

10. Press **ADJ CURR IF STATE** on the spectrum analyzer. Note the ΔMKR amplitude reading.

11. Repeat steps 11 through 20 until the ΔMKR amplitude reading is 50.00 dB ±0.1 dB.

A5 Adjustment Verification

1. On the spectrum analyzer, disconnect W29 from A5J3. Connect the test cable between A5J3 and the 50 Ω output of the 3335A.

2. Set the spectrum analyzer reference level to –10 dBm.

3. Set the 3335A **AMPLITUDE** to –5 dBm.

4. Press **MKR** and **MARKER NORMAL** on the spectrum analyzer.

5. The MARKER amplitude should read –10 dBm ±0.13 dB. If the reading is outside of this range, repeat steps 4 through 21.

6. On the spectrum analyzer, reconnect W29 to A5J3. Press **PRESET** and set the controls as follows:

    Center frequency .... 300 MHz
    Span ....0 Hz
    Reference level ....–10 dBm
    Resolution bandwidth ....300 kHz

7. Connect a BNC cable between the 8563E CAL OUTPUT and INPUT 50Ω .

8. On the spectrum analyzer, press **MKR CAL** and **REF LVL ADJ**.

9. Use the knob or step keys to adjust the REF LEVEL CAL setting until the MKR reads –10.00 dBm ±0.1 dB.

10. On the spectrum analyzer, press **STORE REF LVL**.

5. DC Log Amplifier Adjustments

There are three DC log adjustments; limiter phase, linear fidelity, and log fidelity.

Assembly Adjusted

A4 log amp/cal oscillator

Related Performance Tests

IF Gain Uncertainty Scale Fidelity

Description

These three adjustments need only be done under the following conditions:

Limiter phase   Only if a repair is made to blocks F, G, H, I, or J.

Linear fidelity   Only if a repair is made to blocks C, D, F, G, H, I, J, K, O, IF gain accuracy, RBW switching, or log fidelity.

Log fidelity   Only if a repair is made to blocks D, F, H, K, IF gain accuracy, RBW switching, or log fidelity.

If multiple adjustments are required they should be done in the following order:

1. Limiter phase

2. Linear fidelity

3. Log fidelity

Figure 2-9   DC Log Adjustment Setup
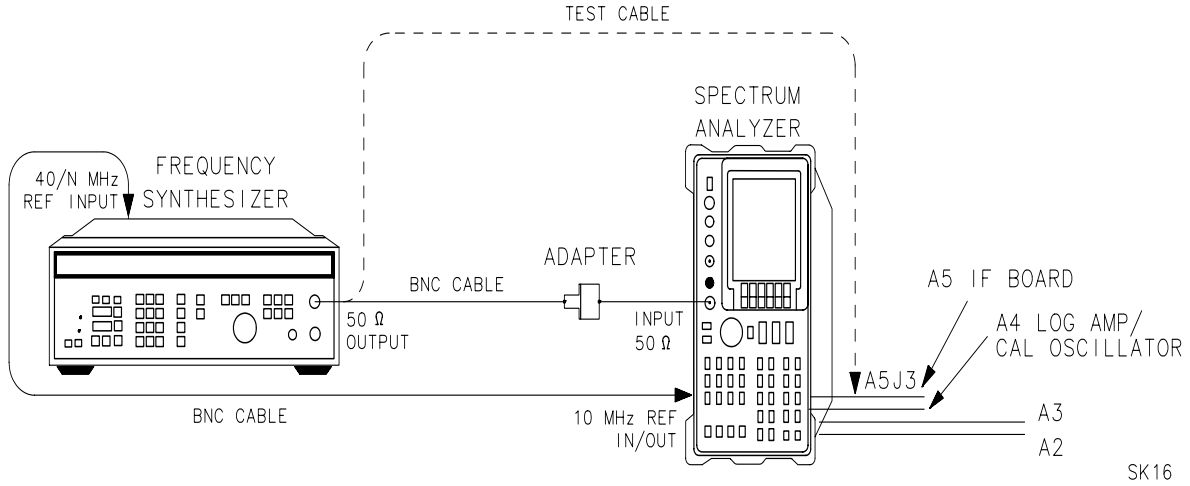
Equipment

Frequency synthesizer 3335A

Adapters

Type N (m) to BNC (f) 1250-1476

Cables

BNC, 122 cm (48 in) 10503A

Test cable 85680-60093

Figure 2-10   **DC Log Adjustment Locations**

A5 IF   A4 LOG AMP/CAL OSC
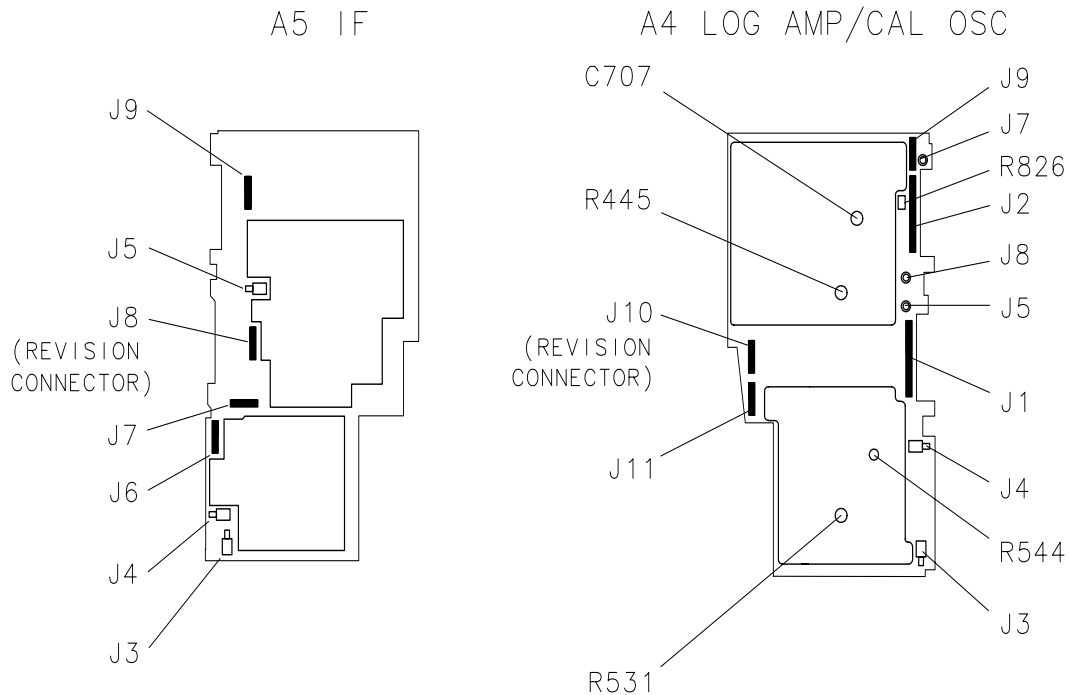
sj11e

NOTE   Adjustments should be made with all of the shields on and only after
allowing at least a 20 minute warm-up.

A4 Limiter Phase Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum
   analyzer cover and place the spectrum analyzer in the service
   position as illustrated in Figure 2-9 on page 80. See Figure 2-10 on
   page 81 for adjustment location.

2. Connect the 3335A 50 Ω output to the spectrum analyzer 50 Ω input.
   Press **LINE** to turn the spectrum analyzer on.

3. Set the spectrum analyzer controls as follows:

   Center frequency .... 15 MHz
   Span .... 0 Hz
   Reference level .... −10 dBm
   dB/division .... 1 dB/DIV
   Resolution bandwidth .... 300 kHz
   IF ADJ .... OFF

4. Set up an 3335A as follows:

   Frequency .... 15 MHz
   Amplitude .... −18 dBm

5. Press **CAL**, **ADJ CURR IF STATE**, wait for the analyzer to complete adjustments, then press **MKR**.

6. Adjust A4R445 for maximum on-screen amplitude. Refer to Figure 2-10 on page 81 for the location of A4R445.

A4 Linear Fidelity Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in Figure 2-9 on page 80. See Figure 2-10 on page 81 for adjustment location.

2. Connect the 3335A 50 Ω output to the spectrum analyzer 50 Ω input. Press **LINE** to turn the spectrum analyzer on.

3. Press **PRESET**, **AMPLITUDE**, **LINEAR**, **MORE 1 of 3**, **AMPTD UNITS,dBm**, **CAL**, **IF ADJ ON OFF**, (OFF).

4. Set the spectrum analyzer controls as follows:

    Center frequency .... 15 MHz
    Span .... 5 MHz
    Resolution bandwidth ....300 kHz
    Reference level ....−10 dBm

5. Set up an 3335A as follows:

    Frequency .... 15 MHz
    Amplitude ....−10 dBm

6. Press **PEAK SEARCH**, **MARKER DELTA**.

7. Reduce the 3335A input power to −58 dBm.

8. If the delta marker amplitude reads −40 dB ±2 dB, no adjustment is necessary.

9. If the signal is lower on the screen than expected (delta marker amplitude reads less than −42dB), then adjust A4R544 (see Figure 2-10 on page 81) for an even lower level and press **CAL**, **ADJ CURR IF STATE**. Allow sufficient time for the analyzer to complete the adjustment.

10. If the signal is higher on the screen than expected (delta marker amplitude reads greater than −38 dB), then adjust A4R544 for an even higher level signal and press **CAL**, **ADJ CURR IF STATE**. Allow sufficient time for the analyzer to complete the adjustment.

11. Repeat steps 5 through 10.

A4 LOG Fidelity Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in Figure 2-9 on page 80. See Figure 2-10 on page 81 for adjustment location.

2. Connect the 3335 50 Ω output to the spectrum analyzer 50 Ω input. Press **LINE** to turn the spectrum analyzer on.

3. Press **PRESET**, **CAL**, **IF ADJ ON OFF** (OFF), **ADJ CURR IF STATE**.

4. Set the spectrum analyzer controls as follows:

    Center frequency .... 15 MHz
    Span .... 0 Hz
    Resolution bandwidth .... 300 kHz
    Reference level .... –10 dBm

5. Set up an 3335A as follows:

    Frequency .... 15 MHz
    Amplitude .... –10 dBm

6. Press **MKR**, **MARKER DELTA** on the spectrum analyzer.

7. Decrease the 3335A power to –26 dBm.

8. Calculate the error:

    Error = delta marker reading – 16 dB

9. If the error is less than ±0.2 dB, no adjustment is necessary.

10. Set the 3335A power to –10 dBm.

11. Adjust A4R531 (see Figure 2-10 on page 81) to read two times the error. For example, if the calculated error is +0.75 dB, adjust A4R531 for a delta marker amplitude reading of +1.5 dB. Press **CAL**, **ADJ CURR IF STATE**.

12. Repeat steps 7 through 11.

6. Sampling Oscillator Adjustment

Assembly Adjusted

A15 RF assembly

Related Performance Test

There is no related performance test for this adjustment procedure.

Description

The sampling oscillator tank circuit is adjusted for a tuning voltage of 5.05 Vdc when the sampling oscillator is set to 297.222 MHz. The voltage monitored is actually the tuning voltage divided by 4.05. The setting is then checked at other frequencies for the full tuning range of the sampling oscillator.

Figure 2-11   **Sampler Adjustment Setup**
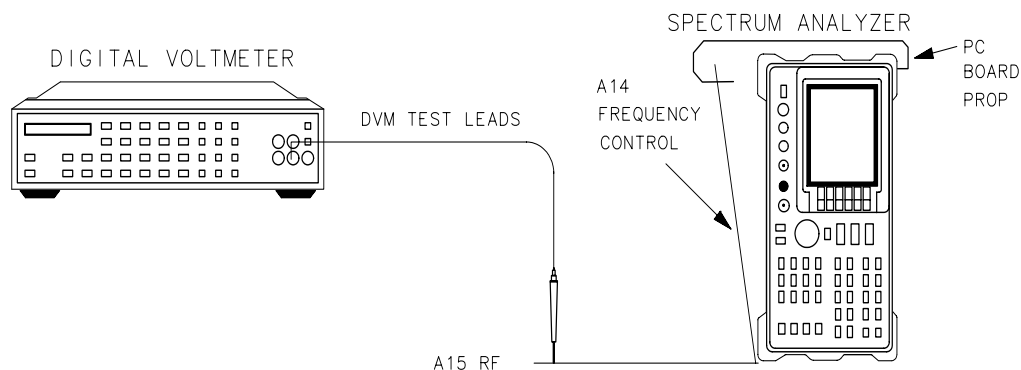
Equipment

Digital voltmeter 3456A

DVM test leads 34118A

Procedure

1. Press **LINE** to turn the spectrum analyzer off and disconnect the line power cord. Remove the spectrum analyzer cover and fold down the A15 RF and A14 frequency control assemblies. Prop up the A14 frequency control assembly. Reconnect the line power cord and press **LINE** to turn the spectrum analyzer on. Connect the equipment as illustrated in Figure 2-11 on page 84.

2. Press **PRESET** on the spectrum analyzer and set the controls as follows:

    Center frequency .... 2126 MHz
    Span ....0 Hz

3. Set the 3456A controls as follows:

    Function ....DC VOLTS
    Range .... 10 V, MANUAL

Sampling Oscillator Adjustment

1. Connect the negative DVM test lead to A15J200 pin 6. Connect the positive DVM lead to A15J200 pin 13.

2. Adjust A15C210 VCO RANGE for a DVM reading of 5.05 V ±0.05 V.

Figure 2-12   **TAM Connector Pin Locations**


```
PIN 2  ● ● ● ● ● ● ● ●  PIN 16
PIN 1  ■ ● ● ●   ● ● ●
```
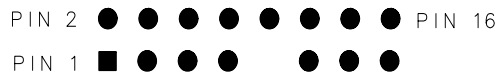
SP114E

Sampler Match Adjustment

1. Connect the negative DVM test lead to A15J400 pin 6, and the positive DVM test lead to A15J400 pin 1.

2. Press **FREQUENCY** and set the spectrum analyzer center frequency to 2302.3 MHz. This sets the sampling oscillator to 291.667 MHz.

3. Adjust A15C100 SMPL MATCH to peak the voltage displayed on the DVM.

4. Record the displayed voltage in Table 2-11 on page 86 as the displayed voltage for the sampling oscillator frequency of 291.667 MHz.

5. Press **FREQUENCY** on the spectrum analyzer. Use the keypad to set the spectrum analyzer center frequency to the frequencies listed in Table 2-11 on page 86. At each listed frequency, record the displayed voltage in the table.

6. If the difference between the maximum and minimum voltages is less than 0.50 V, and all voltage readings are between +0.5 and +2.5 Vdc, proceed to step 15.

7. Locate the center frequency at which the voltage is lowest. Use the keypad to set the spectrum analyzer to this frequency.

8. Readjust SMPL MATCH to set the displayed voltage to 0.8 ±0.1 Vdc.

9. Set the spectrum analyzer center frequency to 2302.3 MHz and repeat steps 9 through 13.

10. Move the positive DVM test lead to A15J400 pin 3. Check that the measured voltage is the negative of the voltage at pin 1, within ±0.1 Vdc.

11. Disconnect the DVM probes from A15J400.

Table 2-11   **Sampling Adjustments**

Center Frequency (MHz)	Sampling Oscillator (MHz)	Displayed Voltage (Vdc)				
		1st Trial	2nd Trial	3rd Trial	4th Trial	5th Trial
2156.3	285.000					
2176.3	286.364					
2230.3	288.462					
2263.3	290.000					
2302.3	291.667					
2158.3	293.478					
2196.3	295.000					
2378.3	296.471					
2422.3	297.222					

7. YTO Adjustment

Assembly Adjusted

A14 frequency control assembly

Related Performance Tests

Frequency Span Accuracy Frequency Readout Accuracy and Frequency Count Marker Accuracy

Description

The YTO main coil adjustments are made with the phase-lock loops disabled. The YTO endpoints are adjusted to bring these points within the capture range of the main loop. The YTO FM coil is adjusted to place the 300 MHz CAL OUTPUT signal at the center vertical graticule in a 20 MHz span.

Figure 2-13   YTO Adjustment Setup
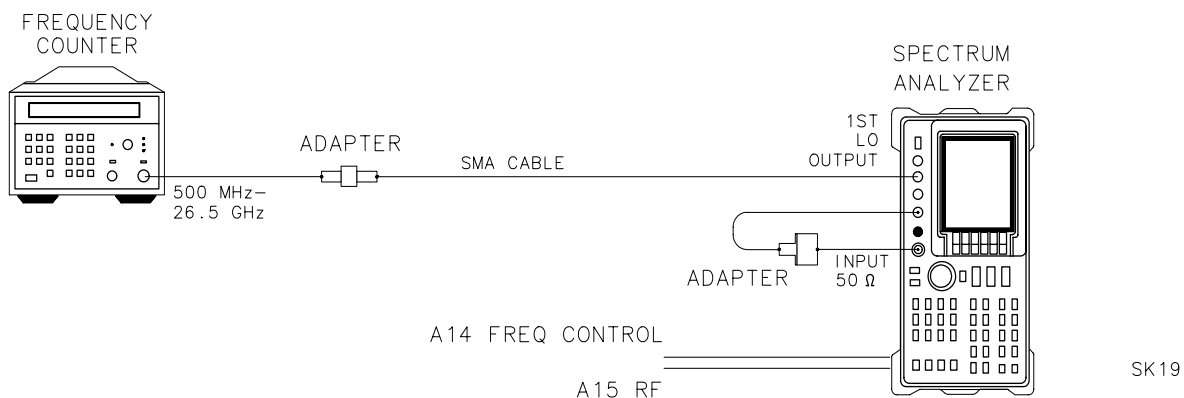
Equipment

Microwave frequency counter .... 5343A Option 001

Adapters

Type N (m) to BNC (f) 1250-1476

Type N (f) to APC 3.5 (f) **(Option 026 only)**........... 1250-1745

APC 3.5 (f) to APC 3.5 (f) 5061-5311

Cables

BNC, 122 cm (48 in) 10503A

SMA, 61 cm (24 in) 8120-1578

Procedure

This adjustment cannot be performed if preselected external mixer mode is selected.

The **SAVELOCK ON OFF** function must be OFF.

YTO Main Coil Adjustments

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and fold down the A15 RF and A14 frequency control assemblies.

2. Disconnect the 50 Ω termination from the first LO OUTPUT. Connect the equipment as shown in Figure 2-13 on page 87. Press **LINE** to turn the spectrum analyzer on.

3. Move the jumper on A14J23 from the NORM position (pins 1 and 2 jumpered) to the TEST position (pins 2 and 3 jumpered). See Figure 2-14 on page 89 for the location on the A14 frequency control assemblies.

4. On the spectrum analyzer, press the following keys:

    CONFIG EXT MXR PRE UNPR, (UNPR) **AUX CTRL, EXTERNAL MIXER, LOCK HARMONIC**, 6 Hz **SPAN, ZERO SPAN FREQUENCY, CENTER FREQ**, 18.8893 GHz, **SGL SWP SAVE, SAVE STATE, STATE 0 FREQUENCY**, 35.7493 GHz **SAVE, SAVE STATE, STATE 1 RECALL, RECALL STATE, STATE 0**.

5. On the 5343A, press **SHIFT** 7 and set the controls as follows:

    Sample rate ....Fully counterclockwise
    10 Hz — 500 MHz/500 MHz — 26.5 GHz switch.......500MHz — 26.5 GHz

6. Adjust A14R93 3.2 GHz for the appropriate frequency counter reading of 3.200 GHz ±1 MHz.

7. On the spectrum analyzer, press **STATE 1**.

8. Adjust A14R42 6.01 GHz for a frequency counter reading of 6.010 GHz ±1 MHz.

9. On the spectrum analyzer, press **STATE 0**.

10. Repeat steps 6 through 9 until both of these interacting adjustments meet their tolerances.

Figure 2-14   YTO Adjustment Locations
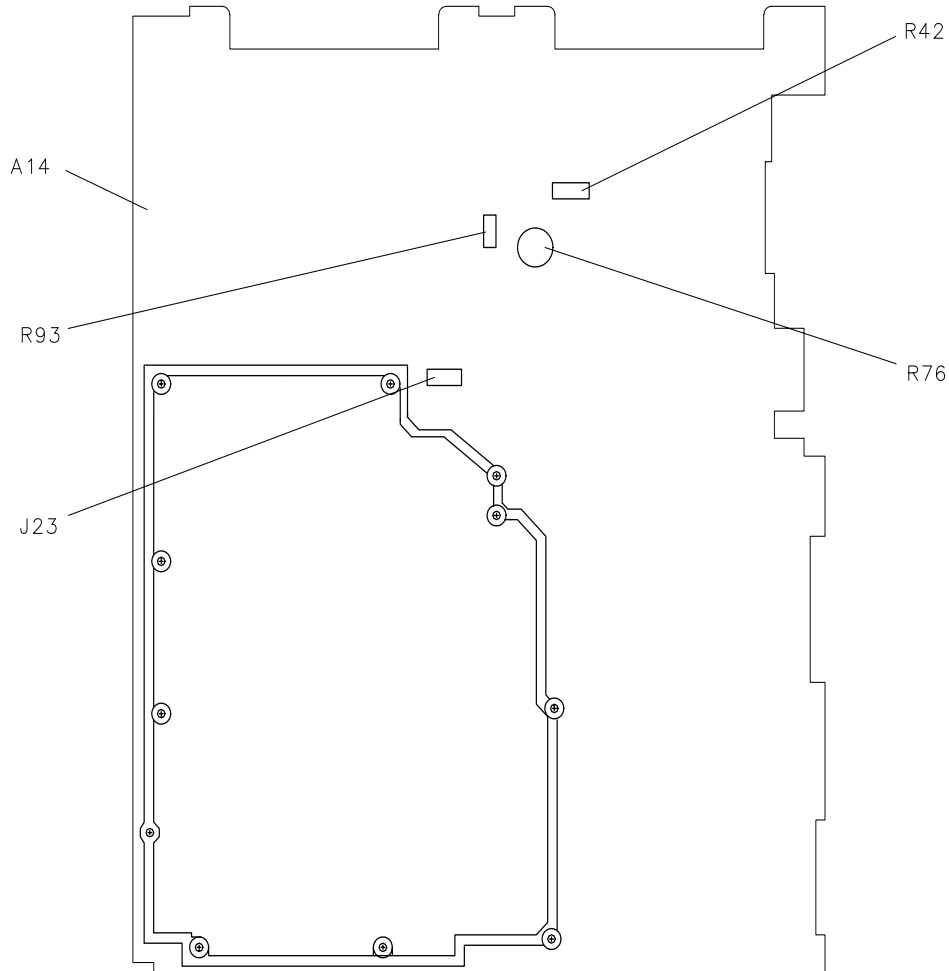
SP116E

11. Place the jumper on A14J23 in the NORM position (pins 1 and 2 jumpered).

12. Disconnect the SMA cable from the first LO OUTPUT jack and reconnect the 50Ω termination on the first LO OUTPUT.

YTO FM Coil Adjustments

On the spectrum analyzer, press **PRESET** and set the controls as follows:

Center frequency .... 300 MHz

Span .... 20 MHz

Adjust A14R76 FM SPAN until the 300 MHz CAL OUTPUT SIGNAL is aligned with the center vertical graticule line.

8. LO Distribution Amplifier Adjustment

Assembly Adjusted

A14 frequency control assembly

Related Performance Test

First LO OUTPUT Amplitude

Description

The gate bias and SENSE voltages for the A7 switched LO distribution amplifier is adjusted to the value specified on the label of A7.

Figure 2-15   First LO Distribution Amplifier Adjustment Setup
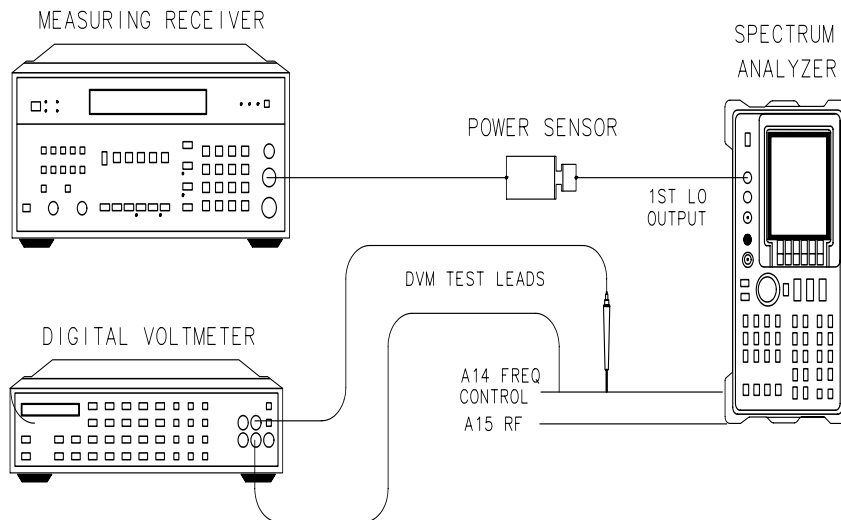
Equipment

DVM 3456A

DVM test leads 34118A

Procedure

1. Set the 8562E/EC **LINE** switch to off and disconnect the line cord. Remove the cover and fold down the A15 RF and A14 Frequency Control assemblies.

2. Move the jumper on A2J12 from the WR PROT to the WR ENA position. The jumper is on the edge of the A2 board assembly and can be moved without folding the board down.

3. Reconnect the line cord and turn on the spectrum analyzer.

4. Set the 8562E/EC controls as follows:

    Center frequency ....1.45 GHz
    Span ....0 Hz

5. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **LO LEVELS**, and **INT LO LEVEL**.

6. Use the knob or keypad to enter the value 32. This sets the LO power to a low level.

7. To set the gate bias, connect the positive lead of the DVM to A14J18 pin 15 and the negative lead to A14J18 pin 6. See Figure 2-16 on page 91 for a pin location drawing.

Figure 2-16   TAM Connector Pin Locations

PIN 2 ● ● ● ● ● ● ● ● PIN 16
PIN 1 ■ ● ● ●   ● ● ●
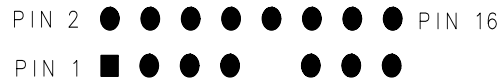
SP114E

8. On the 8562E/EC, press **LO GATE LEVEL**.

9. Note the Gate Bias voltage printed on the A7 LO distribution amp label. Use the knob or keypad to change the displayed DAC value so the DVM reading is equal to the label voltage, ±10 mV.

10. To set the low band sense voltage, connect the positive lead of the DVM to A14J18 pin 13 and the negative lead to A14J18 pin 6.

11. On the 8562E/EC, press **INT LO LEVEL**. The message `DRIVE FOR BAND# 0` will be displayed.

12. Note the "B0 EXT Sense" voltage printed on the A7 LO distribution amp label. Use the knob or keypad, and press enter, to change the displayed DAC value so the DVM reading is 6 mV more negative than the label voltage. For example, if the "BO EXT Sense" voltage is −170 mV, change the displayed DAC value so the DVM reading is −176 mV.

13. Record the DAC value:

    DAC value for 1.45 GHz = _____

14. To set the band 1 sense voltage, set the 8562E/EC center frequency to 4.60 GHz.

15. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **LO LEVELS**, and **INT LO LEVEL**. The message `DRIVEFOR BAND# 1` will be displayed.

16. Note the "B1 INT Sense" voltage printed on the A7 LO distribution amp label. Use the knob or keypad, and press enter, to change the displayed DAC value so the DVM reading is 6 mV more negative than the label voltage. For example, if the "B1 INT Sense" voltage is −170 mV, change the displayed DAC value so the DVM reading is −176 mV.

17. Record the DAC value:

   DAC value for 4.60 GHz =_____

18. To set the band 2 sense voltage, set the 8562E/EC center frequency to 9.46 GHz.

19. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **LO LEVELS**, and **INT LO LEVEL**. The message `DRIVE FOR BAND# 2` will be displayed.

20. Note the "B2 INT Sense" voltage printed on the A7 LO distribution amp label. Use the knob or keypad, and press enter, to change the displayed DAC value so the DVM reading is 6 mV more negative than the label voltage. For example, if the "B2 INT Sense" voltage is −170 mV, change the displayed DAC value so the DVM reading is −176 mV.

21. Set the "Sense EXT" value by pressing **EXT LO LEVEL**.

22. Use the knob or keypad to enter the DAC value for 1.45 GHz from the band 0 sense voltage adjustment above.

23. Save the adjustment values by pressing **PREV MENU**, **STORE DATA**, and **YES**.

24. Move the jumper on A2J12 from WR ENA back to the WR PROT position.

9. Frequency Response Adjustment

Assembly Adjusted

A15 RF assembly

Related Performance Tests

Displayed Average Noise Level Frequency Response

Description

A signal of the same known amplitude is applied to the spectrum analyzer at several different frequencies. At each frequency, the DAC controlling the flatness compensation amplifiers is adjusted to place the peak of the displayed signal at the same place on the screen. The preselector is centered at each frequency before setting the DAC value. There are also correction points at 2 MHz and 6 MHz, which are outside the synthesized sweeper frequency range. The DAC values for these two points are set to a fixed offset from the DAC value at 10 MHz. The DAC values are stored in EEROM.

Automated Procedure Available

The frequency response adjustment requires making several measurements at more than 120 different frequencies over the spectrum analyzer frequency range. This manual procedure takes over two hours to complete. However, an automated procedure, with software, is provided by Agilent Technologies. The software can allow the adjustment to be performed in less than 20 minutes. The Automated 8562E "Front End Cal" adjustment performs this task, and is described in Chapter 3 , "Frequency Response Adjustment Software."

Figure 2-17   **Frequency Response Adjustment Setup**
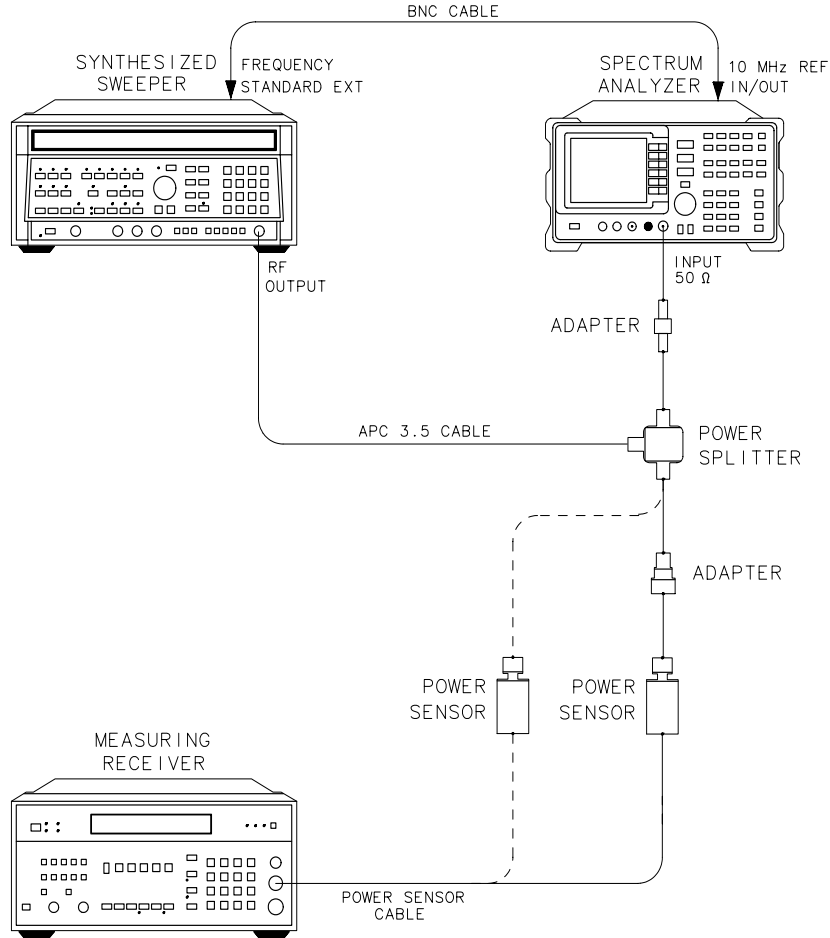
Equipment

Synthesized sweeper 8340A/B

Measuring receiver 8902A

Power sensor 8482A

Power sensor 8485A

Power splitter 11667B

Adapters

Type N (m) to Type N (m) 1250-1475

Type N (m) to APC 3.5 (m) 1250-1743

Type N (f) to APC 3.5 (m) 1250-1750

Type APC 3.5 (f) to APC 3.5 (f) 5061-5311

Cables

BNC, 122 cm (48 in) 10503A

APC 3.5, 91 cm (36 in) 8120-4921

Procedure

The YIG-tuned filter/mixer slope and offset adjustment must be correct before the high band part of the frequency response adjustment can be done.

1. Connect the equipment as shown in Figure 2-17 on page 94. Do not connect the 8482A power sensor to the 11667B power splitter.

2. Zero and calibrate the 8902A/8482A combination in log mode (power levels read out in dBm) and connect the power sensor through an adapter to the power splitter.

3. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR ENA position. The jumper is on the edge of the A2 board assembly and can be moved without folding the board down.

4. Press **PRESET** on the 8562E/EC and set the controls as follows:

   Center frequency .... 10 MHz
   Span ....0 Hz
   Resolution bandwidth ....300 kHz
   dB/division ....2 dB

5. Press **INSTR PRESET** on the 8340A/B and set the controls as follows:

   CW frequency .... 10 MHz
   Power level ....−4 dBm

6. Set ref level cal DAC to zero. Press **CAL**, **REF LVL ADJ** and use the knob to set the value to 0. Press **STORE REF LVL**.

7. On the 8562E/EC, press **MKR**, **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, then **FLATNESS**. The current value of the RF Gain DAC should be displayed in the active function area.

8. Enter the appropriate power sensor calibration factor into the 8902A.

9. Set the 8340A/B **CW** output to the frequency indicated in the active
    function area of the 8562E/EC display. Adjust the 8340A/B
    POWER LEVEL for a –10 dBm reading on the 8902A.

10. On the 8562E/EC, adjust the RF gain DAC value using the
    front-panel knob or keypad until the marker reads –10 dBm
    ±0.10 dB. Each DAC count results in an amplitude change of
    approximately 0.01 dB.

11. On the 8562E/EC, press ⇓ to proceed to the next frequency.

12. Repeat steps 7 through 10 for all low-band frequencies ≥10 MHz.

13. Press ⇓ until 10 MHz is displayed in the active function block.
    Record the RF gain DAC value at 10 MHz.

    10 MHz RF gain DAC value = _____

14. Add 67 to the 10 MHz RF gain DAC value and record as the 2 MHz
    RF gain DAC value.

    2 MHz RF gain DAC value =_____

15. Add 62 to the 10 MHz RF gain DAC value and record as the 6 MHz
    RF gain DAC value.

    6 MHz RF gain DAC value = _____

16. Press ⇓ until 2 MHz is displayed in the active function block. Use the
    DATA keys to enter the 2 MHz RF gain DAC value recorded in
    step 14.

17. Press ⇓ until 6 MHz is displayed in the active function block. Use the
    DATA keys to enter the 6 MHz RF gain DAC value recorded in
    step 15.

18. Press **NEXT BAND** on the 8562E/EC.

19. Disconnect the 8482A and its adapter from the 11667B. Connect the
    8485A to the 8902A. Zero and calibrate the 8902A/8485A
    combination. Connect the 8485A to the 11667B power splitter.

20. Enter the appropriate power sensor calibration factor into the
    8902A.

21. Set the 8340A/B **CW** output to the frequency indicated in the active
    function area of the 8562E/EC display.

22. Adjust the 8340A/B POWER LEVEL to place the signal midscreen
    on the 8562E/EC display.

23. On the 8562E/EC, press **PRESEL AUTO CTR**.

24. Adjust the 8340A/B POWER LEVEL for a –10 dBm reading on the 8902A.

25. On the 8562E/EC, adjust the RF gain DAC value using the knob or keypad until the marker reads –10 dBm ±0.10 dB.

26. On the 8562E/EC, press ⇓ to proceed to the next frequency.

27. Repeat steps 20 through 26 for the remaining frequencies in band 1.

28. On the 8562E/EC, press **NEXT BAND** to proceed to band 2.

29. Repeat steps 20 through 26 for the remaining frequencies in band 2.

30. Press **PREV MENU STORE DATA**, then **YES** on the 8562E/EC.

31. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR PROT position.

10. Calibrator Amplitude Adjustment

Assembly Adjusted

A15 RF assembly

Related Performance Test

Calibrator Amplitude and Frequency Accuracy

Description

The CAL OUTPUT amplitude is adjusted for −10.00 dBm measured directly at the front panel CAL OUTPUT connector.

Figure 2-18   Calibrator Amplitude Adjustment Setup
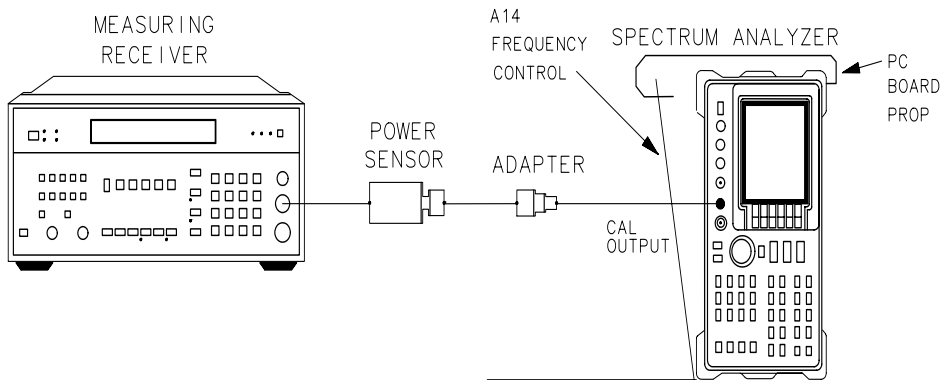
Equipment

Measuring receiver 8902A

Power sensor 8482A

Adapters

Type N (f) to BNC (m) 1250-1477

Procedure

The spectrum analyzer should be allowed to warm up for at least 30 minutes before performing this adjustment.

1. Place the spectrum analyzer in the service position shown in Figure 2-18 on page 98. Prop the A14 frequency control board assembly in the service position.

2. Zero and calibrate the 8902A/8482A combination in log display mode. Enter the power sensor 300 MHz cal factor into the 8902A.

3. Connect the 8482A through an adapter directly to the spectrum analyzer CAL OUTPUT connector.

4. Adjust A15R561 CAL AMPTD for a –10.00 dBm reading on the 8902A display.

11. 10 MHz Reference Adjustment — OCXO (Non-Option 103)

Assembly Adjusted

A21 OCXO assembly

NOTE   Replacement oscillators are factory adjusted after a complete warm-up and after the specified aging rate has been achieved. Thus, readjustment should typically not be necessary after oscillator replacement and is generally not recommended.

Related Performance Test

10 MHz Reference Accuracy

Description

The frequency of the internal 10 MHz frequency reference is compared to a known frequency standard and adjusted for minimum frequency error. This procedure does not adjust the short-term stability or long-term stability of the A21 10 MHz ovenized crystal oscillator (OCXO). Stability is determined by the characteristics of the particular oscillator and the environmental and warm-up conditions to which it has been recently exposed. The spectrum analyzer must be on continuously for at least 24 hours immediately prior to oscillator adjustment to allow both the temperature and frequency of the oscillator to stabilize.

Figure 2-19   10 MHz Reference Adjustment Setup and Adjustment Location
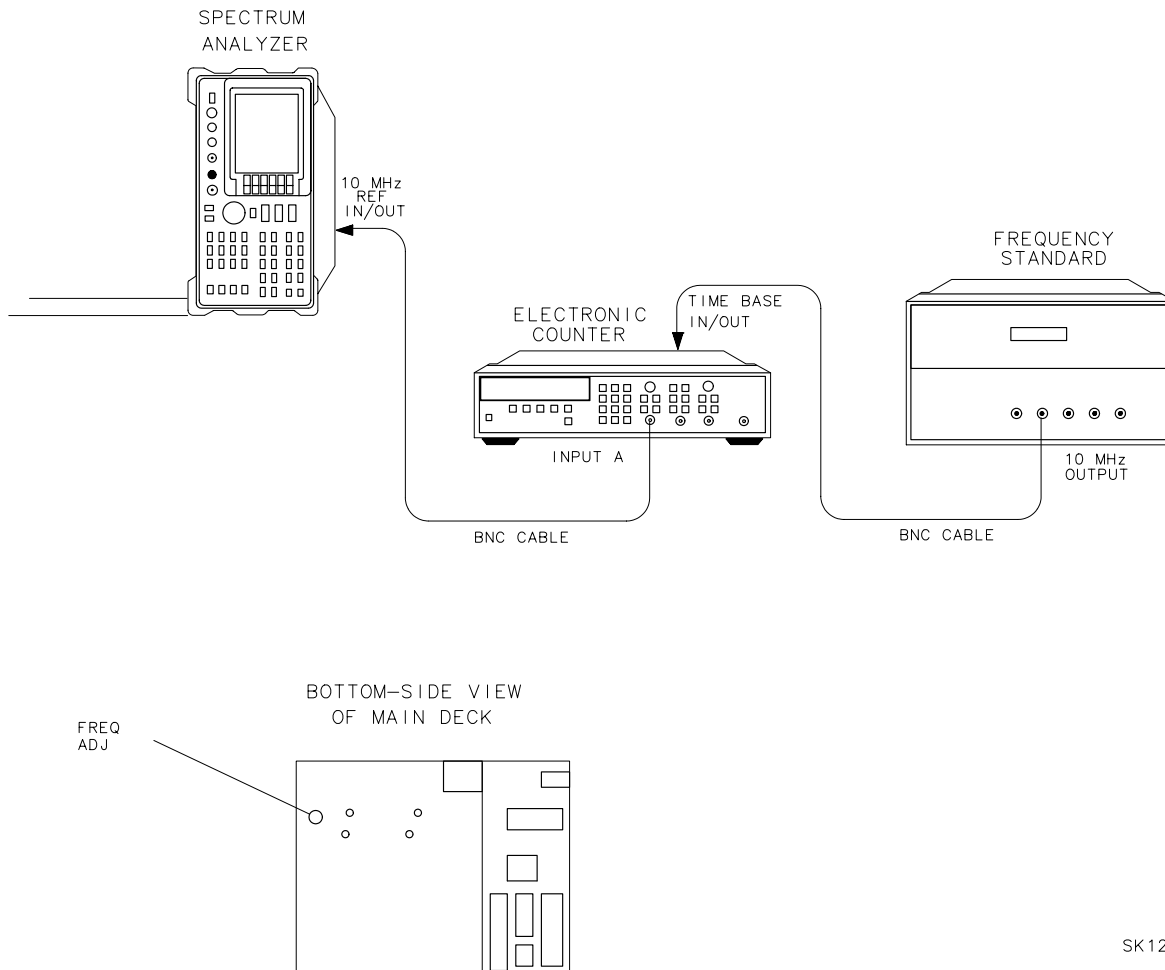
Equipment

Frequency counter 5334A/B

Frequency standard .... 5061B Cesium Beam Standard

  (or any 10 MHz frequency standard with accuracy $<\pm1$ X 10^{-10})

Cable

BNC, 122 cm **(2 required)**..10503A

Procedure

NOTE	Failure to allow a 24 hour minimum warm-up time for OCXO frequency and temperature stabilization may result in oscillator mis-adjustment.

1. Connect equipment as shown in Figure 2-19 on page 101 as follows:

   a. Press **LINE** to turn the spectrum analyzer on. After the automatic power-on adjustment sequence is complete, press **PRESET** to ensure that the frequency reference is set to internal.

   b. Allow the spectrum analyzer to remain powered on continuously for at least 24 hours to ensure that the A21 OCXO temperature and frequency stabilize.

NOTE	If the reference is set to **10 MHz EXT**, press **10 MHz INT**. Allow the 24 hour warm-up for the OCXO before continuing. When the 10 MHz reference is set to **10 MHz EXT**, the OCXO is not operating or warmed up.

   c. Connect the frequency standard to the frequency counter rear panel TIMEBASE IN/OUT connector.

   d. Connect a BNC cable between the spectrum analyzer rear panel 10 MHz REF IN/OUT connector and INPUT A on the frequency counter.

2. Set the frequency counter controls as follows:

   Function/data .... FREQ A
   Input A:
     ×10 Attenuator ....OFF
     AC... OFF (DC coupled)
     50 ΩZ.. OFF (1 MΩ input impedance)
     Auto Trigger ....ON
     100 kHz filter A ....OFF
     INT/EXT switch (rear panel) ....EXT

3. Select a 1 second gate time on the 5334A/B frequency counter by pressing **GATE TIME**, 1, **GATE TIME**.

4. To offset the displayed frequency by –10.0 MHz, press MATH **SELECT/ENTER**, **CHX/EEX**, 10, **CHS/EEX**, 6, **SELECT/ENTER**, **SELECT/ENTER**. The frequency counter should now display the difference between the frequency of the INPUT A signal and 10.0 MHz with a displayed resolution of 0.010 Hz (10 MHz).

5. Locate the FREQ ADJ control on the spectrum analyzer. This control is accessible through the center deck of the spectrum analyzer. See Figure 2-19 on page 101.

6. Remove the dust-cap screw.

7. Use a nonconductive adjustment tool to adjust the FREQ ADJ control on the A21 OCXO for a frequency counter reading of 0.00 Hz.

8. On the 5334A/B frequency counter, select a 10-second gate time by pressing **GATE TIME**, 10, **GATE TIME**. The frequency counter should now display the difference between the frequency of the INPUT A signal and 10.0 MHz with a resolution of 0.001 Hz (1 mHz).

9. Wait at least two gate periods for the frequency counter to stabilize, then adjust the FREQ ADJ control on A21 OCXO for a stable frequency counter reading of 0.000 Hz ±0.010 Hz.

10. Replace the dust-cap screw to A21 OCXO.

12. 10 MHz Reference Adjustment — TCXO (Option 103)

Assembly Adjusted

A15 RF assembly

Related Performance Test

10 MHz Reference Output Accuracy (Option 103)

Description

The frequency counter is connected to the analyzer CAL OUTPUT. The CAL OUTPUT is locked to the 10 MHz frequency reference which yields better effective resolution. The temperature-compensated crystal oscillator (TCXO) is adjusted for a frequency counter reading of 300 MHz.

Figure 2-20   **10 MHz Reference Adjustment Setup — TCXO**
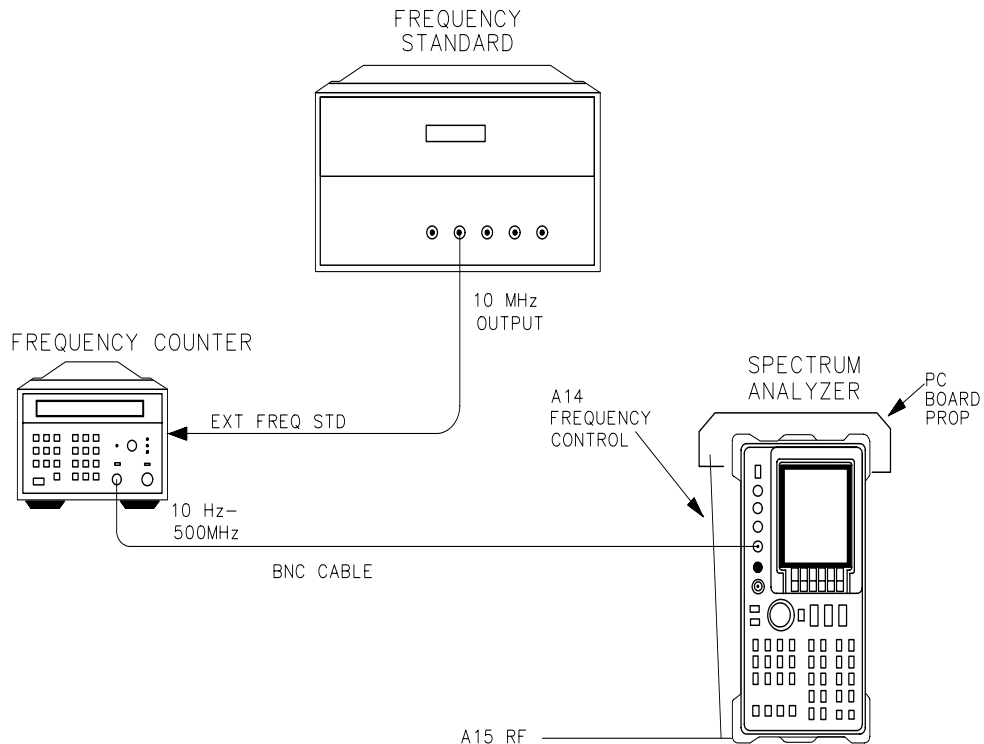
Equipment

Microwave frequency counter .... 5343A Option 001

Frequency standard .... 5061B Cesium Beam Standard

(or any 10 MHz frequency standard with accuracy $<\pm1 \text{ X } 10^{-10}$)

Cables

BNC, 122 cm **(2 required)** 10503A

Procedure

NOTE   Allow the spectrum analyzer to warm up for at least 30 minutes before performing this adjustment.

1. Connect the equipment as shown in Prop up the A14 frequency control assembly.

2. Set the frequency counter controls as follows:

   Sample rate .... Midrange
   50 Ω — 1 MΩ switch ....50 Ω
   10 Hz — 500 MHz/500 MHz — 26.5 GHz switch ...... 10 Hz — 500 MHz

3. Press **AUX CTRL REAR PANEL**. Verify that the 10 MHz reference is set to **10 MHz INT**.

NOTE   When the 10 MHz reference is set to **10 MHz EXT**, the TCXO is not operating and warmed up. If the reference is set to **10 MHz EXT**, set the reference to **10 MHz INT** and allow 30 minutes for the TCXO to warm up.

4. Remove dust cap from A15U302, TCXO. The dust cap is toward the rear of the spectrum analyzer.

5. Adjust 10 MHz ADJ on A15U302 for a frequency counter reading of 300.000000 MHz ±30 Hz.

6. Replace the dustcap on A15U302.

13. Demodulator Adjustment

Assembly Adjusted

A4 log amplifier/cal oscillator assembly

Related Performance Test

There is no related performance test for this adjustment.

Description

A 5 kHz peak-deviation FM signal is applied to the INPUT 50Ω . The detected audio is monitored by an oscilloscope. FM DEMOD is adjusted to peak the response displayed on the oscilloscope.

Figure 2-21   **Demodulator Adjustment Setup**
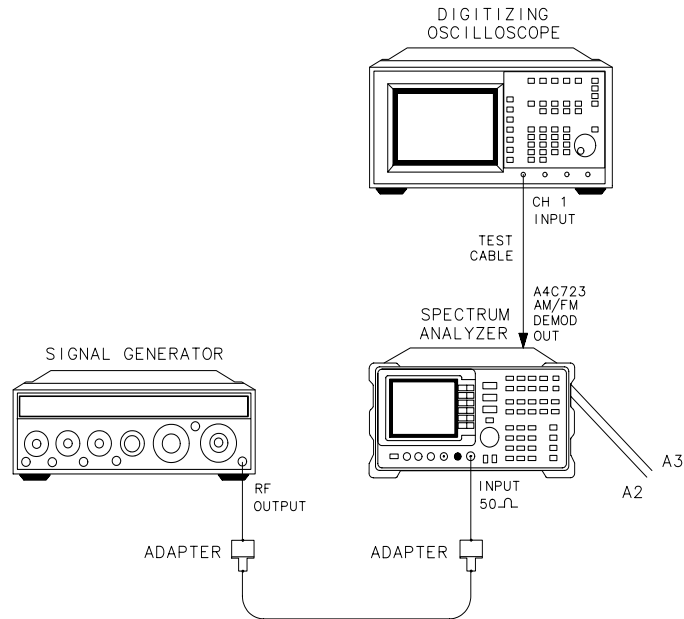
Equipment

AM/FM signal generator 8640B

Oscilloscope 54501A

Adapters

Type N (m) to BNC (f) **(2 required)** 1250-1476

Type N (f) to APC 3.5 (f) **(Option 026 only)** 1250-1745

Cables

BNC, 122 cm (48 in) 10503A

Oscilloscope probe 10432A

Procedure

1. Press **LINE** to turn the spectrum analyzer off. Place the spectrum analyzer in the service position as illustrated in .

2. Connect the oscilloscope probe from the oscilloscope channel 1 input to probe A4C723 (the end closest to A4U707) as in . Press **LINE** to turn the spectrum analyzer on. Connect the 8640B RF OUTPUT to the spectrum analyzer INPUT 50Ω .

3. Set the 8640B controls as follows:

   Range MHz .... 61 to 128
   Frequency .... 100.000 MHz
   Output level .... −10 dBm
   RF...ON
   AM ....OFF
   FM ....INT
   Modulation frequency ....1000 Hz
   Peak deviation .... 5 kHz
   Scale FM ....(k/MHz)

4. Adjust the 8640B FM deviation vernier for a full-scale reading on the meter. Set the FM to off.

5. Set the oscilloscope controls as follows:

    Channel 1 .... on
    Channel 2 .... off
    Channel 1 .... 50 mV/division
    Channel 1 ....ac
    Channel 1 ....BW lim
    Time base .... 1.0 ms/division
    Trigger ....auto
    Trigger source 1
    Trigger level ....0.0 V

6. On the spectrum analyzer, press **PRESET**, then set the controls as follows:

    Center frequency .... 100 MHz
    Span .... 5 MHz
    Reference level .... −10 dBm
    Resolution bandwidth .... 100 kHz

7. On the spectrum analyzer press: **PEAK SEARCH**, **MARKER →CF SPAN**, **ZERO SPAN AUX CTRL**, **AM/FM DEMOD**, **FM DEMOD ON OFF**(ON) **CAL**, **IF ADJ ON OFF** (OFF) **TRIG**, and **SWEEP CONT SGL** (SGL). Set the volume control to midrange.

8. A 1 kHz sine wave should be observed on the oscilloscope. Rotate the volume knob on the front panel of the spectrum analyzer until the amplitude of the 1 kHz signal is at about 150 mV (3 divisions on the oscilloscope).

9. Adjust A4C707 FM DEMOD for a maximum peak-to-peak response on the oscilloscope.

10. Press **LINE** to turn the spectrum analyzer off. Disconnect the test cable from A4C723.

Figure 2-22   **Demodulator Adjustment Locations**
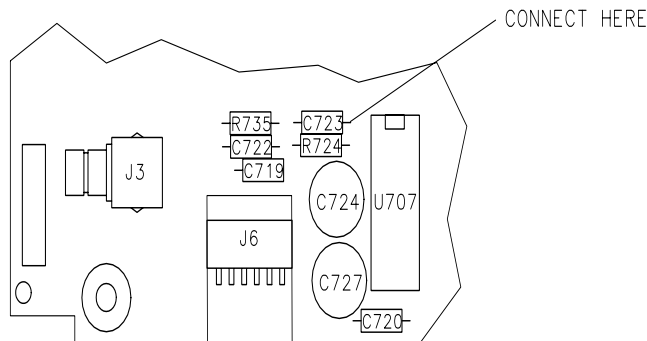
14. External Mixer Bias Adjustment (Non-Option 327)

Assembly Adjusted

A15 RF assembly

Related Performance Test

There is no related performance test for this adjustment.

Description

A voltmeter is connected to the spectrum analyzer IF INPUT with the external mixer bias set to off. The bias is adjusted for a 0 Vdc output.

Figure 2-23   **External Mixer Bias Adjustment Setup**
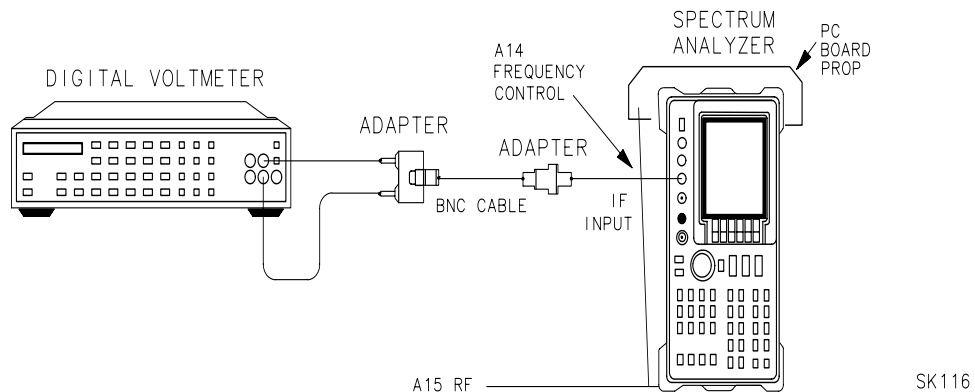
Equipment

DVM 3456A

Adapters

Type BNC (f) to SMA (m) 1250-1200

Type BNC (f) to dual banana plug 1251-2816

Cables

BNC, 122 cm (48 in) 10503A

Procedure

1. Press **LINE** to turn the spectrum analyzer off, and disconnect the ac power cord. Remove the spectrum analyzer cover and connect the equipment as illustrated in . Fold down the A15 RF assembly. Reconnect the power cord and set the **LINE** switch to on.

2. Set the 3456A controls as follows:

   Function ....DC VOLTS
   Range ....0.1 V
   Resolution ....100 mV

3. On the spectrum analyzer press **AUX CTRL**, **EXTERNAL MIXER**, **BIAS**, then **BIAS OFF**.

4. Adjust A15R926 EXT BIAS ZERO for a DVM reading of 0.000 Vdc ±12.5 mV.

15. External Mixer Amplitude Adjustment (Non-Option 327)

Assembly Adjusted

A15 RF assembly

Related Performance Test

IF Input Amplitude Accuracy

Description

The slope of the flatness compensation amplifiers is determined. The user-loaded conversion losses for K-band are recorded and reset to 30 dB. A 310.7 MHz signal is applied to the power sensor and the power level of the source is adjusted for a −30 dBm reading. The signal is then applied to the IF INPUT. The flatness compensation amplifiers are then adjusted (via DACs) to place the displayed signal at the reference level.

Figure 2-24   **External Mixer Amplitude Adjustment Setup**
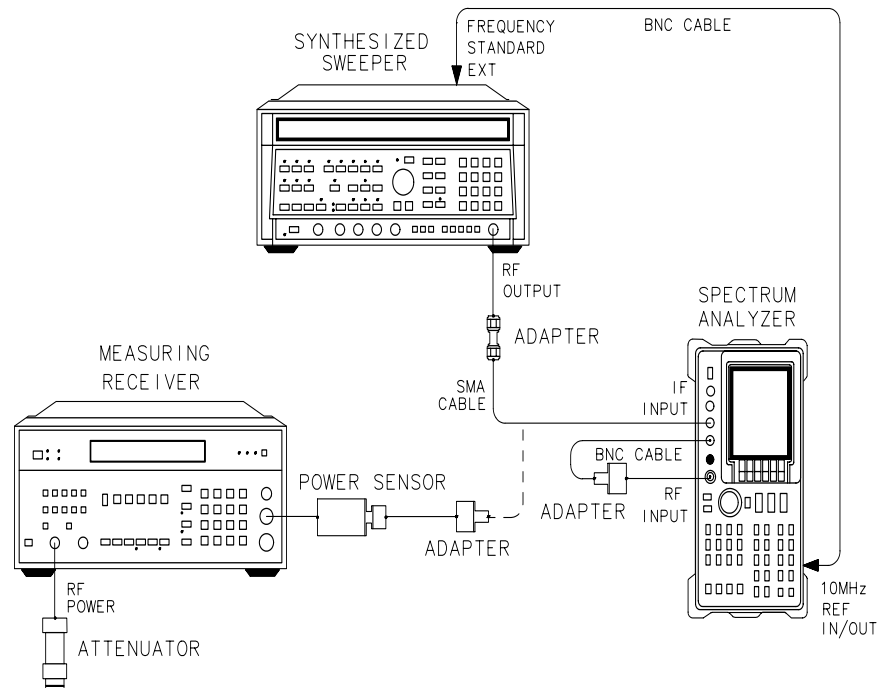
Equipment

Synthesized sweeper 8340A/B
Measuring receiver 8902A
Power sensor 8481D
50 MHz reference attenuator 11708A
  (supplied with 8481D)

Adapters
Type N (f) to SMA (f)... 1250-1772
Type N (m) to BNC (f) 1250-1476
Type APC 3.5 (f) to APC 3.5 (f) 5061-5311

Cables
BNC, 122 cm (48 in) 10503A
SMA, 61 cm (24 in) 8120-1578

Procedure

1. Press **LINE** to turn the spectrum analyzer off and disconnect the power cord. Remove the spectrum analyzer cover and reconnect the power cord.

2. Set up the equipment as illustrated in Figure 2-24 on page 111. Do not connect the SMA cable to the spectrum analyzer.

3. Press ⇓ or ⇓ to display the conversion loss value for each frequency listed in Table 2-12 on page 113. Record any conversion loss reading **not equal** to 30 dB in Table 2-12 on page 113 at the appropriate frequency.

4. Move the WR PROT/WR ENA jumper on the A2 controller assembly to the WR ENA position. The jumper is on the edge of the A2 board assembly and can be moved without folding the board down.

5. Press **LINE** to turn the spectrum analyzer on. On the spectrum analyzer, press **CONFIG**, **EXT MXR PRE UNPR**, (UNPR), **AUX CTRL**, **EXTERNAL MIXER**, **AMPTD CORRECT**, then **CNV LOSS VS FREQ**.

6. If all conversion loss values equal 30 dB, skip to step 7, otherwise continue to step a.

   a. Refer to Table 2-12 on page 113 and press ⇓ or ⇓ to select a frequency at which the conversion loss value does not equal 30 dB.

   b. Use the spectrum analyzer front-panel keys to set the conversion loss value to 30 dB.

   c. Repeat steps a and b for all frequencies having a conversion loss value other than 30 dB.

7. Press **INSTR PRESET** on the 8340A/B and set the controls as follows:

   CW frequency .... 310.7 MHz
   Power level .... −30 dBm

Table 2-12 **Conversion Loss Data**

Frequency (GHz)	Conversion Loss (dB) (≠30 dB)
18	
20	
22	
24	
26	
27	

8. Connect the 8481D to the 11708A attenuator already connected to the 8902A RF power connector. Zero and calibrate the 8902A/8481D combination in log mode. Enter the power sensor 50 MHz cal factor into the 8902A. Connect the power sensor, through an adapter, to the SMA cable.

9. Adjust the 8340A/B **POWER LEVEL** until the power displayed on the 8902A reads −30 dBm ±0.05 dB.

10. On the spectrum analyzer, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **3RD IF AMP**, then **CAL 3RD AMP GAIN**.

11. Wait until the message ADJUSTMENT DONE appears in the active function block and press **EXT MXR REF CAL**.

12. Disconnect the SMA cable from the power-sensor/adapter and connect the cable to the spectrum analyzer IF INPUT.

13. Use the spectrum analyzer front-panel knob, step keys, or keypad to change the amplitude of the displayed signal until the marker reads 0 dBm ±0.17 dB.

14. Press **PREV MENU**, **STORE DATA**, and **YES** on the spectrum analyzer.

15.Place the WR PROT/ WR ENA jumper on the A2 controller assembly in the WR PROT position.

NOTE   The following steps should only be performed if you need to replace the 30 dB conversion loss values to those recorded in Table 2-12 on page 113.

16.Press **AUX CTRL**, **EXTERNAL MIXER**, **AMPTD CORRECT**, then **CNV LOSS VS FREQ** on the spectrum analyzer.

17.Press ⇓ or ⇓ to select frequencies where the conversion loss value was recorded in Table 2-12 on page 113.

18.Use the spectrum analyzer front panel keys to enter the conversion loss values recorded for the frequency.

16. YIG-Tuned Filter/Mixer (RYTHM) Adjustment

Assembly Adjusted

A14 frequency control assembly

Related Performance Tests

Image, Multiple, and Out-of-Band Responses Second Harmonic Distortion Frequency Response

Description

The slope and offset of the A10 RYTHM tuning voltage are set by DACs on the A14 frequency control assembly. The offset DAC value is optimized at a low frequency and the slope DAC value is optimized at a high frequency.

Automated Procedure Available

The YIG-Tuned Filter/Mixer adjustment is included in the automated 8562E "Front End Cal" adjustment, which is described in Chapter 3 , "Frequency Response Adjustment Software."

Figure 2-25   RYTHM Adjustment Setup
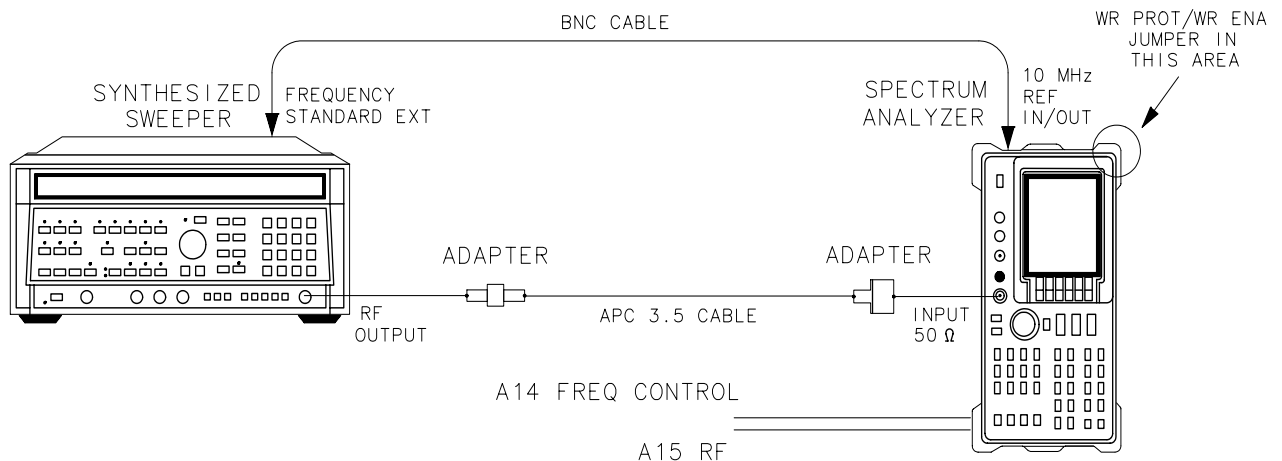
sk121

Equipment

Synthesized sweeper 8340A/B

Adapters

Type N (m) to APC 3.5 (f) 1250-1744

Type APC 3.5 (f) to APC 3.5 (f) 5061-5311

Cables

APC 3.5, 91 cm (36 in) 8120-4921

Procedure

1. Set the 8562E/EC **LINE** switch to off and disconnect the line cord. Remove the spectrum analyzer cover, fold down the A14 and A15 board assemblies, and connect the line cord. Connect the equipment as illustrated in Figure 2-25 on page 115. Press **LINE** to turn the spectrum analyzer on.

2. Move the WR PROT/WR ENA jumper on the A2 controller assembly to the WR ENA position. The jumper is on the edge of the A2 board assembly and can be moved without folding the board down.

3. Press **PRESET** on the 8562E/EC and set the controls as follows:

   Center frequency .... 4.0 GHz
   Span .... 0 Hz

4. On the 8562E/EC, press **CAL**, **IF ADJ ON OFF** so OFF is underlined, **MORE 1OF 2**, **SERVICE CAL DATA**, **PRESEL ADJ**, then **PRESET ALL DACS**.

5. Press **INSTR PRESET** on the 8340A and set the controls as follows:

   CW .... 4.0 GHz
   Power level .... −10 dBm
   Frequency standard switch (rear panel) .... EXT

6. Press **PRESEL OFFSET** on the 8562E/EC. Use the front-panel knob to peak the displayed trace. Record the offset DAC value below:

   Offset at 4.0 GHz = _____

7. Set the 8562E/EC center frequency and the 8340A **CW** to 12.16 GHz.

8. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **PRESEL ADJ**, then **PRESEL OFFSET**. Key in the offset value noted in step 6.

9. Press **PRESEL SLOPE** on the 8562E/EC. Use the front-panel knob to peak the displayed trace. Record the slope DAC value below:

   Slope at 12.16 GHz = _____

10. Set the 8562E/EC center frequency and the 8340A **CW** to 4.0 GHz.

11. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **PRESEL ADJ**, then **PRESEL SLOPE**. Key in the slope value noted in step 9.

12. Repeat steps 6 through 11 until both SLOPE and OFFSET are peaked. Adjust the OFFSET only at 4.0 GHz and the SLOPE only at 12.16 GHz.

13. Press **PRESEL OFFSET**. Press ⇓ to display OFFSET FOR BAND #2. Key in the offset value recorded in step 6.

14. Press **PREV MENU**, **STORE DATA**, and **YES**.

15. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR PROT position.

16. On the 8562E/EC, press **RECALL**, **MORE 1 OF 2**, **FACTORY PRSEL PK**, **SAVE**, then **SAVE PRESEL PK**.

17. 16 MHz PLL Adjustment

Assembly Adjusted

A2 controller assembly

Related Performance Tests

Sweep Time Accuracy Gate Delay Accuracy and Gate Length Accuracy
Delayed Sweep Accuracy Fast Sweep Time Accuracy (Option 007)

Description

The 16 MHz CPU clock is phase locked to the 10 MHz reference. The
output of the 16 MHz PLL loop integrator is adjusted for a clock
frequency of approximately 14.4 MHz with the loop unlocked. This
ensures that the CPU will still function and the display annotation will
be distorted but readable, even if the 10 MHz reference to A2 is absent.

NOTE   If necessary, perform the display adjustments after performing the
following adjustment.

Figure 2-26   **16 MHz PLL Adjustment Setup**
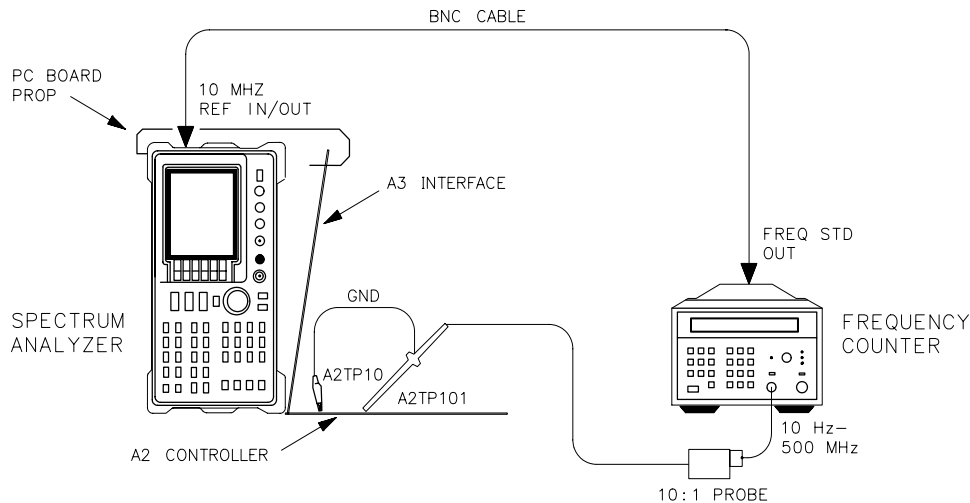
sj140e

Equipment

Microwave frequency counter 5343A

10:1 probe 10432A

Procedure

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and fold out the A2 controller and A3 interface assemblies. Use a pc board prop to hold up the A3 interface assembly, as shown in Figure 2-26 on page 118.

2. Connect the equipment as shown if Figure 2-26 on page 118. The ground lead of the 10:1 probe connects to A2TP10, and the probe tip connects to A2TP101.

3. The 16 MHz PLL adjustment location is shown in Figure 2-27 on page 120.

Figure 2-27   16 MHz PLL Adjustment Location
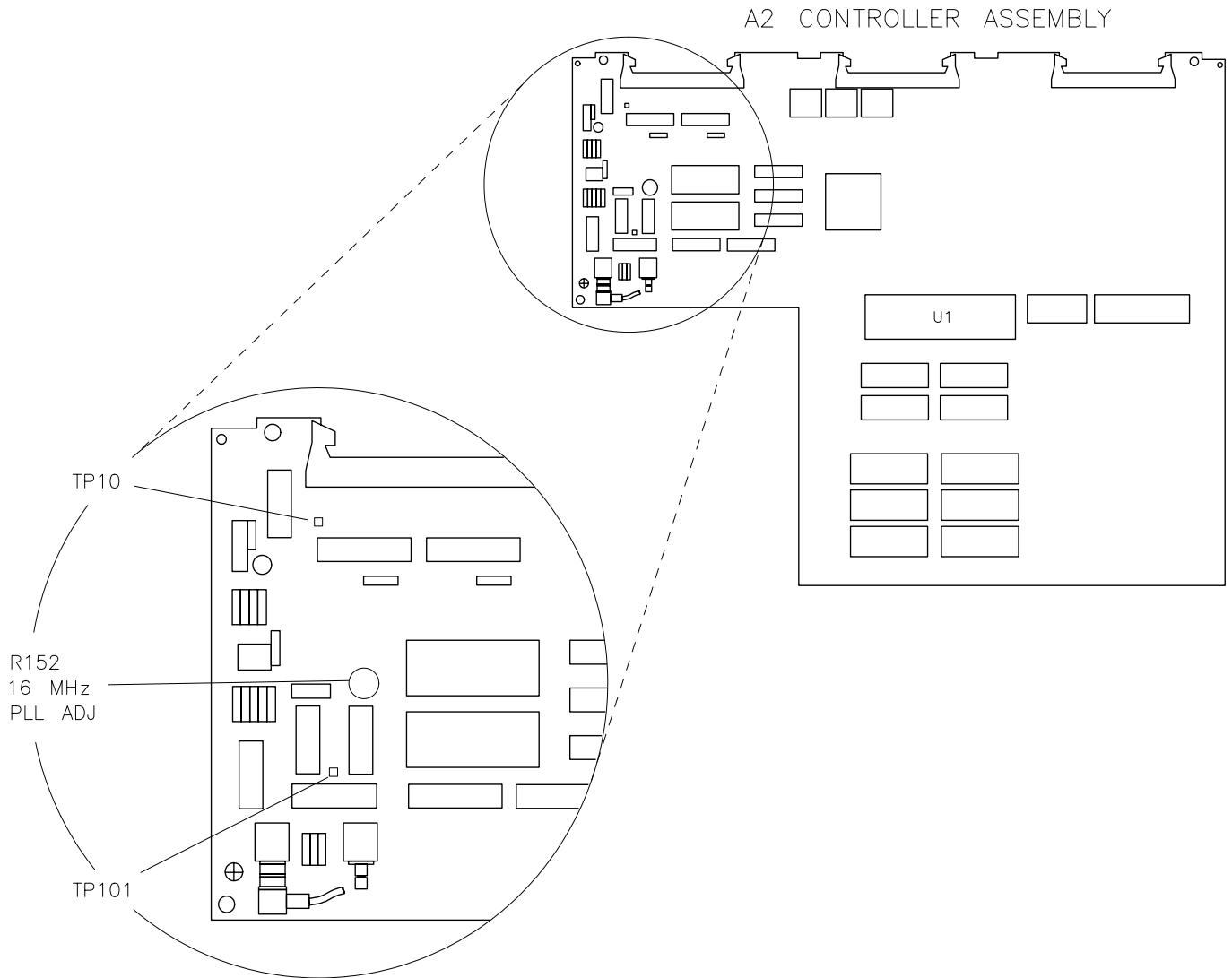
4. Press **LINE** to turn the spectrum analyzer on. Wait until the spectrum analyzer power-on adjustments have completed.

5. Set the microwave frequency counter as follows:

    Sample rate ....Fully counterclockwise
    10 Hz — 500 MHz/500 MHz — 26.5 GHz switch... 10 Hz — 500 MHz
    50 Ω/1 MΩ switch ....1 MΩ

6. On the spectrum analyzer, press **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT**.

7. Disconnect W22 (10 MHz frequency counter) from A2J8. The display will probably appear distorted and error messages may appear. Ignore the error messages.

8. Adjust A2R152 (16 MHz PLL ADJ) until the microwave frequency counter reads 14.4 MHz ±200 KHz.

9. Reconnect W22 to A2J8. The microwave frequency counter should read 16 MHz. If the counter reads 16 MHz and the display is still distorted, perform the display adjustments in "2. Display Adjustment (8562E)" on page 62.

10. On the spectrum analyzer, press **CAL**, **REALIGN LO and IF** to clear any error messages.

18. 600 MHz Reference Adjustment

Assembly Adjusted

A15 RF assembly

Related Performance Test

There is no related performance test for this adjustment.

Description

The 100 MHz VCXO and the tripler are adjusted for a maximum signal level at 600 MHz. A spectrum analyzer is used to monitor the amplitude of the 600 MHz signal while performing these adjustments.

Equipment

Spectrum analyzer 8566A/B

Procedure

1. Press **LINE** to turn the spectrum analyzer off, disconnect the power cord, and remove the spectrum analyzer cover. Fold down the A15 RF and A14 frequency control assemblies. Prop up the A14 frequency control assembly.

2. Disconnect W33, gray/brown coax cable, from A15J701.

3. Connect the signal at A15J701 to the input of the 8566A/B spectrum analyzer.

4. Reconnect the power cord and press **LINE** to turn the spectrum analyzer on.

5. Set the center frequency of the 8566A/B to 600 MHz and set the frequency span and resolution bandwidth of the 8566A/B for the best display of the 600 MHz signal.

6. Set the peak of the 600 MHz signal near the top graticule line on the 8566A/B display and set to 1 dB per division.

7. Adjust A15 C750, VCXO Adjust, for maximum amplitude.

8. Adjust A15 C751 Tripler Adjust, for maximum amplitude. The level, after proper adjustment, should be between –3 and +4.8 dBm (typically 0 to +1 dBm).

9. Reconnect W33 to A15J701.

2a Adjustment Procedures: 3335A Source Not Available

What You'll Find in This Chapter

This chapter provides alternative procedures for the adjustment of the spectrum analyzer that do not require the use of the 3335A Synthesizer Level Generator. The 3335A has been obsoleted. Because of the unavailability of the 3335A, new adjustment procedures are required that use different signal sources. If the 3335A is not available, substitute these procedures for those of the same number found in Chapter 2 , "Adjustment Procedures."

Required Test Equipment

The following table lists the test equipment required to execute the adjustments in this chapter. These adjustments originally required the use of the 3335A Synthesizer Level Generator.

Table 2a-1   **Recommended Test Equipment**

Instrument	Critical Specifications for Equipment Substitution	Recommended Model
Sources		
Synthesized Signal Generator	Frequency range: 250 kHz to 3 GHz Frequency resolution: 1 Hz Attenuator resolution: 0.02 dB Level accuracy: ±0.5 dB External 10 MHz Ref. Input	E4421B or E4422B, E4432B E4433B
Cables		
Cable, 50 Ω coaxial *(four required)*	Connectors: BNC (m) Length: ≥ 122 cm (48 in.)	10503A
Cable	Test Cable	85680-60043
Adapters		
Adapter *(four required)*	Type N (m)-to-BNC (f)	1250-1476
Adapter *(Option 026 only)*	APC-3.5 (f) to APC-3.5 (f)	5061-5311
Adapter *(Option 026 only)*	APC-3.5 (f) to BNC-3.5 (f)	1250-1200

4a. IF Amplitude Adjustments

The IF amplitude adjustments consist of the cal oscillator amplitude adjustment and the reference 15 dB attenuator adjustment.

Assembly Adjusted

A4 log amp/cal oscillator A5 IF assembly

Related Performance Tests

IF Gain Uncertainty Scale Fidelity

Description

This adjustment sets the output amplitude of the A4 log amp/cal oscillator and the absolute amplitude of the reference 15 dB attenuator.

The output of the A4 log amp/cal oscillator is adjusted so that a –55 dBm signal applied to the 10.7 MHz IF input on the A5 IF assembly (A5J3) causes a displayed signal of –60 dBm. The effect of this adjustment is visible only after the **ADJ CURR IF STATE** sequence is complete. **ADJ CURR IF STATE** causes the IF gain adjustment to use the "new" output amplitude from the A4 log amp/cal oscillator.

This procedure also sets the attenuator of the reference 15 dB attenuator so that a source amplitude change of 50 dB combined with a spectrum analyzer reference level change of 50 dB displays an amplitude difference of 50 dB.

Figure 2a-1 IF Amplitude Adjustment Setup
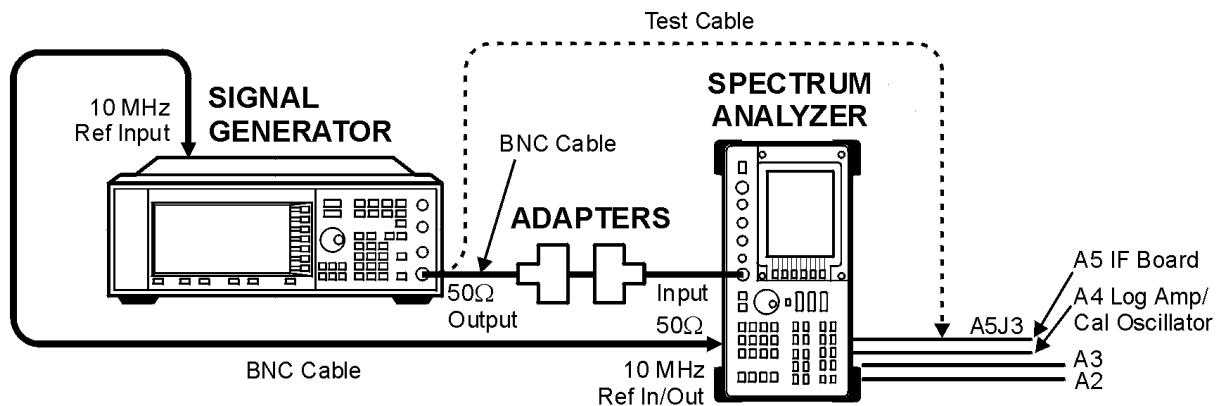
hj11e

Equipment

Signal Generator E4421B

Adapters

Type N (m) to BNC (f) 1250-1476

Cables

BNC, 122 cm (48 in) 10503A

Test cable 85680-60093

Figure 2a-2 IF Amplitude Adjustment Locations
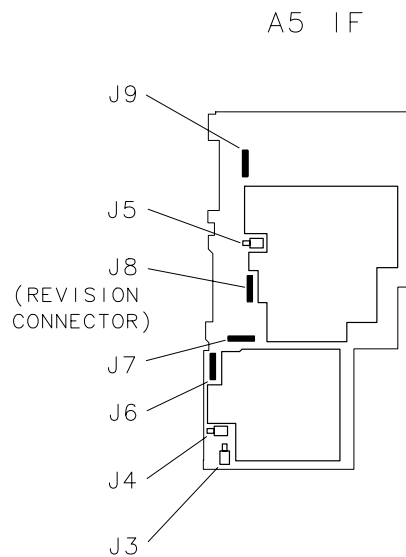
NOTE   The 15 dB reference attenuator adjustment is preset at the factory and
              need not be done if the entire A5 IF assembly is replaced.

Procedure

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in Figure 2a-1 on page 126.

2. Disconnect W29, violet coax cable, from A5J3. Connect the test cable between A5J3 and the RF output of the E4421B. Press **LINE** to turn the spectrum analyzer on.

3. Set the spectrum analyzer controls as follows:

   Center Frequency . . . . 10.7 MHz

   Span . . . . .200 kHz

   Reference Level . . . .–60 dBm

   Attenuator . . . . .0 dB

   dB/division . . . . .1 dB/DIV

   Resolution bandwidth. . . . . .300 kHz

   Video bandwidth . . . . .100 Hz

4. On the spectrum analyzer, press **MKR**, **CAL**, and **IF ADJ ON OFF** so OFF is underlined.

5. Set the E4421B controls as follows:

   Frequency . . . . 10.7 MHz

   Amplitude . . . .–55 dBm

   Mod On/Off . . . . Off

6. Note the marker value. Ideally it should read –60 dBm ±0.1 dB.

7. If the marker reads less than –60.1 dBm, rotate A4R826 CAL OSC AMPTD one-third turn clockwise for every 0.1 dB less than –60 dBm. See Figure 2a-2 for the location of A4R826. A change in the displayed amplitude will not be seen until **ADJ CURR IF STATE** is pressed.

8. If the marker reads greater than –59.9 dBm, rotate A4R826 CAL OSC AMPTD one-third turn counter clockwise for every 0.1 dB greater than –60 dBm. See Figure 2a-2 for the location of A4R826. A change in the displayed amplitude will not be seen until **ADJ CURR IF STATE** is pressed.

NOTE   If A4R826 has inadequate range, refer to "Inadequate CAL OSC AMPTD Range" on page 477.

9. On the spectrum analyzer, press **ADJ CURR IF STATE**. After allowing the analyzer time to complete the adjustments, the displayed amplitude and marker reading should change.

10. Repeat step 7 and step 9 until the marker reads –60 dBm ±0.1 dB.

11. Disconnect the test cable from A5J3 and reconnect W29 to A5J3.

A5 Reference Attenuator Adjustment

1. Set the spectrum analyzer reference level to –60 dBm. If markers are displayed, press **MKR** and **MARKERS OFF**.

2. Set the E4421B **Amplitude** to –60 dBm.

3. Connect a BNC cable between the RF output of the E4421B and the spectrum analyzer INPUT 50Ω .

4. On the spectrum analyzer, press **CAL** and **REF LVL ADJ**. Use the front panel knob or step keys to place the peak of the displayed signal 3 dB to 5 dB below the reference level.

5. Press **PEAK SEARCH** and **MARKER DELTA** on the spectrum analyzer. Set the spectrum analyzer reference level to –10 dBm.

6. Change the 4421B **Amplitude** to –10 dBm.

7. On the spectrum analyzer, press **CAL**.

8. Note the ΔMKR amplitude. Ideally, it should read 50.00 dB ±0.1 dB.

9. If the ΔMKR amplitude is less than 49.9 dB, rotate A5R343 15 dB ATTEN one-half turn counterclockwise for each 0.1 dB less than 50.00 dB. Do not adjust A5R343 more than five turns before continuing with the next step.

10. If the ΔMKR amplitude is greater than 50.1 dB, rotate A5R343 15 dB ATTEN one-half turn clockwise for each 0.1 dB greater than 50.00 dB. Do not adjust A5R343 more than five turns before continuing with the next step.

11. On the spectrum analyzer, press **ADJ CURR IF STATE**. Note the ΔMKR amplitude reading.

12. Repeat step 1 through step 11 until the ΔMKR amplitude reading is 50.00 dB ±0.1 dB.

A5 Adjustment Verification

1. On the spectrum analyzer, disconnect W29 from A5J3. Connect the test cable between A5J3 and the RF output of the E4421B.

2. Set the spectrum analyzer reference level to −10 dBm.

3. Set the E4421B **Amplitude** to −5 dBm.

4. On the spectrum analyzer, press **MKR** and **MARKER NORMAL**.

5. The MARKER amplitude should read −10 dBm ±0.13 dB. If the reading is outside of this range, repeat through .

6. On the spectrum analyzer, reconnect W29 to A5J3. Press **PRESET** and set the controls as follows:

   Center frequency . . . . 300 MHz

   Span . . . . .0 Hz

   Reference level . . . .−10 dBm

   Resolution bandwidth . . . . .300 kHz

7. Connect a BNC cable between the 8563E CAL OUTPUT and INPUT 50Ω .

8. On the spectrum analyzer, press **MKR CAL** and **REF LVL ADJ**.

9. Use the knob or step keys to adjust the REF LEVEL CAL setting until the MKR reads −10.00 dBm ±0.1 dB.

10. On the spectrum analyzer, press **STORE REF LVL**.

5a. DC Log Amplifier Adjustments

There are three DC log adjustments; limiter phase, linear fidelity, and log fidelity.

Assembly Adjusted

A4 log amp/cal oscillator

Related Performance Tests

IF Gain Uncertainty Scale Fidelity

Description

These three adjustment need only be done under the following conditions:

Limiter phase	Only if a repair is made to blocks F, G, H, I, or J.
Linear fidelity	Only if a repair is made to blocks C, D, F, G, H, I, J, K, O, IF gain accuracy, RBW switching, or log fidelity.
Log fidelity	Only if a repair is made to blocks D, F, H, K, IF gain accuracy, RBW switching, or log fidelity.

If multiple adjustments are required they should be done in the following order:

1. Limiter Phase

2. Linear Fidelity

3. Log Fidelity

Figure 2a-3 DC Log Adjustment Setup
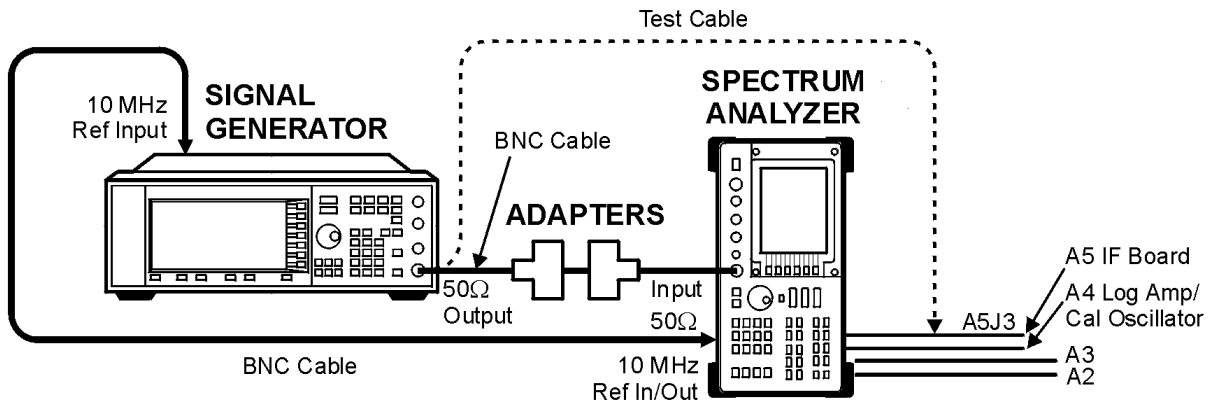
hj11e

Equipment

Signal Generator E4421B

Adapters

Type N (m) to BNC (f) 1250-1476

Type N (f) to 2.4 mm (f) 11903B

Cables

BNC, 122 cm (48 in) 10503A

Test cable 85680-60093

Figure 2a-4 DC Log Adjustment Locations
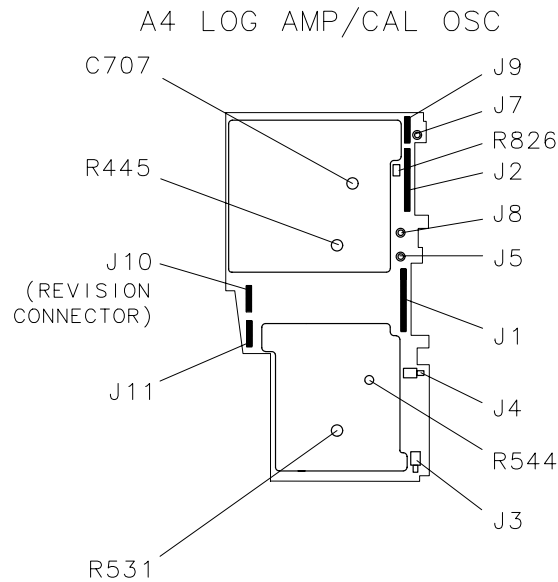
NOTE   Adjustments should be made with all of the shields on and only after allowing at least a 20 minute warm-up.

A4 Limiter Phase Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in . See for adjustment location.

2. Connect the E4421B RF output to the spectrum analyzer 50Ω input. Press **LINE** to turn the spectrum analyzer on.

3. Set the spectrum analyzer controls as follows:

   Center frequency . . . . 15 MHz

   Span . . . . 0 MHz

   Reference level . . . . −10 dBm

   dB/division . . . . 1 dB/DIV

   Resolution bandwidth . . . . 300 kHz

   IF ADJ . . . . OFF

4. Set up an E4421B as follows:

Frequency . . . . 15 MHz

Amplitude . . . .–18 dBm

Mod On/Off . . . . Off

5. Press **CAL**, **ADJ CURR IF STATE**, wait for the analyzer to complete adjustments then press **MKR**.

6. Adjust A4R445 for maximum on-screen amplitude. Refer to Figure 2a-4 on page 133 for the location of A4R445.

A4 Linear Fidelity Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in Figure 2a-3 on page 132. See Figure 2a-4 on page 133 for adjustment location.

2. Connect the E4421B RF output to the spectrum analyzer 50Ω input. Press **LINE** to turn the spectrum analyzer on.

3. On the spectrum analyzer, press **PRESET AMPLITUDE**, **LINEAR**, **MORE 1 of 3**, **AMPTD UNITS**, **dBm**, **CAL**, and **IF ADJ ON OFF** (OFF).

4. Set the spectrum analyzer controls as follows:

Center frequency. . . . . 15 MHz

Span. . . . . 5 MHz

Resolution bandwidth. . . . . .300 kHz

Reference level. . . . .–10 dBm

5. Set up an E4421B as follows:

Frequency . . . . 15 MHz

Amplitude . . . .–10 dBm

Mod On/Off . . . . Off

6. On the spectrum analyzer, press **PEAK SEARCH** and **MARKER DELTA**.

7. Reduce the E4421B input power to –58 dBm.

8. If the delta marker amplitude reads –40 dB ±2 dB, no adjustment is necessary.

9. If the signal is lower on the screen than expected (delta marker amplitude reads less than –42dB) then adjust A4R544 (see Figure 2a-4 on page 133) for an even lower level and press **CAL** and **ADJ CURR IF STATE**. Allow sufficient time for the analyzer to complete the adjustment.

10. If the signal is higher than expected (delta marker amplitude reads greater than –38 dB) then adjust A4R544 for an even higher level signal and press **CAL** and **ADJ CURR IF STATE**. Allow sufficient time for the analyzer to complete the adjustment.

11. Repeat step 7 through step 10.

A4 LOG Fidelity Adjustment

1. Press **LINE** to turn the spectrum analyzer off. Remove the spectrum analyzer cover and place the spectrum analyzer in the service position as illustrated in Figure 2a-3 on page 132. See Figure 2a-4 on page 133 for adjustment location.

2. Connect the E4421B RF output to the spectrum analyzer 50Ω input. Press **LINE** to turn the spectrum analyzer on.

3. On the spectrum analyzer, press **PRESET**, **CAL**, **IF ADJ ON OFF** (OFF), and **ADJ CURR IF STATE**.

4. Set the spectrum analyzer controls as follows:

   Center frequency . . . . 15 MHz

   Span . . . . 0 MHz

   Resolution bandwidth . . . . 300 kHz

   Reference level . . . . –10 dBm

5. Set up an E4421B as follows:

   Frequency . . . . 15 MHz

   Amplitude . . . . –10 dBm

   Mod On/Off . . . . Off

6. On the spectrum analyzer, press **MKR** and **MARKER DELTA**.

7. Decrease the E4421B power to –26 dBm.

8. Calculate the error:

$$\text{Error} \ = \ \text{delta marker reading} - 16 \text{ dB}$$

9. If the error is less than ±0.2 dB, no adjustment is necessary.

10. Set the E4421 power to –10 dBm.

11. Adjust A4R531 (see Figure 2a-4 on page 133) to read two times the error. For example, if the calculated error is +0.75 dB, adjust A4R531 for a delta marker amplitude reading of +1.5 dB. Press **CAL** and **ADJ CURR IF STATE**.

12. Repeat step 7 through step 11.

3 Frequency Response Adjustment Software

Introduction

This chapter describes how to load and run the frequency response adjustment software, which can be downloaded from www.agilent.com/find/8560_software. This software actually automates two manual adjustments: Frequency Response Adjustment, and YIG-Tuned Filter/Mixer (RYTHM) Adjustment. The automated test software is designed to adjust the flatness and preselector of the spectrum analyzer in a minimum amount of time. The frequency response adjustment software automates the most tedious spectrum analyzer adjustment; the adjustment would take over two hours if done manually. The software can allow the adjustment to be performed in less than 20 minutes. The frequency response adjustment requires making several measurements at more than 120 different frequencies over the spectrum analyzer frequency range.

Getting Started

First, make sure you have a compatible controller (computer), and the proper test equipment. The following paragraphs describe requirements for controllers and test equipment. Once the proper equipment is identified, proceed to "Equipment Connections" on page 141.

Spectrum Analyzers

The 8562E Frequency Response Adjustment software is only for 8562E and 8562EC spectrum analyzers. Errors will occur if this software is used to adjust spectrum analyzers other than the 8562E or 8562EC. The 85629B Test and Adjustment Module (TAM) is recommended for automated frequency response adjustments of the 8560E/EC, 8561E/EC, and 8563E/EC. The 8564E/8565E Adjustment/Diagnostic Software is required to adjust the frequency response of the 8564E/EC and 8565E/EC spectrum analyzers.

Controller (Computer)

Frequency Response Adjustment software requires using any combination of one of the following HP controllers and the HP BASIC operating system:

Controller

HP 9000 model 216

HP 9000 model 236

HP 9000 model 310

Operating System

HP BASIC 2.0 with
extensions 2.1

HP BASIC 3.0 and required
BIN files

HP BASIC 4.0 and required
BIN files

Other HP 9000 Series 300 controllers are compatible with the Frequency Response Adjustment software; however, graph printouts might not be full width. This is especially true with medium- and high-resolution displays.

The Frequency Response Adjustment program requires at least 1 MB of free memory. The computer can have either single or dual GPIB ports. Refer to "Dual-Bus Operation" on page 147 for information on using the program with dual GPIB ports.

Test Equipment

Table 3-1 on page 140 summarizes the equipment required to run the Frequency Response Adjustment procedure. The adjustment can use various model numbers of a particular equipment type. Information about selecting the equipment model number you want to use is provided in "Setting GPIB Addresses" on page 145.

NOTE	The validity of the Frequency Response Adjustment depends in part on required test equipment measurement accuracy. Verify proper calibration of test equipment before adjusting the analyzer with the software.

Warm-up Time

Test Equipment Warm-up

Allow sufficient warm-up time for test equipment. Refer to their individual operating and service manuals for warm-up specifications.

Spectrum Analyzer Warm-up

Warm the spectrum analyzer up for at least fifteen minutes before performing the first adjustment.

Table 3-1   **Required Test Equipment Summary**

Type of Equipment	Model Number
Controller*	HP 9000 model 216 (9816), or HP 9000 model 236 (9836), or HP 9000 model 310
Synthesized sweeper (10 MHz to 13.2 GHz)	8340A/B, or 83640A, or 83650A
Measuring receiver	8902A
Power meter	436A or 438A (alternate)
Power sensor (10 MHz to 18 GHz)	8481A, or 8485A
Power splitter (dc to 18 GHz)	11667A, or 11667B
Miscellaneous cables and adapters	As per test setup
* 1 Megabyte of free memory is required for the test program.	

Equipment Connections

Computer (Controller) Setup

For HP 9000 model 216 or model 236 computers, setup instructions are provided in Chapter 1, "Computer Installation," of the *BASIC Operating Manual*. For HP 9000 model 310 computers, setup information is provided in *Configuration Reference Manual* for Series 300 computers.

GPIB Cables

All test equipment controlled by GPIB should be connected to the internal GPIB of the controller (select code 7). If the controller has only one GPIB connector, connect the spectrum analyzer to it as well. If the controller has dual GPIB connectors, connect the spectrum analyzer under test to the second GPIB (typically, select code 8).

10 MHz Reference

The 10 MHz REF IN/OUT on the spectrum analyzer under test should be connected to the synthesized sweeper 10 MHz Reference Output. That is, it should be connected to the 10 MHz REF OUTPUT of the 8340A/B, 83640A or 83650A.

Adjustment Setups

Adjustment setups are included with each adjustment. These are in "Adjustment Setups" on page 141. The program prompts the operator to make appropriate equipment connections if the correct equipment setup is not detected.

Using Frequency Response Adjustment Software

Loading the Program

Load HP BASIC into the computer. HP BASIC choices are:

BASIC 2.0 and extensions 2.1

BASIC 3.0 or 4.0, which must include the following binaries:

MAT
IO
GRAPH
GRAPHX
PDEV
GPIB
MS
CLOCK
CS80
DISC
KBD

For configuration instructions, refer to the *BASIC Operating Manual*. Download the 8562E/EC Frequency Response Adjustment software from www.agilent.com/find/8560_software.

Once the software is on a drive accessible by the test computer, type:

```
LOAD "FR_END8562",1
```

Press **EXECUTE** on HP 9000 Series 200 computers, or **RETURN** on HP 9000 Series 300 computers, to load the software and start the program running.

Program Operation

The frequency response adjustment consists of three menus. They are the Conditions Menu, the Adjust Menu, and the Sensor Utilities Menu, which are accessed from the Conditions Menu. Program operation is controlled through a combination of softkeys and user prompts. Some prompts, primarily in the Conditions and Sensor Utilities Menus, require computer keyboard entries. Terminate keyboard entries with the **RETURN** or **ENTER** key. Most prompts, however, tell the user what to do next or provide informational messages.

If the message `(any key)` follows a prompt, pressing any key on the keyboard continues the program. If the message `(any key or `Q' to quit)` follows a prompt, pressing any key except `Q` continues the program. Pressing `Q` terminates the current procedure at the next, most logical point in the program.

Conditions Menu

The first menu screen displayed is the Conditions Menu. The pointer displayed along the left edge of the screen may be moved with the knob (if one is present) or the up (⇓) and down (⇓) arrow keys. Notice that the menu has two pages. Moving the pointer below the last entry on the page brings up the next page. Similarly, moving the pointer above the first entry on a subsequent page brings up the preceding page.

Test Record Header Information

The information in the first six entries of this menu is for the user's information only; it is not printed or saved with any data. The spectrum analyzer model number and serial number are stored in the analyzer memory. The program queries these numbers via GPIB and displays them. If the spectrum analyzer under test does not respond at the address listed under GPIB Addresses, or no address is listed, a message appears where the model and serial numbers are normally displayed.

The program also queries the time and date in the computer. If an HP 9000 Series 200 computer is used, it might be necessary to reset the time and date; HP 9000 Series 300 computers have built-in real-time clocks.

Entries for Operator, Test Conditions, and Other Comments are optional. To make or to change an entry, move the pointer to the line where the entry is to be made or changed. Press **Change Entry** and type in your new entry. Entries for Operator, Test Conditions, and Other Comments can be up to 37 characters long, but only the first 25 characters of the Operator entry are printed on the test record.

System Mass Storage File Location

Calibration factor data for different power sensors and a customized set of conditions may be stored on disk. The mass storage unit specifier (msus) for the disk containing this information should be entered as the system mass storage file location. Refer to the *BASIC Operating Techniques Manual* for information on the syntax of the msus. The software allows a system mass storage file location with more than 37 characters though only the first and last 17 characters will be displayed.

Power Sensors

The frequency response adjustment program supports two models of power sensors, but only one model is necessary to run all the tests. The 8481A is the preferred sensor. The 8485A may be substituted if it has calibration factor data from 10 MHz to at least 18 GHz (the 8485A comes standard with data down to only 50 MHz). Refer to "Sensor Utilities Menu" on page 147 for more information regarding storing, viewing, editing, and purging cal factor data for power sensors.

To select a particular sensor of a certain model number, move the pointer to the desired model number and press **Change Entry**. Enter the last five digits of the power sensor serial number (that is, the serial number suffix). The program checks to see that a data file containing the cal factor data for that particular sensor exists.

To create, edit, view, or purge power sensor cal factor data files, press **Sensor Utils** to bring up the Sensor Utilities Menu. Refer to "Sensor Utilities Menu" on page 147 for more information.

A `WARNING` message appears if the program does not find a data file for the sensor. If this occurs, check that the system mass storage file location specifies the disk where the power sensor data resides. If the system mass storage file location is correct, the cal factor data for that particular sensor has not been stored.

NOTE

Power sensor data files created using the `VERIFY_6XE` operation verification software (for 8560E/61E/62E/63E/64E/65E spectrum analyzers) are compatible with the frequency response adjustment software.

Refer to "Sensor Utilities Menu" on page 147 for additional information.

Setting GPIB Addresses

The last seven lines of the Conditions Menu are for selecting the GPIB addresses of test equipment used for the Operation Verification program. It is not necessary to use all the test equipment listed. Some model numbers listed are "alternates." Table 3-1 on page 140 lists the test equipment required, and alternates.

Entering zero as the test equipment address results in that model number being unavailable in the program (`NA` is displayed in the address field). To minimize possible confusion later, enter a zero for the address of each piece of test equipment that is not available.

Enter the address for each piece of test equipment that is available, including the spectrum analyzer under test. Addresses must contain the select code of the bus to which the equipment is connected followed by the equipment address on that bus. For example, if the 8902A is at address 14 on a bus with a select code of 7, enter an address of 714. If the 8902A were on a bus with a select code of 12, you should enter an address of 1214.

A question mark (?) next to a GPIB address indicates the address has not been checked to verify a response. An asterisk (*) next to a GPIB address indicates the address was checked and that an instrument responds at that address. If there is neither an asterisk nor a question mark next to an address, the address has been checked and no response was detected.

Storing and Loading the Conditions File

The information in the Conditions Menu may be stored for future use by pressing **Store Conds**. A file named CONDITIONS is created on the disk specified by the system mass storage file location.

NOTE

CONDITIONS files used with the operation verification software for either the 8560 A/B-Series spectrum analyzers, or the 8560 E-Series spectrum analyzers are *not* compatible with the frequency response adjustment software. If the software is stored on an HFS-formatted hard drive, the frequency response adjustment software and operation verification software should be in separate directories.

When running the frequency response adjustment program in the future, set the system mass storage file location to read the disk where the CONDITIONS file is located and press **Load Conds**. If the CONDITIONS file resides on the default system mass storage file location, the CONDITIONS file is loaded automatically the next time the program is run.

The default system mass storage file location is `:,700,1`. For the HP 9000 Model 236 (9836), it is necessary to use an external disk drive. The disk drive must support double-sided format.

Getting to the Adjust Menu

Once all necessary items in the Conditions Menu are selected, you can run an adjustment by pressing **Adjust Menu**. Before the Adjust Menu is displayed, these things occur:

- Appropriate power sensor data files are loaded.

- GPIB is checked for a response at each address.

- Serial and model number of the spectrum analyzer under test are queried.

Refer to for more details on running the adjustments.

Verifying the GPIB

To see which test equipment responds on GPIB, press **Verify Bus**. This check only verifies that there is a response at the address listed; it cannot tell that a particular piece of equipment is at a particular address. This is useful for verifying GPIB connections without entering the Adjust Menu.

Querying the Spectrum Analyzer Serial Number

The frequency response adjustment program automatically queries the spectrum analyzer serial and model number on three occasions: at program initiation, when loading the CONDITIONS file, and when entering the Adjust Menu. To query the analyzer serial and model numbers at any other time, press **Query DUT S/N**. This is helpful for adjusting multiple spectrum analyzers; you do not have to reload the CONDITIONS file or restart the program.

Exiting Frequency Response Adjustment

Press **Exit Program** to exit the frequency response adjustment program.

Dual-Bus Operation

The frequency response adjustment program may be used on dual GPIB systems, such as the microwave test set. In these systems, all the test equipment is connected to GPIB at select code 7, and the device under test (for example, the spectrum analyzer) is connected to GPIB at select code 8.

To run this program in a dual-bus configuration, enter equipment addresses as described in "Setting GPIB Addresses" on page 145, making sure that each address properly identifies the bus select code to which it is connected. Program operation is the same for dual-bus and single-bus configuration.

Sensor Utilities Menu

The frequency response adjustment program needs to know the cal factors of each power sensor being used. Create, edit, view, and delete data files containing cal factors for each power sensor in the Sensor Utilities Menu. Power sensor data filenames include the last five digits of the power sensor serial number. For example,

- for 8481A power sensors the filename is SEN81NNNNN

- for 8485A power sensors the filename is SEN85NNNNN

where NNNNN represents the last five digits of the power sensor serial number (the serial number suffix). Note that the first two digits in the filename correspond to the last two digits of the power sensor model number.

All power sensor data files available on the system mass storage location file are listed upon entering the Sensor Utilities Menu.

NOTE   Power sensor data files created using the VERIFY_6XE operation verification software (for 8560E/61E/62E/63E/64E/65E spectrum analyzers) are compatible with the frequency response adjustment software.

Adding a Power Sensor Data File

To add a new power sensor data file, press **Add File**, and enter the power sensor model number as requested. An error message is displayed if a disk at the current system mass storage file location is not found.

When prompted for the power sensor serial number, enter only the last five digits (the serial number suffix). You are then prompted for a cal factor frequency and for the cal factor. These frequency/cal-factor pairs need not be entered in order of increasing frequency; the program inserts the pairs in their proper place. All frequencies should be entered in MHz.

NOTE

To use the 8485A, it must have a calibration factor at 10 MHz. Standard 8485As have calibration factors down to only 50 MHz.

A 50 MHz Cal-Factor must be entered in order to calibrate the power sensor. Some power sensors do not include a 50 MHz Cal-Factor on their chart or calibration record; it is listed as part of the Calibration Procedure on the case of the power sensor.

If a mistake is made entering a cal factor, enter the frequency of the erroneous cal factor at the next frequency prompt. Enter the correct cal factor at the next prompt. If an error was made entering the frequency value, enter the erroneous frequency at the next frequency prompt and a zero for the cal factor to delete that frequency point.

Once all cal factor data for a power sensor is entered, enter an S at the next frequency prompt. The power sensor data is then stored on disk.

Viewing and Editing a Power Sensor Data File

Press **View/Edit** to view or edit a power sensor data file. Only data files listed on the screen can be viewed or edited. If a file is created but data is not stored, the filename is listed, but no data is viewed and it cannot be edited.

To change the cal factor at a particular frequency, enter that frequency at the frequency prompt, then enter the new cal factor.

To delete a frequency/cal factor pair, enter the frequency of the pair to be deleted and a cal factor of zero. Add a frequency/cal factor pair by entering the new frequency at the frequency prompt and the new cal factor.

Deleting a File

Press **Delete File** to remove a listed file. At the prompt, enter the filename exactly as it appears on-screen. You are asked for confirmation to delete the file.

Changing the System Mass Storage File Location

To add, edit, or view power sensor data on a disk other than the one currently specified by the system mass storage file location, press **System File**. Enter the msus of the new system mass storage file location. All power sensor files residing on that disk are listed. When returning to the Conditions Menu, the system mass storage file location is the one determined in the Sensor Utilities Menu.

Listing Available Power Sensor Data Files

Press **List Files** to list all power sensor data files on the currently specified system mass storage location file.

Returning to the Conditions Menu

Press **Cond Menu** to return to the Conditions Menu.

Adjust Menu

The Adjust Menu displays the one adjustment that can be performed by the frequency response adjustment program.

If GPIB controlled equipment for a given adjustment does not respond over GPIB, that adjustment is flagged MISSING ETE (missing electronic test equipment). These adjustments cannot be run.

Equipment connection prompts are displayed on the computer screen. Most adjustments check equipment connections and only prompt the operator if a mis-connection is detected.

NOTE   The Front End Cal adjustment refers to the 8481A or 8485A power sensor as the "Channel B Power Sensor," even if a single-channel power meter (such as an 436A or 8902A) is being used.

If more than one power meter (or the measuring receiver and one of the power meters) is present, the program asks which model to use as the power meter. Enter the model number without the alphabetic character (for example, enter 8902 for an 8902A).

Single Test

Press **Single Test** to run the adjustment indicated by the pointer. Once the adjustment is running, press **Restart** to abort and restart the test.

Calibrate Power Sensor

The frequency response adjustment program keeps track of which power sensor is being used and the elapsed time since it was last calibrated.

The program prompts the user to re-calibrate the power sensor if more than 2 hours elapses since the last calibration. Also, if the power sensor is changed, the new power sensor must be calibrated.

If there is a significant change in ambient temperature, or improved power meter accuracy is desired, it is advisable to re-calibrate the sensor more often than the program requires. Press **Cal Sensor** and follow the instructions on the computer screen to re-calibrate the power sensor.

List Equipment

To obtain a list of required test equipment for running a test, move the pointer to the test, press **List Equip**. All GPIB controlled equipment and passive devices, other than required cables and adapters, are listed. If a test is flagged `MISSING ETE` but all test equipment appears present, press **List Equip** to see what is needed, then return to the Conditions Menu and verify that the equipment is present. Press **Cond Menu** to return to the Conditions Menu from the Test Menu.

Frequency Response Adjustment Menu Softkeys

This section provides a brief description of each menu of softkeys. More detailed information is provided in "Program Operation" on page 143. The softkey order shown below may vary with what appears on the computer display; the order differs depending on whether an HP 9000 Series 200 or Series 300 computer is used.

Conditions Menu

Adjust Menu   displays the Adjust Menu, which allows you to perform an adjustment. Refer to "Adjust Menu" on page 152.

Load Conds   loads the CONDITIONS file from the disk specified by the system mass storage file location.

Sensor Utils   displays the Sensor Utilities Menu, which allows viewing, editing, and adding power sensor data files. Refer to "Sensor Utilities Menu" on page 152.

Change Entry   permits changing a Conditions Menu entry, indicated by the pointer along the left edge of the computer display. Press the **RETURN** or **ENTER** keys to terminate an entry.

Verify Bus   checks each listed GPIB address for response. **Verify Bus** does not verify that a particular piece of equipment is at a specified address.

Query DUT S/N   queries the GPIB for the serial number and model number of the spectrum analyzer under test.

Store Conds   stores the current conditions in the CONDITIONS file on the specified system mass storage file location.

Exit Program   exits the frequency response adjustment program.

Sensor Utilities Menu

View/Edit   allows user to view and edit power sensor data files.

Add File   creates a new power sensor data file.

Delete File   deletes a power sensor data file. User is asked for confirmation before deletion takes place.

List Files   lists all power sensor data files on the disk currently specified by the system mass storage file location.

System File   allows user to change the currently specified system mass storage file location.

Cond Menu   returns you to the Conditions Menu.

Adjust Menu

Single Test   runs the adjustment indicated by the pointer, once.

Cal Sensor   allows you to re-calibrate the current power sensor and resets the internal "time-since-last-calibration" timer.

List Equip   lists the required equipment for the test indicated by the pointer.

Cond Menu   returns to the Conditions Menu.

Front End Cal (YIG-Tuned Filter/Mixer (RYTHM) and Frequency Response Adjustment)

Assemblies Adjusted

A14 Frequency Control Assembly A15 RF Assembly A10 RYTHM

Related Performance Tests

Displayed Average Noise Level Frequency Response Image, Multiple, and Out-of-Band Responses Second Harmonic Distortion

Description

Front End Cal is an automated adjustment that performs the equivalent of two manual adjustment procedures, Frequency Response Adjustment, and YIG-Tuned Filter/Mixer (RYTHM) adjustment. The RYTHM adjustment is performed first, followed by the frequency response adjustment.

The RYTHM adjustment optimizes the settings of the offset and slope DACs on the A14 Frequency Control assembly for maximum amplitude response. The offset DAC value is optimized at a low frequency and the slope DAC value is optimized at a high frequency.

The frequency response adjustment consists of applying a signal of known amplitude at several different frequencies to the spectrum analyzer. At each frequency, the RF GAIN DAC controlling the flatness compensation amplifiers is adjusted to place the displayed signal at the same place on screen. When tuned to a frequency in a preselected band, the preselector is centered before adjusting the RF GAIN DAC.

After both adjustments are done, the preselector slope and offset DAC values, the RF GAIN DAC values, and the preselector peak DAC values are stored in EEROM.

NOTE   Front End Cal refers to the 8481A or 8485A power sensor as the "Channel B Power Sensor," even if a single-channel power meter (such as an 436A or 8902A) is being used.

If an 8485A Power Sensor is used, it must have a calibration factor at 10 MHz. Standard 8485As have calibration factors down to only 50 MHz.

Figure 3-1   **Front End Cal Adjustment Setup**
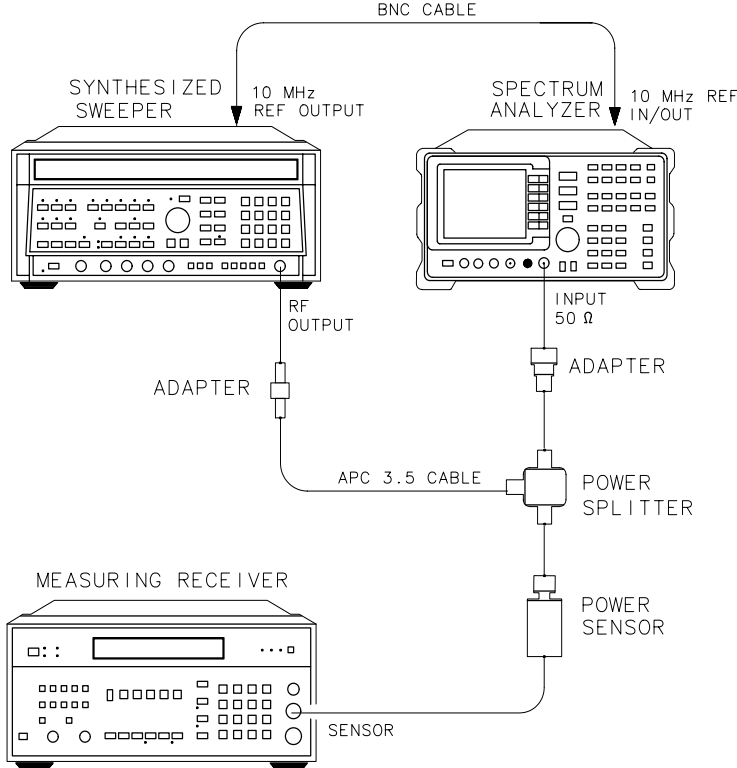
sl132e

Frequency Response Adjustment Error Messages

The frequency response adjustment software displays prompts and error messages on the computer display. Error messages are preceded with ERROR:. For more information on prompts, refer to "Program Operation" on page 143.

The following error messages are listed in three groups: messages beginning with alphabetic characters, those beginning with numeric characters, and others beginning with variables such as filenames or instrument model numbers. If an error message is not found in either of the first two groups, it probably begins with a variable. Refer to the third group that begins with variables. The error message descriptions include recommended corrective action.

Error Messages Beginning with Alphabetic Characters

Address must be from 0 to 30 inclusive

GPIB addresses must be in the range from 0 to 30. Press any key and enter new address in this range.

Cal Factor outside of 0 to 150% range entered

Cal Factor entries must be within this range. Press any key and enter the frequency again. Then enter a Cal Factor in the proper range.

CONDITIONS file from system file location is not compatible! WARNING

CONDITIONS files from Operation Verification programs for the 8560 A/B-Series, or 8560 E-Series analyzers are not compatible with the frequency response adjustment software. Put the frequency response adjustment software in a different directory than the Operation Verification programs, if possible. Default CONDITIONS data will be used. Change the mass storage file location to a different location than either of the operation verification programs. Then, modify the conditions data as necessary and press **STORE CONDS**.

Conditions Menu DUT ID disagrees with responding DUT ID

The model and/or serial number of the spectrum analyzer under test (DUT) listed in Chapter 3 , "Frequency Response Adjustment Software," does not agree with that of the DUT which is responding over GPIB. Press any key and follow the instructions in the next three prompts.

Data not accepted, check entry format

The data just entered was not valid. Press any key and try again, checking for the proper entry format.

DUT doesn't respond at address listed

Program attempted to address the spectrum analyzer under test at the address listed, but the spectrum analyzer did not respond. Check the GPIB connections and the address listed.

File <filename> not found

The filename of the power sensor data file entered could not be found on the currently specified system mass storage file location. Check the filename and the system mass storage file location.

Insufficient equip. to do test <test number> : <test name>

The required GPIB-controlled test equipment for the test indicated is not available. Press any key and choose another test.

No GPIB address listed for DUT

Program attempted to address the spectrum analyzer (DUT), but no GPIB address was listed for it. Press any key and enter an address for the spectrum analyzer.

Non-numeric entry other than S entered, or frequency <=0

When entering a frequency of a frequency/Cal-Factor pair to be added, edited, or deleted, the entry must either be a number greater than 0, or S to store the current data.

No sensor file found for <sensor model> S/N <sensor serial #>

A power sensor data file for the indicated power sensor could not be found on the currently specified system mass storage file location specifier. Check the sensor model and serial numbers and the system mass storage file location.

Power meter reads <value> dBm

The power meter has read a value far exceeding the specification of the CAL OUTPUT amplitude; check that power sensor is connected to CAL OUTPUT and press any key. The power will be read once more and assumed to be valid.

Select code <value> does not currently support GPIB operations

The address just entered specified a select code which is not a GPIB interface. Check the address entered and the select code of the appropriate interface.

Sensor serial number must be from 1 to 99999

The power sensor serial number entered was not in the range indicated. Enter the serial number correctly.

System mass storage file location catalog cannot be read

Program attempted to read the catalog of the system mass storage file location. Check the msus of the system mass storage file location.

This program does not support the current DUT

The frequency response adjustment software supports only the 8562E and 8562EC. Refer to "Spectrum Analyzers" on page 139.

Unable to load CONDITIONS file from listed system file location

Program attempted to load the CONDITIONS file from the listed system mass storage file location. Check the msus of the System mass storage file location and the presence of the CONDITIONS file.

Unable to load data from <sensor filename>

Program found power sensor data file, but could not read the data from the file. Use the Sensor Utilities to delete the file and enter new data.

Unable to obtain catalog from <system mass storage file location>

The system could not verify that the system mass storage file location entered was available. Check the msus of the system mass storage file location.

Unable to reach power level of <value> dBm

Program was unable to set the source amplitude for a desired power meter reading. Check the test setup.

WARNING: CONDITIONS file from system file location is not compatible!

CONDITIONS files from Operation Verification programs for the 8560 A/B-Series, or 8560 E-Series analyzers are not compatible with the frequency response adjustment software. Put the frequency response adjustment software in a different directory than the Operation Verification programs, if possible. Default CONDITIONS data will be used. Change the mass storage file location to a different location than either of the operation verification programs. Then, modify the conditions data as necessary and press **STORE CONDS**.

Error Messages Beginning with Numeric Characters

8481A Sensor cal data minimum frequency not <= 50 MHz

Program requires the 8481A power sensor to have a Cal Factor at or below 50 MHz. Use Sensor Utilities to add a Cal Factor at or below 50 MHz.

8481A Sensor cal data maximum frequency not >= 300 MHz

Program requires the 8481A power sensor to have a Cal Factor at or above 300 MHz. Use Sensor Utilities to add a Cal Factor at or above 300 MHz.

8485A Sensor cal data minimum frequency not = 10 MHz

Program requires the 8485A power sensor to have a Cal Factor at 10 MHz. Use Sensor Utilities to add a Cal Factor at 10 MHz.

8485A Sensor cal data maximum frequency not >= 26.5 GHz

Program requires the 8485A power sensor to have a Cal Factor at or above 26.5 GHz. Use Sensor Utilities to add a Cal Factor at or above 26.5 GHz.

Error Messages Beginning with Variables

<filename> file not found

The file indicated could not be found at the listed system mass storage file location. Check the filename and the system mass storage file location.

<keyboard entry> is a non-numeric entry

The program expected a numeric entry but did not receive one. Enter a numeric entry.

<number of instruments> instruments have GPIB addresses of <GPIB address>

The indicated number of instruments have all been set to the same GPIB address. Review the addresses and eliminate the duplication.

<power meter model number> doesn't read signal to be in –1 +/–5 dBm range

The power meter (or measuring receiver) does not read a power level within the range indicated. Check for loose connections.

<source model number> signal not in +5 +/–5 dBm range

The source indicated was set for +5 dBm output, but the spectrum analyzer measured the amplitude to be outside the ±5 dB range. Check test setup.

<source model number> signal not in –1 +/–5 dBm range

The source indicated was set for + 5 dBm output and the source output is fed through a power splitter to the spectrum analyzer under test. The spectrum analyzer should measure the amplitude to be within 5 dB of –1 dBm (6 dB loss through power splitter). Check test setup.

<source model number> +10 dBm signal not in +10 +/–8 dBm range

The source indicated was set for a +10 dBm output and the source output is fed through a low-pass filter(s) to the spectrum analyzer under test. The spectrum analyzer should measure the amplitude to be within 8 dB of +10 dBm (the filters have some insertion loss). Check test setup.

<source model number> has a cold oven

The 10 MHz reference oven oscillator has not warmed up yet. Allow the oven to warm up.

<source model number> is unlevelled

The source indicated has been programmed for an amplitude which results in an unlevelled condition. Check the test setup for loose connections.

4   Assembly Replacement

Introduction

This chapter describes the removal and replacement of all major assemblies. The following replacement procedures are provided:

Tools required to perform the procedures are listed in Table 4-1 on page 164.

The words *right* and *left* are used throughout the replacement procedures to indicate the side of the spectrum analyzer as viewed from the front panel. See Figure 4-1 on page 165.

Numbers in parentheses are used throughout the replacement procedures to indicate numerical callouts on the figures.

CAUTION	The spectrum analyzer contains static-sensitive components. Read the section entitled, "Electrostatic Discharge" on page 32.

Access to Internal Assemblies

Servicing the 8562E/EC requires the removal of the spectrum analyzer cover assembly and folding down six board assemblies. Four of these assemblies lay flat along the top of the spectrum analyzer and two lay flat along the bottom of the spectrum analyzer. All six assemblies are attached to the right side frame of the spectrum analyzer with hinges and fold out of the spectrum analyzer allowing access to all major assemblies. See Figure 4-1 on page 165.

- To remove the spectrum analyzer cover, refer to "Procedure 1. Spectrum Analyzer Cover" on page 165.

- To access the A2, A3, A4, and A5 assemblies, refer to "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

- To access the A14 and A15 assemblies, refer to "Procedure 9. A14 and A15 Assemblies" on page 217.

- To remove and replace the backlight cables, which illuminate the A18 LCD, refer to "Procedure 2A. A1 Front Frame/A18 LCD (8562EC)" on page 166.

- To remove the A17 LCD assembly in 8562EC instruments, refer to "Procedure 2A. A1 Front Frame/A18 LCD (8562EC)" on page 166.

- To remove the A16 or A17 assembly in 8562E instruments, refer to "Procedure 10. A16 Fast ADC and A17 CRT Driver (8562E)" on page 220.

Cable Color Code

Coaxial cables and wires will be identified in the procedures by reference designation or name followed by a color code. The code is identical to the resistor color code. The first number indicates the base color with second and third numbers indicating any colored stripes. For example, W23, coax 93, indicates a white cable with an orange stripe.

Table 4-1 **Required Tools**

Description	Part Number
5/16-inch open-end wrench	8720-0015
3 mm hex (Allen) wrench	8710-1366
4 mm hex (Allen) wrench	8710-1164
17 mm socket wrench	T362609
No. 4 hex (Allen) wrench	5020-0288
No. 6 hex (Allen) wrench	5020-0289
7 mm nut driver	8710-1217
3/8-inch nut driver	8720-0005
7/16-inch nut driver	8720-0006
9/16-inch nut driver (drilled out, end covered with heatshrink tubing)	8720-0008
Small No. 1 pozidrive screwdriver	8710-0899
Large No. 2 pozidrive screwdriver	8710-0900
T-8 TORX screwdriver	8710-1614
T-10 TORX screwdriver	8710-1623
T-15 TORX screwdriver	8710-1622
Long-nose pliers	8710-0030
Wire cutters	8710-0012

Procedure 1. Spectrum Analyzer Cover

Removal/Replacement

1. Disconnect the line-power cord. Remove any adapters from the front panel connectors and place the spectrum analyzer on its front panel.

2. If an 85620A Mass Memory Module or 85629B Test and Adjustment Module is mounted on the rear panel, remove it. Loosen (but do not remove) the four rear-bumper screws, using a 4 mm hex wrench. Pull the cover assembly off towards the rear of the instrument.

CAUTION   When replacing the spectrum analyzer cover, use caution to avoid damaging any cables.

3. When installing the cover assembly, be sure to locate the cover air vent holes on the bottom side of the spectrum analyzer. Attach with the four screws loosened in step 2, and tighten the four screws gradually to ensure that the cover is seated in the front frame gasket groove.

4. Torque each screw to 40 to 50 inch-pounds to ensure proper gasket compression to minimize EMI.

Figure 4-1   **Hinged Assemblies**
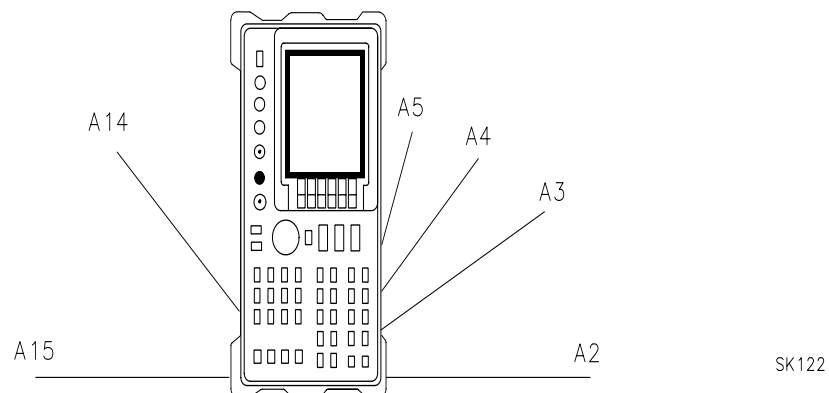
NOTE   Figure 4-1 shows an 8560 E-series instrument. In the assembly removal and replacement procedures the words "left" and "right" assume you are facing the front panel of the instrument, as shown in Figure 4-1 on page 165, with A14 and A15 to your left, and A2 through A5 on your right. The 8560 EC-series instrument is identical except the A2 board is smaller.

Procedure 2A. A1 Front Frame/A18 LCD (8562EC)

Removal of the Front Frame

1. Remove the spectrum analyzer cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165. Place the instrument on its side, with the display section upper-most, as shown in Figure 4-1 on page 165.

2. Fold out the A2, A3, A4, and A5 assemblies as described in steps 2 through 6 under "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188. Facing the front panel, the A2, A3, A4, and A5 assemblies will lay to your left.

3. Fold out the A14 and A15 assemblies as described in steps 3 through 4 under "Procedure 9. A14 and A15 Assemblies" on page 217. Facing the front panel, the A14 and A15 assemblies will lay to your right.

4. Disconnect ribbon cable A1A1W1, which connects HDR1 on the A1 front frame assembly and A3J602 on the A3 interface board.

5. Disconnect the following cables from the A2 controller board:

   a. Ribbon cable W60, which connects J8 on the A2 controller board with J1 on the A17 display driver board.

   b. W61, which connects J9 on the A2 controller board with J7 on the A17 display driver board.

6. Disconnect ribbon cable W64 from the J1 VGA port on the rear panel (do not disconnect W64 from the A17 display driver board).

7. Disconnect the W3 line switch cable from the power supply.

   a. Remove the power supply cover. Use a T-6 TORX driver to remove the 3 screws (0515-2309) that secure the power supply cover to the power supply.

   b. Remove the line switch connector from A6J2 on the power supply.

   c. Loosen FL 1. Remove the two screws (0515-2332) which are used to secure FL 1 to the right side of the chassis.

   d. After FL 1 has been loosened, route the W3 line switch cable through the opening behind FL 1, from the left to the right side of the instrument (if you still have difficulty routing W3 through the opening, use an open ended 5/16-inch wrench to further loosen, or disconnect FL 1).

To disconnect the line switch from the front panel, see "Removal of the Line Switch from the Front Panel" on page 169.

Disconnect the following connectors which are attached to the inside of the A1 front panel assembly:

a. INPUT 50 Ω RF connector. Use a 5/16-inch open-end wrench to disconnect cable W41 from the front panel. Loosen the opposite end of cable W41, which is connected to the attenuator.

b. RF OUT 50 Ω connector *for Option 002 spectrum analyzers.* Use a 5/16-inch wrench to disconnect cable W47 from the front panel.

c. 1ST LO OUTPUT connector. Disconnect cable W42 from A7J3 and from the front panel 1st LO OUTPUT connector.

   To remove the 1st LO OUTPUT connector use a 5/16 socket and thread pliers. Use the pliers to hold the 1st LO connector in place, while loosening the connector inside the instrument with the 5/16-inch socket.

d. 1ST LO OUTPUT connector *For Option 002 spectrum analyzers.* Disconnect W46 from the front panel.

e. IF INPUT connector. Disconnect W36 from the front panel.

8. Remove the following from the face of the front panel:

   a. VOLUME knob. Use a 0.050 Allen wrench to remove the two screws (3030-0007) that secure the volume knob to the face of the front panel. If necessary, use a 5/16-inch nut driver to drill out the nut which secures the VOLUME potentiometer assembly. Cover the tip with heatshrink tubing or tape to avoid scratching the enameled front panel.

   b. CAL OUTPUT connector. Use a 9/16-inch nut driver to remove the dress nut that holds the front panel CAL OUTPUT connector to the front panel. If necessary, drill out the nut driver to fit over the BNC connectors and cover the tip with heatshrink tubing or tape to avoid scratching the enameled front panel.

9. Remove the front frame from the chassis of the instrument.

   a. Remove the screw (0515-1227) that secures the top of the attenuator to the inside of the front frame of the instrument.

   b. Remove the three screws (0515-1101) that secure the A1 front frame assembly to the bottom of the spectrum analyzer.

   c. Remove the three screws (0515-1101) that secure the A1 front frame assembly to the top of the spectrum analyzer.

   d. Remove the A1 front frame assembly from the chassis.

Note that the line switch cable is still attached to the front frame. To remove the line switch you must first remove the display driver and LCD assembly. For instructions on removing the line switch, see "Removal of the Line Switch from the Front Panel" on page 169.

Removal of the Display Driver Board, Inverter Board, and LCD

After the front panel has been removed, follow these steps to remove the display driver and LCD:

1. Disconnect the following cables from the A17 display driver board. These can be disconnected through openings in the display driver shield. See Figure 4-2 on page 170.

   a. W60, a ribbon cable that connects J1 on the A17 display driver board with J8 on the A2 controller board.

   b. W61, which connect J7 on the A17 display driver board with J9 on the A2 controller board.

2. Remove the four screws (0515-0665) that secure the display driver shield to the LCD backplate. Use a T-10 TORX driver set to 6 in./lbs. Remove the display driver shield.

3. Disconnect the following cables from the A17 display driver board:

   a. W64, the VGA ribbon cable, which connects J4 on the A17 display driver board to J1 on the rear panel.

   b. W63, a ribbon cable that connect J5 on the A17 display driver board with the LCD.

4. If you want to remove the A17A1 inverter board, proceed to step a. If you intend to keep the A17A1 inverter board secured to the A17 display driver board, proceed to step 4.

   a. Remove the two screws (0515-0430) which secure the A17A1 inverter board to standoffs on the A17 display driver board.

   b. Disconnect W62 from J6 on the A17 display driver board (do not disconnect W62 from the A17A1 inverter board, to which it is attached).

5. Remove the two backlight cables from the inverter board.

6. Remove the four screws (0515-0372) which secure the display driver board to the LCD backplate. Use a T-10 TORX driver. Remove the display driver board.

7. Remove four black cushions (0400-0333) from the inner-most posts on the LCD backplate.

8. Remove the two large screws (0515-0382) which secure the LCD backplate to the left side of the front panel chassis. Use a T-15 TORX driver.

9. Remove the four (0515-0430) screws which secure the LCD backplate to the right side of the front panel chassis. Use a T-8 TORX driver.

10. Carefully lift the display driver backplate over the two backlight cables and the W63 ribbon cable.

11. Remove the LCD assembly from the black rubber mount Take care not to damage the backlight cables or W63 ribbon cable.

12. To remove the glass plate, first remove the LCD display from the display mount. Carefully remove the glass from the inside of the display mount.

NOTE   The LCD glass plate was originally placed in the LCD assembly in a clean room environment to ensure optimal performance of the LCD display. Take all possible precautions to ensure that the glass plate is clean before replacing it in the LCD assembly.

Removal of the Backlights

1. Remove the LCD assembly by following steps 1 through 12 in "Removal of the Display Driver Board, Inverter Board, and LCD" on page 168.

2. Remove each backlight cable assembly (2090-0380). *Carefully* grasp the end of the metal backlight assembly, which is connected to the backlight cable, and pull the backlight out from its slot. The backlight cable slots are located at the top and at the bottom of the LCD.

NOTE   Whenever there is a need to replace a single backlight, both backlights must be replaced.

Removal of the Line Switch from the Front Panel

After the A1 front frame assembly, the A17 display driver, and the A18 LCD have been removed, you can proceed to remove the line switch. Follow these steps:

1. Remove the green LED from the line switch assembly on the front frame, by gently pulling on the orange and black cables (wrapped in shrink tubing), to which the LED is connected.

2. Remove the two screws (0515-1521) that secure the line switch to the front frame.

3. Remove the screw (0515-0430) that secures the striped green and white ground cable to the line switch.

4. Remove the line switch from the front panel.

Figure 4-2   LCD Assembly - Exploded View
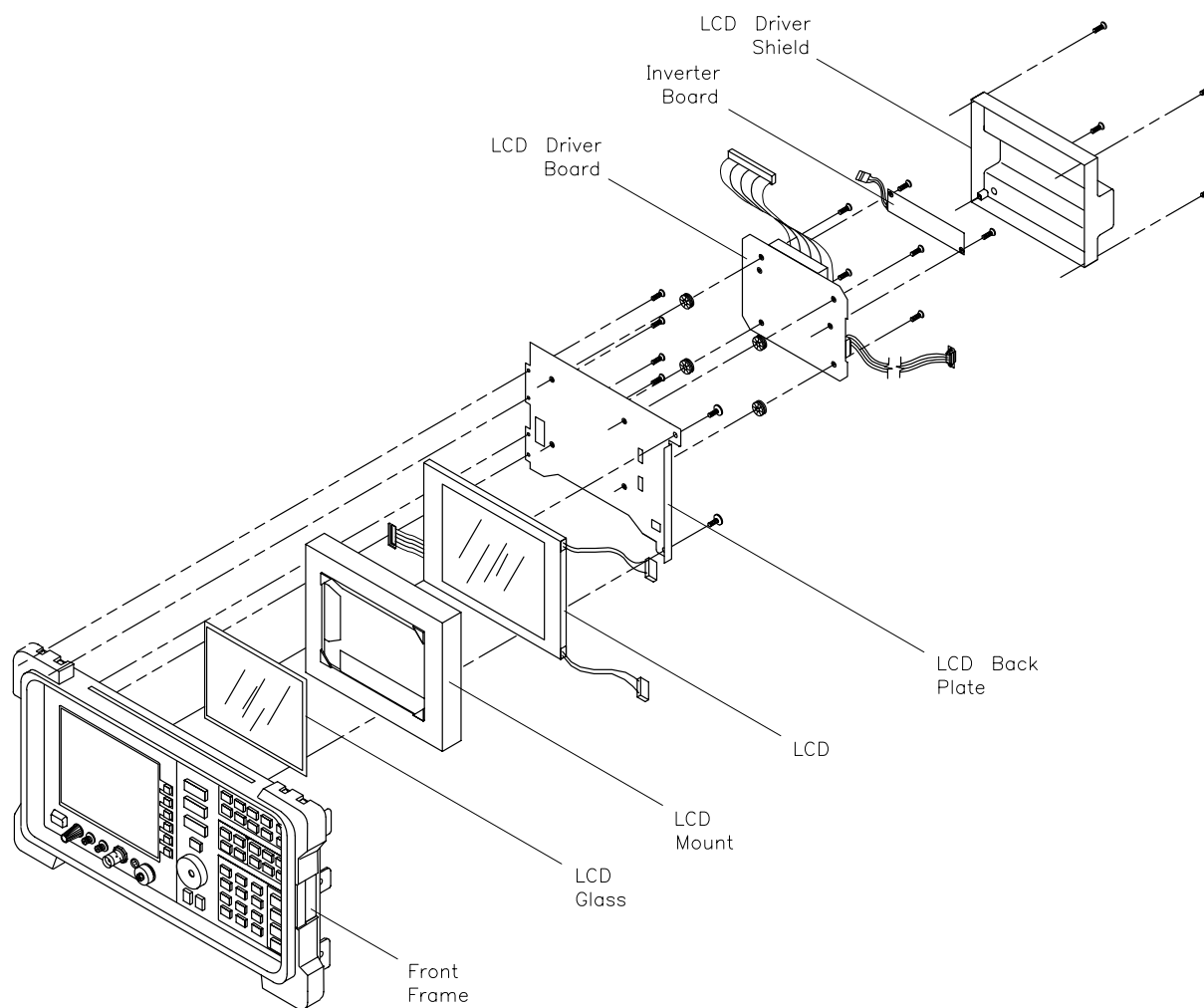
s1135c

Removal of the Keyboard

1. Disconnect cable A1A1W1 from HDR1 on the A1 front panel assembly and from A3J602 on the A3 interface board.

2. Disconnect the power probe cable from the probe power connector on the front frame PC board.

3. Unhook the RPG cable.

4. Remove the seven screws (0515-1934) that secure the front frame PC board to the front frame. Use a T-8 TORX driver set to 6-in/lbs.

Replacement of the Front Frame

1. Remove the cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165. Place the instrument on its side, with the display section upper-most, as shown in Figure 4-1 on page 165.

2. Fold out the A14 and A15 assemblies as described in steps 3 through 4 under "Procedure 9. A14 and A15 Assemblies" on page 217. Facing the front panel, the A14, and A15 assemblies will lie to your right.

3. Fold out the A2, A3, A4, and A5 assemblies as described in steps 2 through 6 under "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188. Facing the front panel, the A2, A3, A4, and A5 assemblies will lie to your left.

4. Place the A1 front frame assembly in the chassis of the instrument.

    a. Position the A1 front frame assembly in the chassis.

    b. Insert the three screws (0515-1101) that secure the front frame chassis to the bottom of the spectrum analyzer.

    c. Insert the three screws (0515-1101) that secure the front frame chassis to the top of the spectrum analyzer.

    d. Insert the screw (0515-1227) that secures the top of the attenuator to the inside of the A1 front frame assembly.

5. Secure the following connectors to the inside of the A1 front panel assembly.

    a. INPUT 50 Ω RF connector. Use a 5/16-inch open-end wrench to connect cable W41 to the front panel from the attenuator.

    b. RF OUT 50 Ω connector *for Option 002 spectrum analyzers.* Use a 5/16-inch open-end wrench to connect cable W47 to the front panel.

c. 1ST LO OUTPUT connector. Connect cable W42 from A7J3 to the front panel 1st LO OUTPUT connector.

   To replace the 1st LO OUTPUT connector use a 5/16 socket and thread pliers. Use the pliers to hold the 1st LO connector in place, while tightening the connector inside the instrument with the 5/16-inch socket.

d. 1ST LO OUTPUT connector *for Option 002 spectrum analyzers.* Connect W46 from the front panel.

e. IF INPUT connector. Connect W36 from the front panel.

6. Replace the following from the face of the front panel.

a. VOLUME knob and potentiometer. Use a 5/16-inch nut driver to secure the VOLUME potentiometer assembly. Use a 0.050 Allen wrench to replace the two screws (3030-0007) that secure the volume knob to the face of the front panel.

b. CAL OUTPUT connector. Replace the dress nut that holds the CAL OUTPUT connector to the front panel.

7. If the line switch has been disconnected from the power supply you will have to route the W3 line switch cable from the right side of the instrument, through the opening behind FL 1, to the power supply on the left side of the instrument.

a. Loosen the two screws (0515-2332) that secure FL 1 to the instrument's chassis.

b. Route the W3 line switch cable from the right side of the instrument to the left side, through the opening that can now be accessed, since FL 1 has been loosened. If the opening is still tight, loosen or remove FL 1 using a 5/16 -inch wrench.

c. Secure the W3 line switch cable to the instrument chassis by routing it through the white collar, that is adjacent to the power supply assembly, on the chassis of the instrument.

d. Route the W3 line switch cable through the notched opening on the right side of the power supply, and insert the line switch connector into A6J2.

   If the line switch has been disconnected from the front panel, see the instructions for its replacement on .

8. Replace the power supply cover by inserting the 3 screws (0515-2309) that secure the power supply cover to the power supply.

9. If the LCD assemblies have not been removed from the front panel assembly, you will need to reconnect the following cables, which are routed through openings in the display driver shield.

    a. W60, the large ribbon cable (80 lines) that goes to J8 on the A2 controller board.

    b. W61, a coax cable that connects to J10 on the A2 controller board.

    c. W64, the VGA ribbon cable (10 lines), that goes to J1 on the rear panel.

Replacement of the Display Driver Board, Inverter Board, and LCD

Follow these steps to replace the A18 LCD assembly, the A17 display driver, and the A17A1 inverter board.

NOTE   If the line switch assembly has been removed from the front panel, it must be replaced before you replace the display driver and LCD assemblies.

1. Place the front panel face down on your bench. The opening for the display will be on the right side of the front panel.

2. If the LCD glass place has been removed, carefully insert the glass plate into the brackets on the front side of the rubber display mount. Make sure that the side of the glass which has a broad silver border (the left side, when facing the front of the display) is inserted into the side of the mount that has larger brackets, into which the glass plate will slide.

NOTE   The glass plate was originally placed in the LCD assembly in a clean room environment to ensure optimal performance of the LCD display. Take all possible precautions to ensure that the glass plate is clean before placing it in the LCD assembly.

3. Insert the LCD into the display mount. The LCD is correctly oriented when the small ribbon cable from the LCD extends through an opening in the right side of the display mount, and the two backlight cables extend through openings on the left side of the mount.

4. Carefully lower the LCD bookplate onto the display mount. Ensure that the ribbon cable on the right, and the two backlight cables on the left, are inserted into the appropriate openings in the LCD backplate.

5. Lower the LCD backplate and LCD assembly, as a unit, into the display section on the right side of the A1 front frame chassis.

6. Secure the LCD backplate to the chassis.

   a. Insert four (0515-0444) screws into the right side of the backplate. Use a T-8 TORX driver.

   b. Insert two large (0515-0382) screws into the left side of the LCD backplate. Use a T-15 TORX driver.

7. Place the four black cushions (0400-0333) on the four inner-most posts on the LCD backplate. Place the A17 display driver board on the four black cushions. Insert the four screws (0515-0372) that secure the A17 display driver board to the LCD backplate, into the posts on which you have set the cushions. Use a T-10 TORX driver.

8. If the A17A1 inverter board has been removed from the driver board, proceed to step a. below. If the inverter board is attached to the A17 display driver, proceed to step 10.

   a. Connect the W62 cable from the A17A1 inverter board to J6 on the A17 display driver board.

   b. Insert 2 screws (0515-0430) that secure the A17A1 inverter board to the standoffs on the A17 display driver board.

9. Reconnect ribbon cable W63, which connects the A18 LCD with J5 on the A17 display driver board.

10. Connect the two backlight cables from the A18 LCD to the two slotted connectors on the A17A1 inverter board.

11. Route W64, the VGA cable, from J1 on the rear panel, through the rectangular opening in the display driver shield, to J7 on the A17 display driver board (the display driver shield has not yet been secured to the LCD backplate).

12. Lower the display driver shield onto the LCD backplate. Insert four screws (0515-0665) that secure the LCD backplate to the display driver board shield. Use a T-10 TORX driver.

13. Route cable W61 from J9 on the A2 controller board, through the circular opening in the display driver shield, to J7 on the A17 display driver board.

14. Route cable W60 from J8 on the A2 controller board, through the rectangular opening in the display driver shield, to J7 on the A17 display driver board.

15. Connect ribbon cable A1A1W1 from J602 on the A3 interface board to HDR1 on the A1 front panel assembly.

Replacing the Backlights

1. If the LCD or backlights have not been removed from the front frame, follow the procedures outlined in "Removal of the Front Frame" on page 166, "Removal of the Display Driver Board, Inverter Board, and LCD" on page 168, and "Removal of the Backlights" on page 169, as needed.

2. *Carefully* grasp the end of the replacement backlight cartridge (2090-0380), which is attached to the backlight cable, and insert the backlight into the backlight slot at the top of the LCD. Repeat for the backlight located at the bottom of the LCD.

NOTE
Whenever there is a need to replace a single backlight, both backlights must be replaced.

3. Insert the LCD into the display mount. The LCD assembly is correctly oriented when the small ribbon cable extends through an opening in the right side of the display mount.

4. Follow steps 4 through 17 of "Replacement of the Display Driver Board, Inverter Board, and LCD" on page 173 to complete replacement of the LCD into the front panel. Follow the instructions in "Replacement of the Front Frame" on page 171 to replace the front panel in the front frame.

Replacement of the Line Switch

After you have replaced the A1 front frame assembly you can replace the line switch by following these steps (note that the line switch must be replaced before the LCD and display driver can be replaced):

1. Insert the line switch into the A1 front frame assembly. Insert the two screws (0515-1521) that secure the line switch to the front frame.

2. Insert the screw (0515-0430) that secures the striped green and white ground cable for the line switch (this screw also secures the ground for the power probe; if the black cable from the power probe cable assembly is not secured to the ground, secure it also).

3. Carefully insert the green LED from the top-center of the line switch assembly into the LED opening in the A1 front frame assembly.

Replacement of the Keyboard

1. Insert the seven screws (0515-1934) that secure the front frame PC board to the A1 front frame assembly. Use a T-8 TORX driver.

2. Connect the RPG cable to the RPG connector on the front frame PC board.

3. Connect the power probe cable to the connector that is labelled "probe power" on the front frame PC board.

4. Connect A1A1W1 from HDR1 on A1 front frame assembly to A3J602 on the A3 interface board.

Procedure 2B. A1 Front Frame/A18 CRT (8562E)

Removal

The voltage potential at A6A1W3 is +9 kV. Disconnect at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument.

1. Remove the spectrum analyzer cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165.

2. Fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 2 through 6.

3. Disconnect A1A1W1 from A3J602.

4. Place the spectrum analyzer top-side-up on the work bench.

5. Connect the spectrum analyzer line-power cord to provide proper grounding while discharging the A6A1W3 post-accelerator cable. Make sure that the spectrum analyzer line-power switch is in the off position.

6. Connect a high voltage probe (1000:1), such as the 34111A to a voltmeter with a 10 megohm input.

7. Connect the clip lead of the probe (ground) to the chassis of the spectrum analyzer.

8. Slip the tip of the high voltage probe under the rubber shroud of the A6A1W3 post-accelerator cable to obtain a reading on the voltmeter. See Figure 4-3 on page 179.

9. Keep the high voltage probe on the post-accelerator connector until the voltage has dropped to a voltmeter reading of less than 5 mV (less than 5 V at the connector). This normally takes about 30 seconds.

10. Disconnect the line-power cord from the spectrum analyzer.

To avoid possible electrical shock, in the next step, use a screwdriver having a conductive metal shank and tip, with an insulated handle.

11. Connect one end of a wire clip lead to a small screwdriver having a conductive shank and tip. Connect the other end of the clip lead to the CRT shield assembly as shown in Figure 4-3 on page 179. Hold the insulated screwdriver handle and slip the tip of the screwdriver under the rubber shroud of the A6A1W3 post-accelerator cable, shorting the cable to ground through the CRT shield assembly. See Figure 4-3 on page 179.

12. Using a small screwdriver with the shank in contact with the CRT shield assembly, slip the tip of the screwdriver under the A6A1W3 post-accelerator cable rubber shroud and short the cable to ground on the CRT shield assembly.

13. Pry out the black grommet protecting post-accelerator cable A6A1W3 from the CRT shield assembly.

14. Carefully unsnap the A6A1W3 post-accelerator cable from the CRT and discharge it by shorting the cable to chassis ground on the CRT shield assembly.

15. Place the spectrum analyzer on its right side frame with the front frame assembly hanging over the front edge of the workbench.

16. Fold out the A14 and A15 assemblies as described in steps 3 and 4 under "Procedure 9. A14 and A15 Assemblies" on page 217.

WARNING **The voltage potential at A6A1W3 is +9 kV. Failure to discharge A6A1W3 correctly may result in severe electrical shock to personnel and damage to the instrument.**

Figure 4-3   Discharging High Voltage on the CRT

SLIP PROBE
UNDER
RUBBER SHEATH

GROMMET

A6A1W3

1000:1
HIGH-VOLTAGE PROBE

CONDUCTIVE
SHAFT

GROMMET

A6A1W3

CLIP LEAD

INSULATED
HANDLE
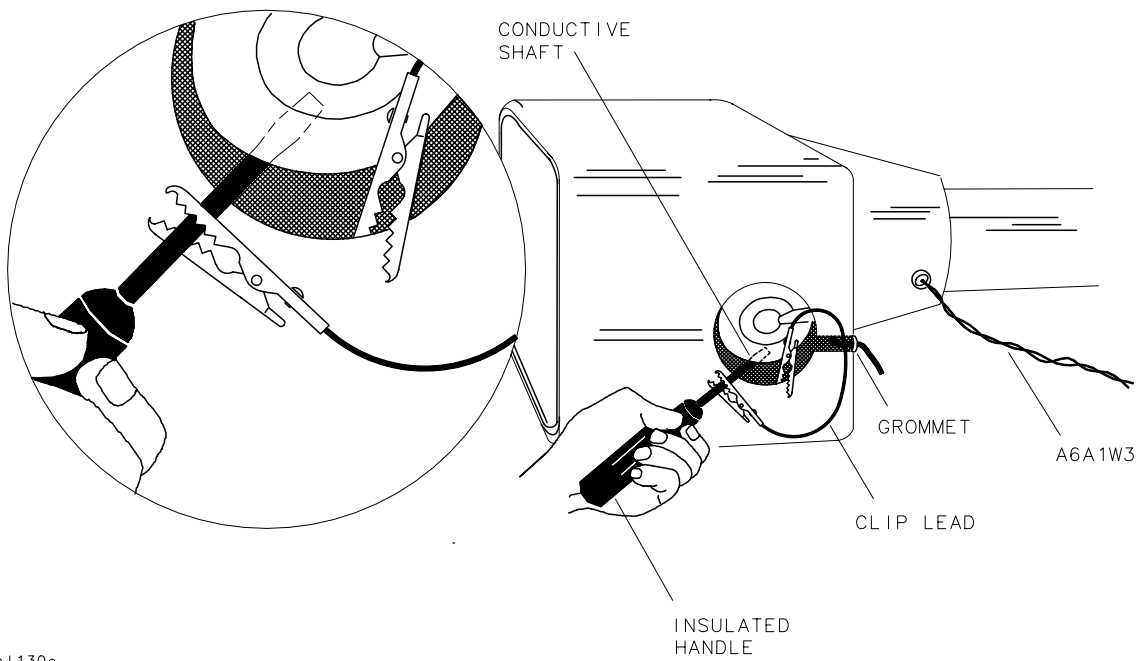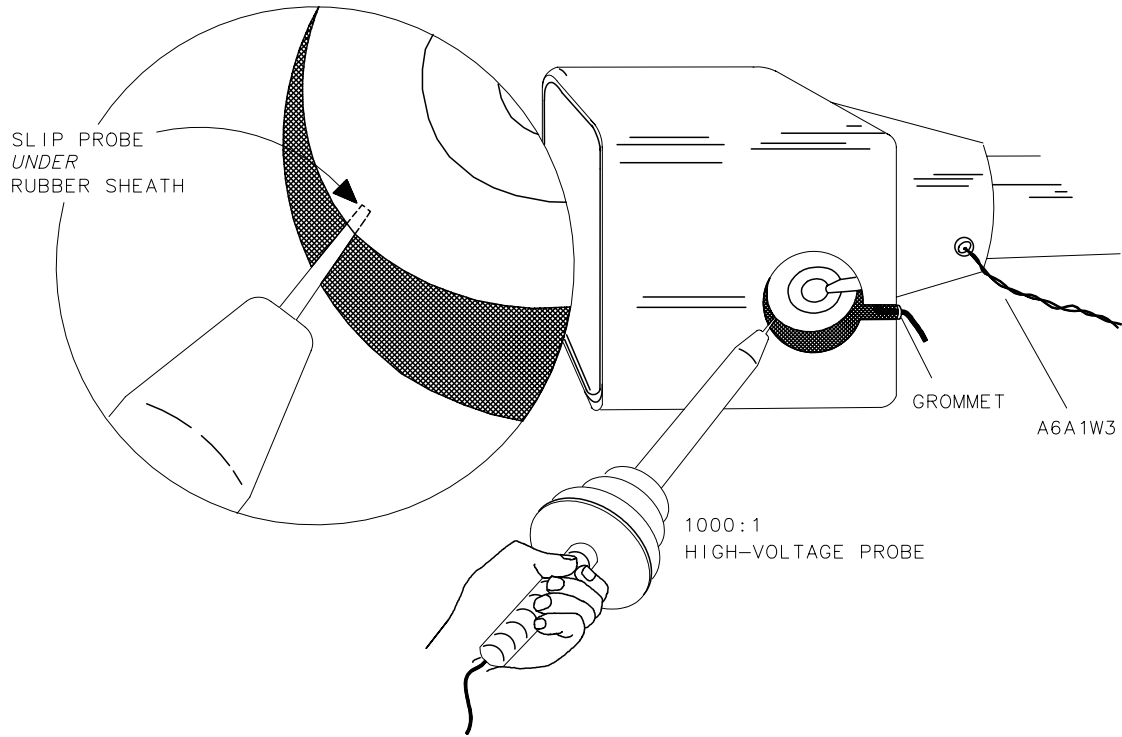
sl130e

Figure 4-4   A9, A18, and Line-Switch Assembly Mounting Screws
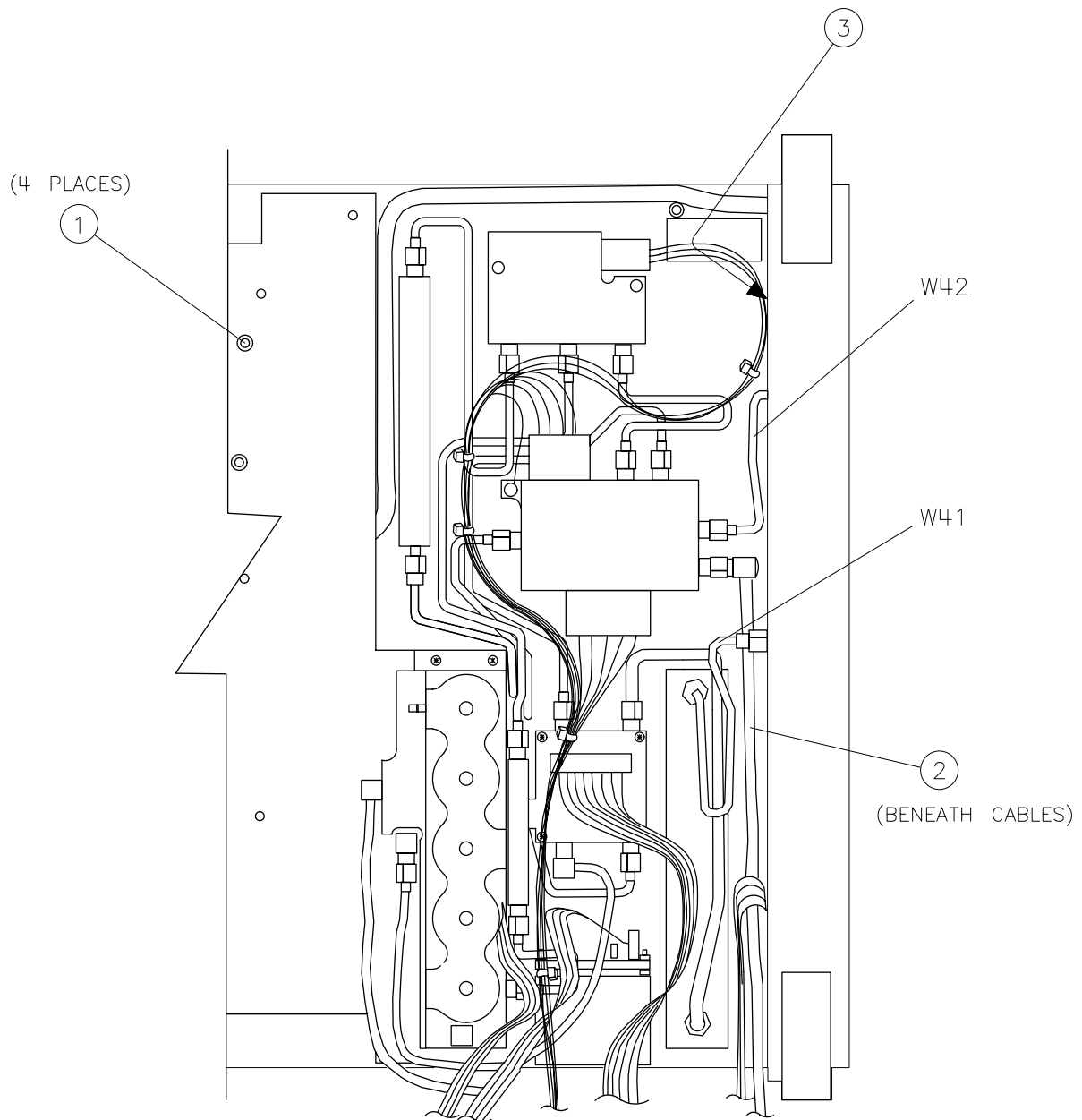
s l 12e

17. Remove screw (2) securing the A9 input attenuator assembly to the center support on the front frame. See Figure 4-4 on page 180.

18. Use a 5/16-inch open-end wrench to disconnect W41 from the front panel INPUT 50Ω connector. Loosen the opposite end of W41.

19. Disconnect W42 from A7 and the front panel First LO OUTPUT connector.

20. Disconnect W36, coax 86, from the front panel IF INPUT connector.

21. Remove the VOLUME knob and potentiometer from the front panel. If necessary, drill out the nut driver used to remove the VOLUME potentiometer and cover the tip with heatshrink tubing or tape to avoid scratching the enameled front panel.

22. Use a 9/16-inch nut driver to remove the dress nut holding the front panel CAL OUTPUT connector to the front panel. If necessary, drill out the nut driver to fit over the BNC connectors and cover the tip with heatshrink tubing or tape to avoid scratching the enameled front panel.

23. Loosen screw (3) securing the line-switch assembly to the front frame. This is a captive screw and cannot be removed from the line-switch assembly. See Figure 4-4 on page 180.

24. Gently remove the line-switch assembly, using caution to avoid damaging A1W1 and power indicator LED A1W1DS1.

25. Remove A1W1 and A1W1DS1 from the line-power switch assembly.

26. Remove the three screws (1) securing the front frame assembly to the right side frame of the spectrum analyzer. See Figure 4-5 on page 182.

Figure 4-5   front frame Mounting Screws
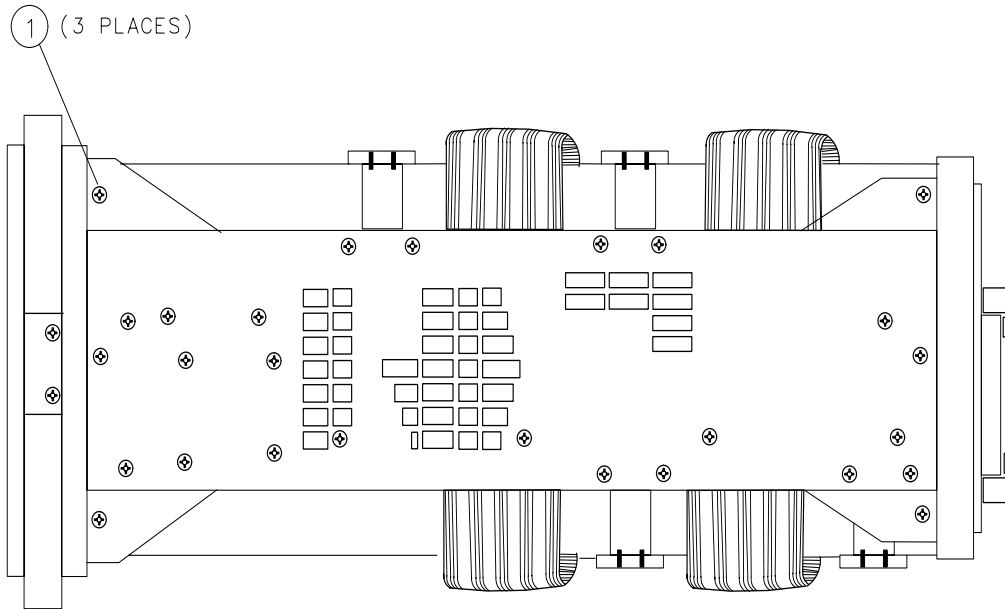
s l 1 1 6 e

27. Remove the three screws securing the front frame assembly to the left side frame of the spectrum analyzer.

28. Remove the four screws (1) (Figure 4-4 on page 180) securing the CRT mounts to the deck.

29. Pull the cable tie (1) to free W9. See Figure 4-6 on page 183. Gently pry W9, the CRT cable, from the end of the CRT assembly.

30. Support the A18 CRT assembly while gently pulling the front frame and CRT out of the spectrum analyzer 1 or 2 inches.

31. Disconnect A18W1, the trace align wires, from A17J5. Remove the front frame and CRT assemblies.

32. Gently pull the CRT assembly off of the front frame assembly.

Figure 4-6   Installing the CRT and front frame Assemblies
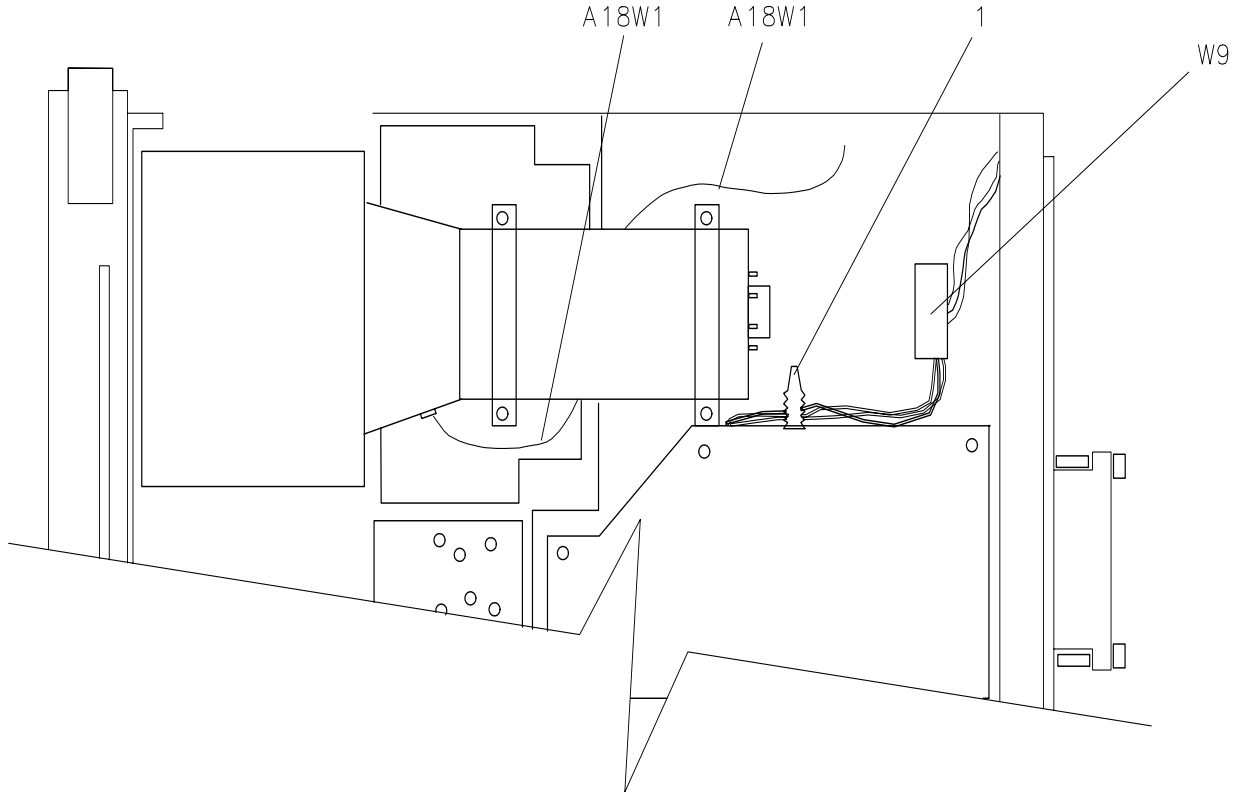
sm627e

Replacement

Use care when handling the glass CRT EMI shield. The glass may be cleaned using thin-film cleaner (part number 8500-2163) and a lint-free cloth. When installing the glass shield, face the side of the glass with the silver coated edge towards the inside of the spectrum analyzer.

1. Place the spectrum analyzer on its right side frame with the front end extending slightly over the front of the work bench.

2. Gently place the A18 CRT assembly into the A1 front frame assembly as illustrated in Figure 4-7 on page 184.

3. Place the front frame and CRT assemblies into the spectrum analyzer, using caution to avoid pinching any cables.

4. Dress the A18W1 trace-align wires between the CRT assembly mounts and the A6 power supply top shield.

Figure 4-7   Placing the CRT into the Front Frame

A1A1W1

SK127
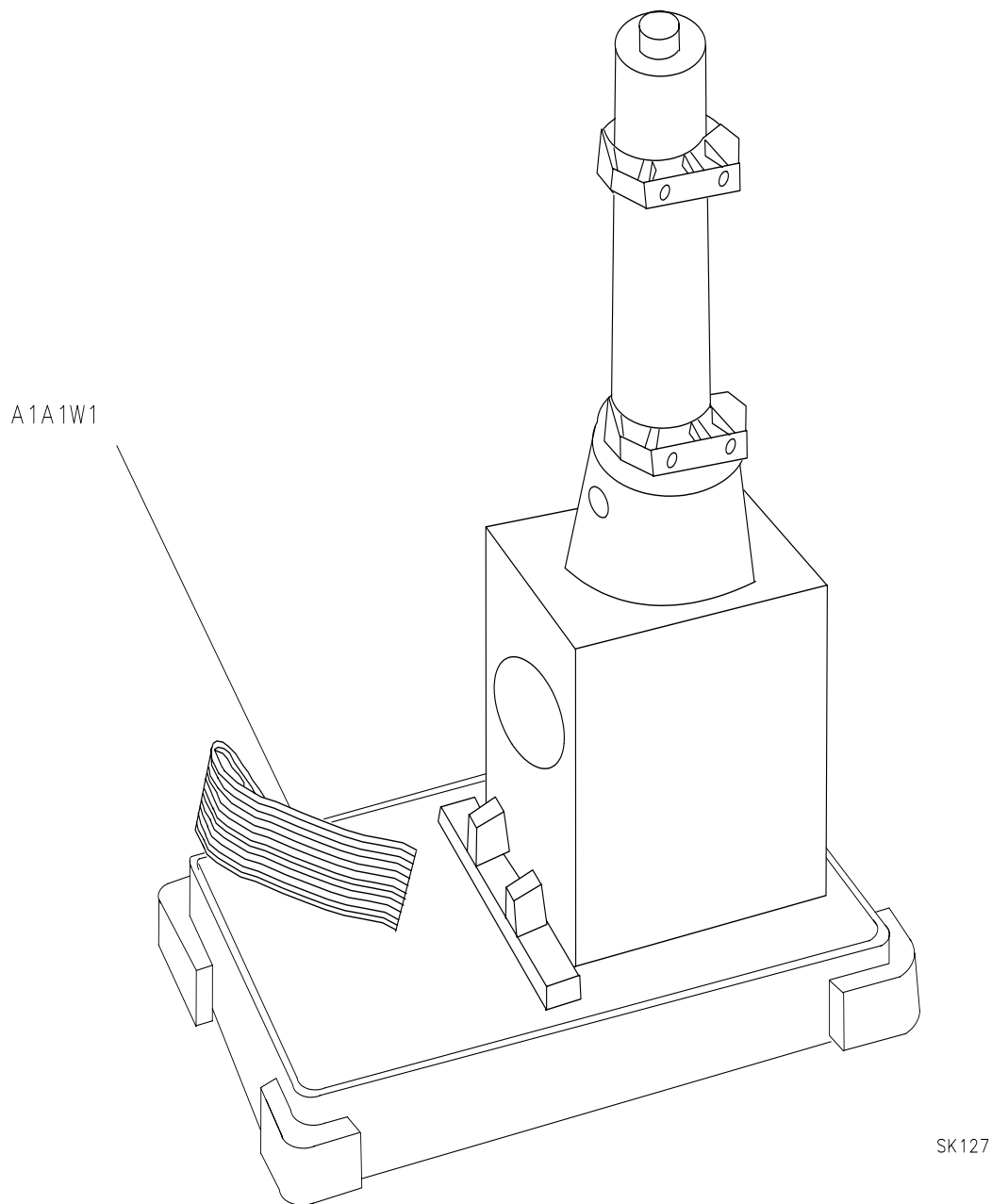
5. Connect A18W1 to A17J5.

6. Snap CRT cable W9 onto the end of the CRT assembly.

7. Fully seat the front frame and CRT assemblies into the spectrum analyzer.

8. Secure the front frame to the side frames of the spectrum analyzer, using three flathead screws per side. See Figure 4-5 on page 182.

9. Retighten the four screws securing the CRT mounts to the deck.

10. Place W9 between the CRT assembly and the A6 power supply assembly top shield so that the W9 wires are below the surface of the top shield.

11. Connect W42 to A7J5 and the front panel First LO OUTPUT connector.

12. Use a 9/16-inch nut driver to reconnect CAL OUTPUT connector to the front panel.

13. Connect the VOLUME potentiometer and knob to the front panel.

14. Connect W36, coax 86, to the front panel IF INPUT connector.

15. Use a 5/16-inch wrench to connect W41 from the A9 input attenuator to the front panel INPUT 50Ω connector. Make sure that W40, W36, and A1W1 are routed between W41 and the attenuator bracket. Secure the A9 input attenuator bracket to the center support on the front frame using one panhead screw. See Figure 4-4 on page 180 (2).

16. Place led A1W1DS1 into the line-power switch assembly.

17. Attach the line switch assembly into the front frame using one panhead screw. Be sure to connect the line-power switch ground lug with the screw. The screw is captive.

18. Fold up the A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217 steps 3 through 5.

19. Place the spectrum analyzer top-side-up on the work bench and connect A1A1W1 to A3J602.

20. Snap post-accelerator cable A6A1W3 to the A18 CRT assembly.

21. Snap the black grommet protecting the A6A1W3 into the CRT shield.

22. Fold up assemblies A2, A3, A4, and A5 as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 6 through 12.

23. Replace the spectrum analyzer cover assembly.

24. Connect the line-power cord and switch the spectrum analyzer power on. If the display does not operate properly, turn off spectrum analyzer power, disconnect the line cord, and recheck the spectrum analyzer.

Procedure 3. A1A1 Keyboard/Front Panel Keys

Removal

1. Remove the front frame from the spectrum analyzer. Place the front frame face down on the bench. For 8562EC instruments, follow the instructions in "Procedure 2A. A1 Front Frame/A18 LCD (8562EC)" on page 166. For 8562E instruments, follow the instructions in "Procedure 2B. A1 Front Frame/A18 CRT (8562E)" on page 177.

   For 8562EC instruments, proceed to step 3. For 8562E instruments, proceed to step 2.

2. Remove the front frame center support.

3. Disconnect A1W1 from A1A1J3 and the RPG cable from A1A1J2.

4. Remove the nine screws holding the A1A1 keyboard assembly to the front frame and remove the assembly.

5. Remove the rubber keypad.

NOTE   In 8562E instruments, the front panel softkey actuators are part of the CRT bezel assembly and are not replaceable. Should the softkeys become damaged, replace the bezel assembly.

Replacement

1. Install the rubber keypad, ensuring that the screw holes are visible through the pad.

2. Place the A1A1 keyboard assembly over the rubber keypad. Secure with nine panhead screws.

3. Connect the RPG cable to A1A1J2, and A1W1 to A1A1J3.

   For 8562EC instruments, proceed to step 5. For 8562E instruments, proceed to step 4.

4. Secure the center support to the front frame using two panhead screws. The arrow stamped on the center support should point to the top of the frame.

5. Install the front frame assembly. For 8562EC instruments, follow the instructions in "Procedure 2A. A1 Front Frame/A18 LCD (8562EC)" on page 166. For 8562E instruments, follow the instructions in "Procedure 2B. A1 Front Frame/A18 CRT (8562E)" on page 177.

Procedure 4. A1A2 RPG

Removal

1. Remove the A9 input attenuator as described in "Procedure 8. A7 through A13 Assemblies" on page 206.

2. Disconnect the RPG cable from the A1A1 keyboard assembly.

3. If the serial number of your instrument is above or equal to 3738A00518 (8562E/EC) proceed to step a. If the serial number of your instrument is below3738A00518 (8562E) proceed to step b.

   a. Pull the front panel RPG knob off of the face of the front panel of the spectrum analyzer. Proceed to step 4.

   b. Remove the set screw from the front panel RPG knob using a number 6 hex (Allen) wrench. Proceed to step 4.

4. Use a 7/16-inch nut driver, set to 20-in./lbs., to remove the nut holding the RPG shaft to the front panel.

5. Remove the RPG.

Replacement

1. Place the RPG into the front frame with the cable facing the bottom of the spectrum analyzer. Place a lock washer and nut on the RPG shaft to hold it in the frame. If the serial number of your instrument is below 3738A00518 (8562E) proceed to step a. Otherwise, proceed to step 2.

   a. Insert the set screw into the RPG knob using a number 6 hex (Allen) wrench. Proceed to step 2.

2. Use a 7/16-inch nut driver to secure the RPG assembly to the front frame.

3. Connect the RPG cable to A1A1J2.

4. Insert the RPG knob into the front panel assembly.

5. Replace the A9 input attenuator as described in "Procedure 8. A7 through A13 Assemblies" on page 206.

Procedure 5. A2, A3, A4, and A5 Assemblies

Removal

1. Remove the spectrum analyzer cover.

2. Place the spectrum analyzer on its right side frame.

3. Remove the eight screws holding the A2, A3, A4, and A5 assemblies to the top of the spectrum analyzer. These screws are labeled (2), (3), and (4) in Figure 4-8 on page 189. They are also labeled on the back of the A2 board assembly.

4. Remove ribbon cable W4 from A2J6. See Figure 4-8 on page 189.

CAUTION   Do not fold the board assemblies out of the spectrum analyzer one at a time. Always fold the A2 and A3 assemblies as a unit and the A4 and A5 assemblies as a unit. Folding out one assembly at a time binds the hinges attaching the assemblies and may damage an assembly and hinge.

5. The board assemblies are attached to the right side frame of the spectrum analyzer with two hinges. Fold both the A2 and A3 assemblies out of the spectrum analyzer as a unit.

6. Fold both the A4 and A5 assemblies out of the spectrum analyzer as a unit.

7. Remove the cables from the assembly being removed, as illustrated in Figure 4-9 on page 190.

8. Remove the two screws that attach the assembly being removed to its two mounting hinges.

CAUTION   Do not torque shield TORX screws to more than 8 inch-pounds. Applying excessive torque will cause the screws to stretch.

NOTE   Diagrams that illustrate features common to E-series and EC-series instruments are shown with E-series instruments. Where there are differences between E-series and EC-series features separate diagrams are provided.

Figure 4-8   A2, A3, A4, and A5 Assembly Removal
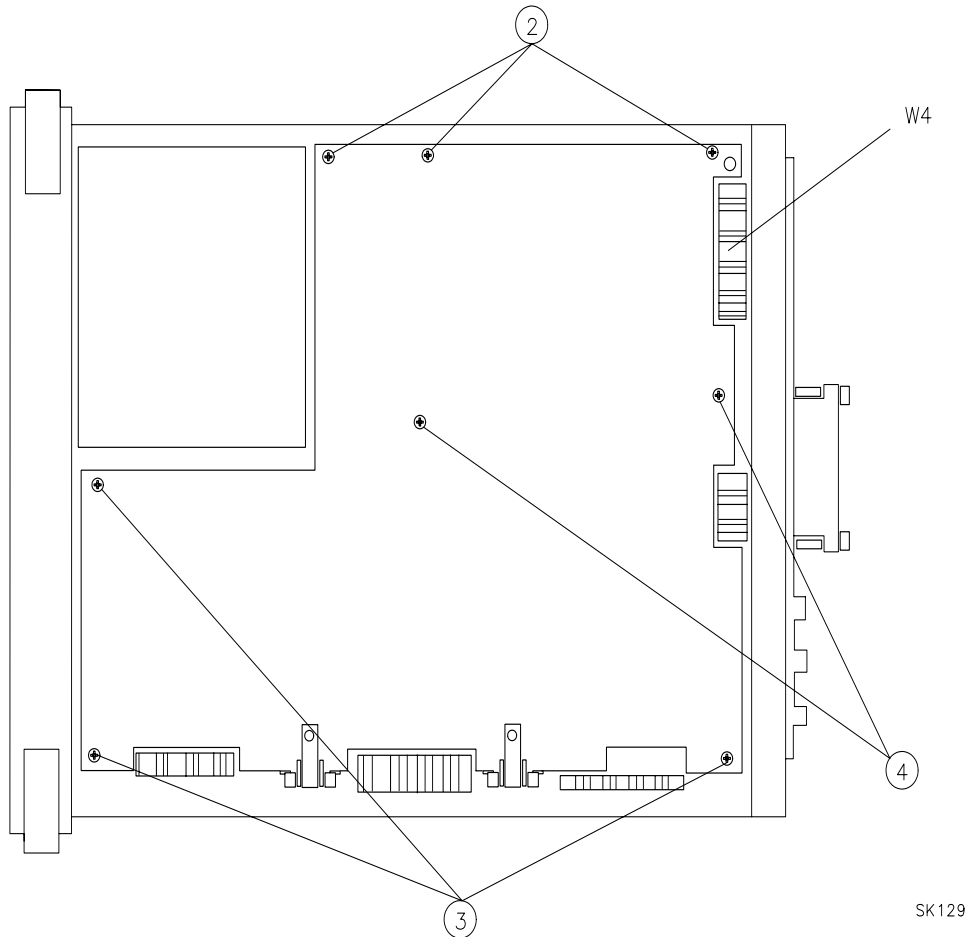
Replacement

1. Place the spectrum analyzer on its right side on the work bench.

2. Attach the assembly being installed to the two chassis hinges with two panhead screws.

3. Leave the assembly in the folded-out position and attach ribbon cables W1 and W2.

4. Attach all cables to the assembly, as illustrated in Figure 4-9 on page 190.

5. Locate the cable clip on the inside of the right side frame. Make sure that the coaxial cables are routed properly on the clip as illustrated in Figure 4-12 on page 192 for EC-series instruments, and in Figure 4-13 on page 193 for E-series instruments.

6. Lay the A2, A3, A4, and A5 assemblies flat against each other in the folded-out position. Make sure that no cables become pinched between the two assemblies.

Figure 4-9   Assembly Cables (1 of 3) – EC-Series
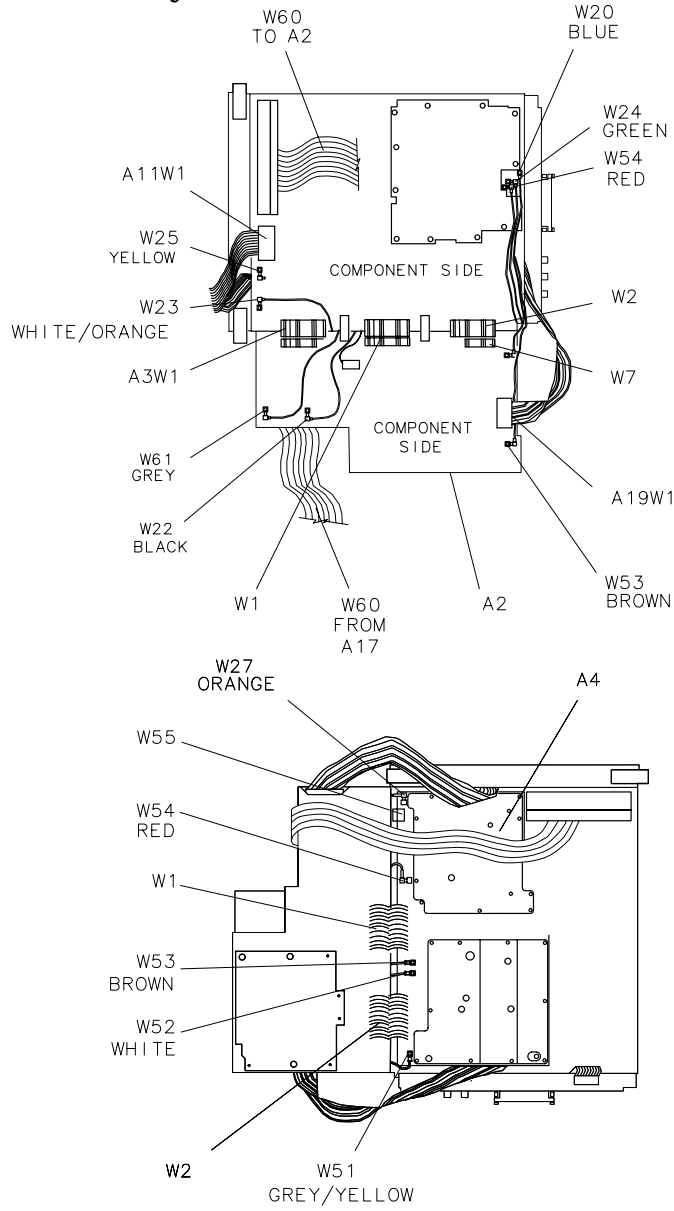
Figure 4-10   Assembly Cables (2 of 3) – EC-series
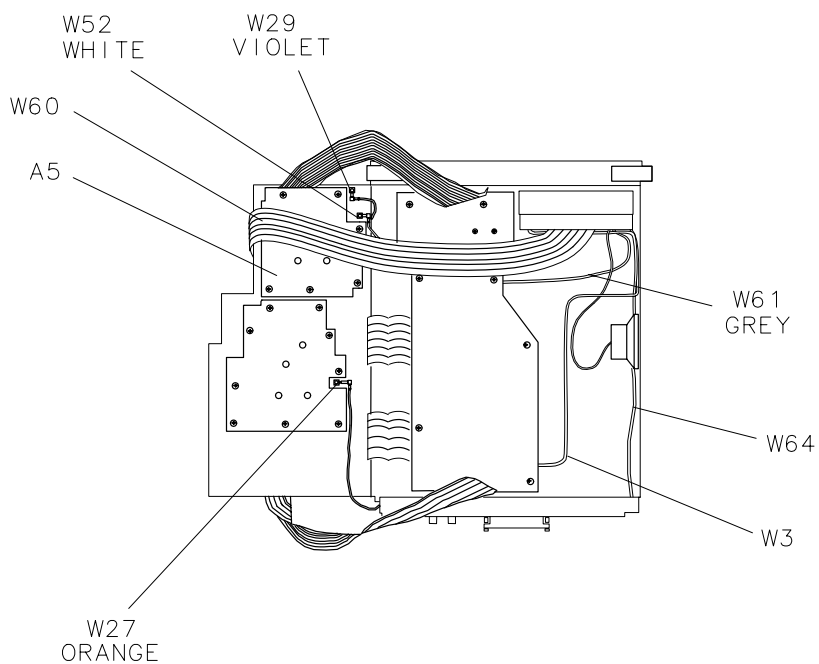
Figure 4-11   Assembly Cables (3 of 3)– E-series
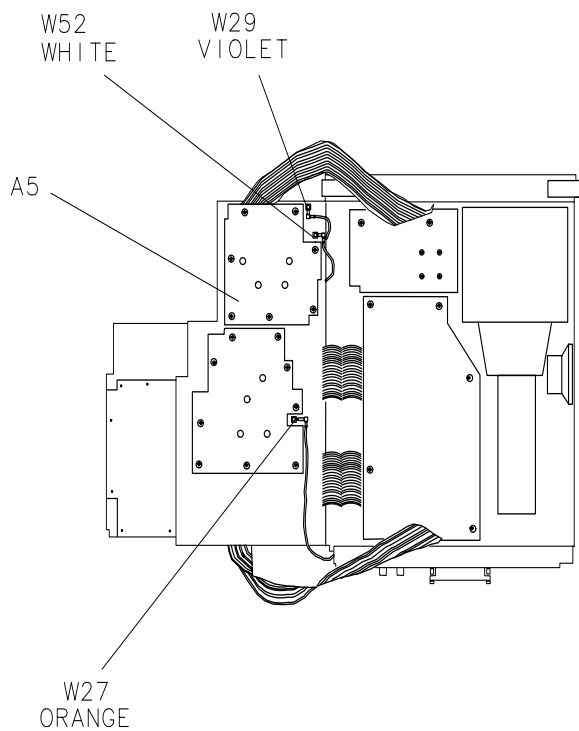
Figure 4-12   Coaxial Cable Clip – EC-Series

CABLE CLIP
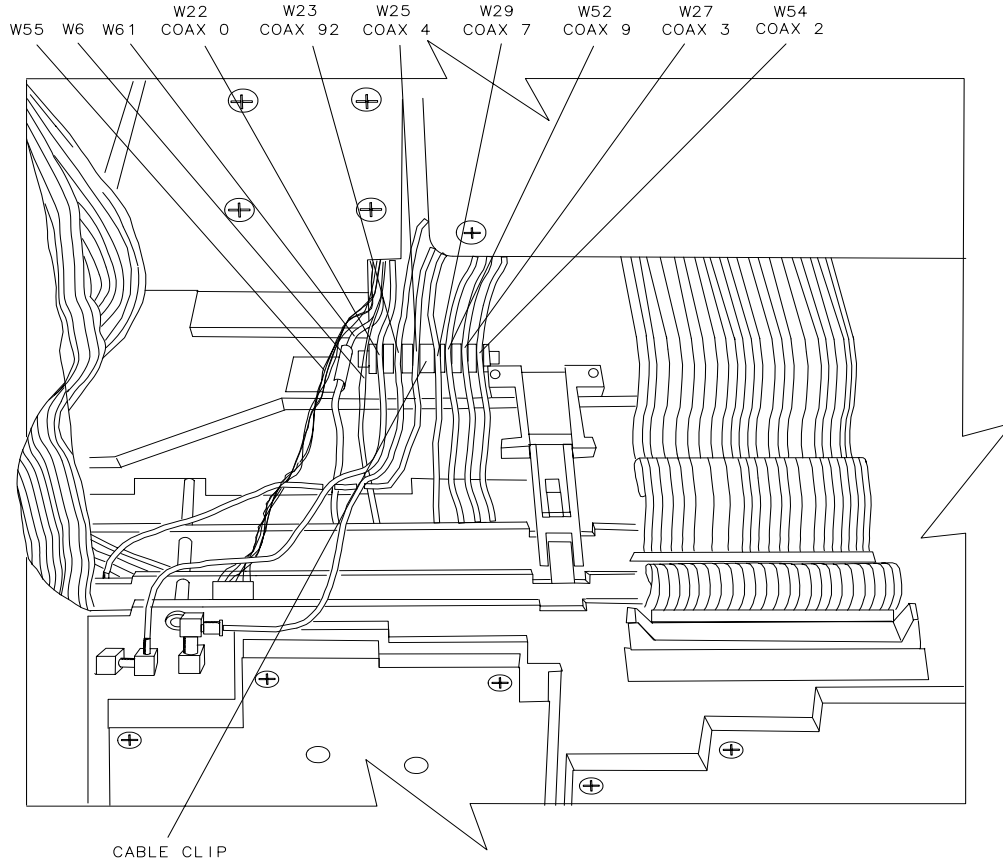
sl121c

7. Check to ensure that no cables will become pinched under the hinges when folding up the A4 and A5 assemblies.

8. Fold the A4 and A5 assemblies together as a unit into the spectrum analyzer. Use caution to avoid damaging any cable assemblies. The standoffs on the A5 assembly must fit into the cups on the A6 power supply top shield.

9. Fold the A2 and A3 assemblies together as a unit into the spectrum analyzer. Be sure to fold GPIB cable A19W1 between the A3 and A4 assemblies, using the two sets of hook and loop (Velcro) fasteners.

10. Fold ribbon cable A1A1W1 between A3 and A4 assemblies. Take care to dress the protective tubing as close to A3J602 connector as possible, so that the tubing does not fold with the cable. See Figure 4-14 on page 194.

11. Attach ribbon cable W4 to A2J6 while folding up the assemblies.

12. Secure the assemblies using the eight screws removed in "Removal," step 3. See Figure 4-8 on page 189.

Figure 4-13   Coaxial Cable Clip – E-Series

CABLE CLIP
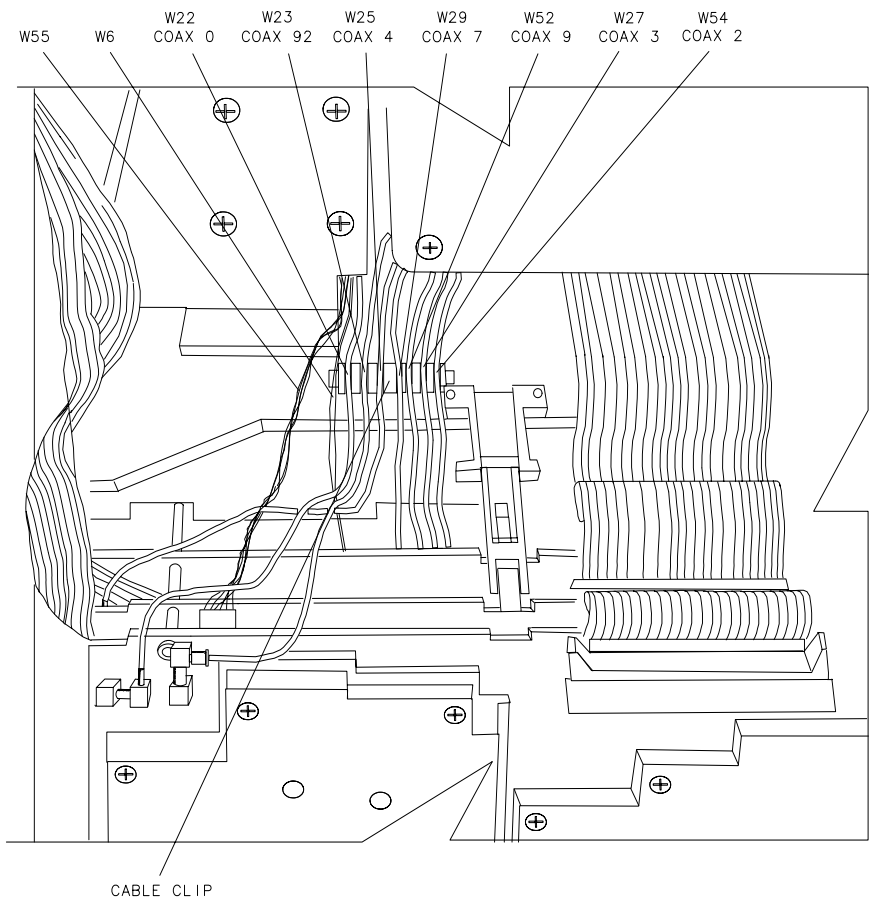
sl19e

Figure 4-14   **GPIB and A1A1 W1 Cable Placement**
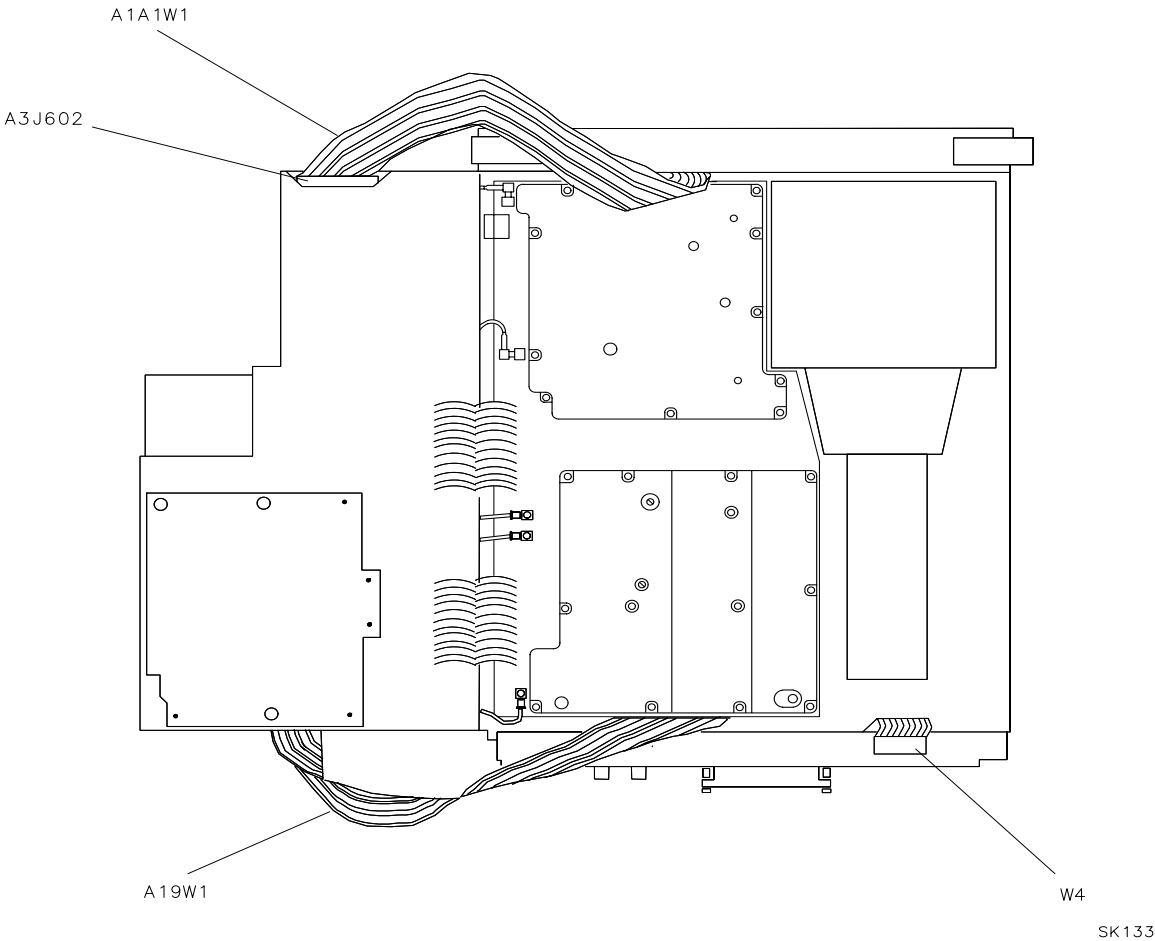
Procedure 6A. A6 Power Supply Assembly (8562EC)

Removal

WARNING

The A6 Power Supply assembly contains lethal voltages with lethal currents in all areas. Use extreme care when servicing this assembly. Always disconnect the power cord from the instrument before beginning this replacement procedure. Failure to follow this precaution will represent a shock hazard which may result in personal injury.

1. Disconnect the power cord from the spectrum analyzer.

2. Remove the spectrum analyzer cover assembly. Refer to "Procedure 1. Spectrum Analyzer Cover" on page 165.

3. Fold out the A2, A3, A4, and A5 assemblies as described in steps 2 through 6 under "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

4. Place the spectrum analyzer on the workbench with A2, A3, A4, and A5 folded out to the right.

5. Remove the three screws securing the power supply shield to the power supply and remove the shield. See Figure 4-16 on page 197.

6. Disconnect all cables from the A6 power supply assembly. See Figure 4-17 on page 200.

7. Use a T-10 TORX driver to remove the screws from the shield wall, the heatsink, the base of the power supply (0515-1950) and the A6 power supply assembly.

8. Remove the A6 power supply assembly by lifting from the regulator heatsink toward the front of the spectrum analyzer.

Figure 4-15   Power Supply Cover
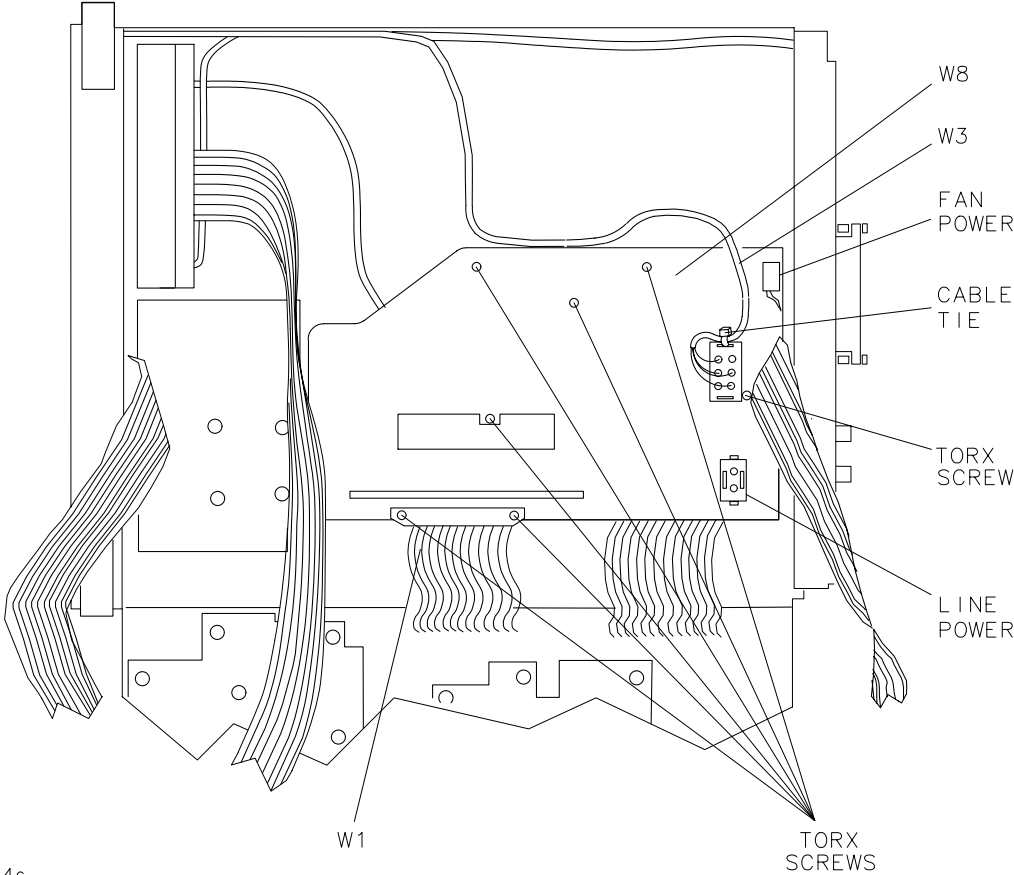
Replacement

1. Ensure that the bottom shield wall is in place before replacing the A6 power supply assembly.

2. Attach the A6 power supply assembly to the spectrum analyzer chassis and top shield wall using the four screws, torqued to 10-inch lbs. Attach all other screws, torqued to 6-inch lbs.

3. Connect W1 to A6J1, W3 to A6J2, fan power wires to A6J3, W8 to A6J4, and the line-power jack to A6J101. See Figure 4-15 on page 196.

4. Ensure that all cables are safely routed and will not be damaged when securing the A6 cover.

5. Secure the power supply cover shield to the power supply using three flathead screws (1). See Figure 4-16 on page 197. One end of the cover fits into a slot provided in the rear frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove.

6. Fold the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in steps 6 through 12 under "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

Figure 4-16   **Power Supply Cover**
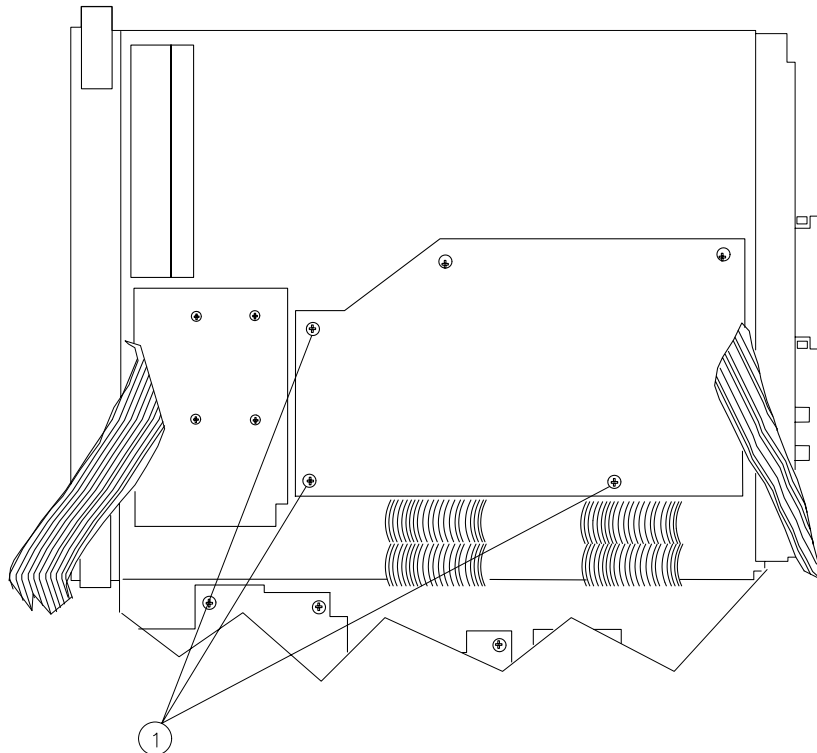
sp122c

Procedure 6B. A6 Power Supply Assembly (8562E)

Removal

WARNING
The A6 power supply and A6A1 high voltage assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before beginning this replacement procedure. Failure to follow this precaution will present a shock hazard which may result in personal injury.

1. Disconnect the power cord from the spectrum analyzer.

2. Remove the spectrum analyzer cover assembly. Refer to "Procedure 1. Spectrum Analyzer Cover" on page 165.

3. Fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 2 through 6.

4. Place the spectrum analyzer top-side-up on the work bench with A2, A3, A4, and A5 folded out to the right.

WARNING
The voltage potential at A6A1W3 is +9 kV. Disconnect at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument.

5. Connect the spectrum analyzer line-power cord to provide proper grounding while discharging the A6A1W3 post-accelerator cable. Make sure that the spectrum analyzer line-power switch is in the off position.

6. Connect a high voltage probe (1000:1), such as the 34111A to a voltmeter with a 10 megohm input.

7. Connect the clip lead of the probe (ground) to the chassis of the spectrum analyzer.

8. Slip the tip of the high voltage probe under the rubber shroud of the A6A1W3 post-accelerator cable to obtain a reading on the voltmeter. See Figure 4-3 on page 179.

9. Keep the high voltage probe on the post-accelerator connector until the voltage has dropped to a voltmeter reading of less than 5 mV (less than 5 V at the connector). This normally takes about 30 seconds.

10. Disconnect the line-power cord from the spectrum analyzer.

11. Using a small screwdriver with the shank in contact with the CRT shield assembly, slip the tip of the screwdriver under the rubber shroud of the A6A1W3 post-accelerator cable and short the cable to ground on the CRT shield assembly. See Figure 4-3 on page 179.

12. Remove the three screws securing the power supply shield to the power supply and remove the shield.

13. Remove the three screws securing the A6A1 high voltage assembly to the A6 power supply assembly.

14. Disconnect ribbon cable A6A1W1 from A6J5 and lift the A6A1 assembly out of the way. See Figure 4-17 on page 200.

15. Disconnect all cables from the A6 power supply assembly. See Figure 4-17 on page 200.

16. Use a TORX screwdriver to remove the hardware from the shield wall, the heatsink, and the A6 power supply assembly.

17. Remove the A6 power supply assembly by lifting from the regulator heatsink toward front of spectrum analyzer.

Replacement

1. Ensure that the bottom shield wall is in place before replacing the A6 power supply assembly.

2. Attach the A6 power supply assembly to the spectrum analyzer chassis and top shield wall using the four screws.

3. Connect W1 to A6J1, W3 to A6J2, fan power wires to A6J3, W8 to A6J4, and the line-power jack to A6J101. See Figure 4-17 on page 200.

4. Secure the A6A1 high voltage assembly to the A6 power supply assembly, using three TORX screws. Connect ribbon cable A6A1W1 to A6J5.

5. Snap post-accelerator cable A6A1W3 to the CRT assembly.

Figure 4-17   A6 Power Supply Connections
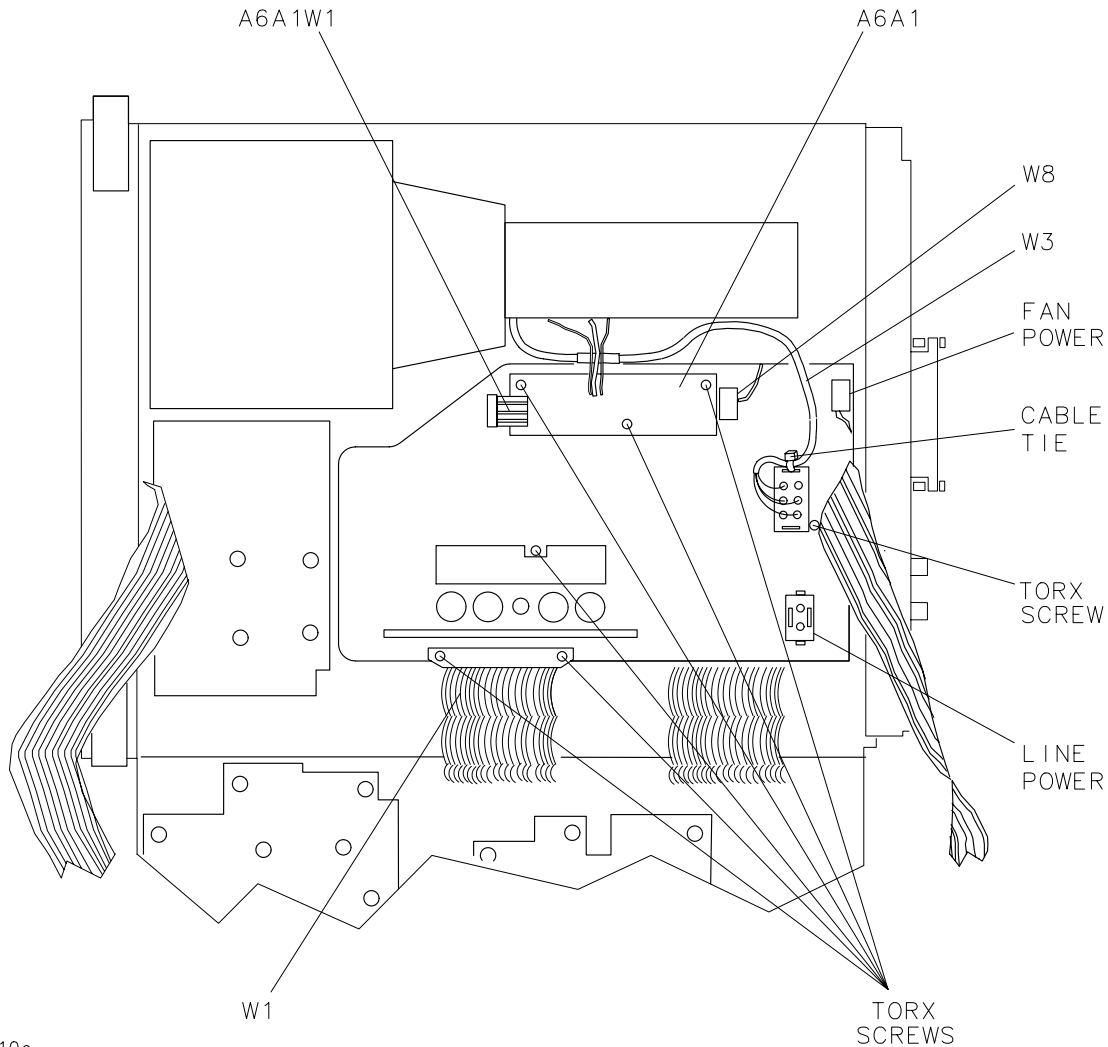
6. Ensure that all cables are safely routed and will not be damaged when securing the A6 cover.

7. Secure the power supply cover shield to the power supply using three flathead screws (1). See Figure 4-18 on page 201. One end of the cover fits into a slot provided in the rear frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove.

8. Fold the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 6 through 12.

Figure 4-18   Power Supply Cover
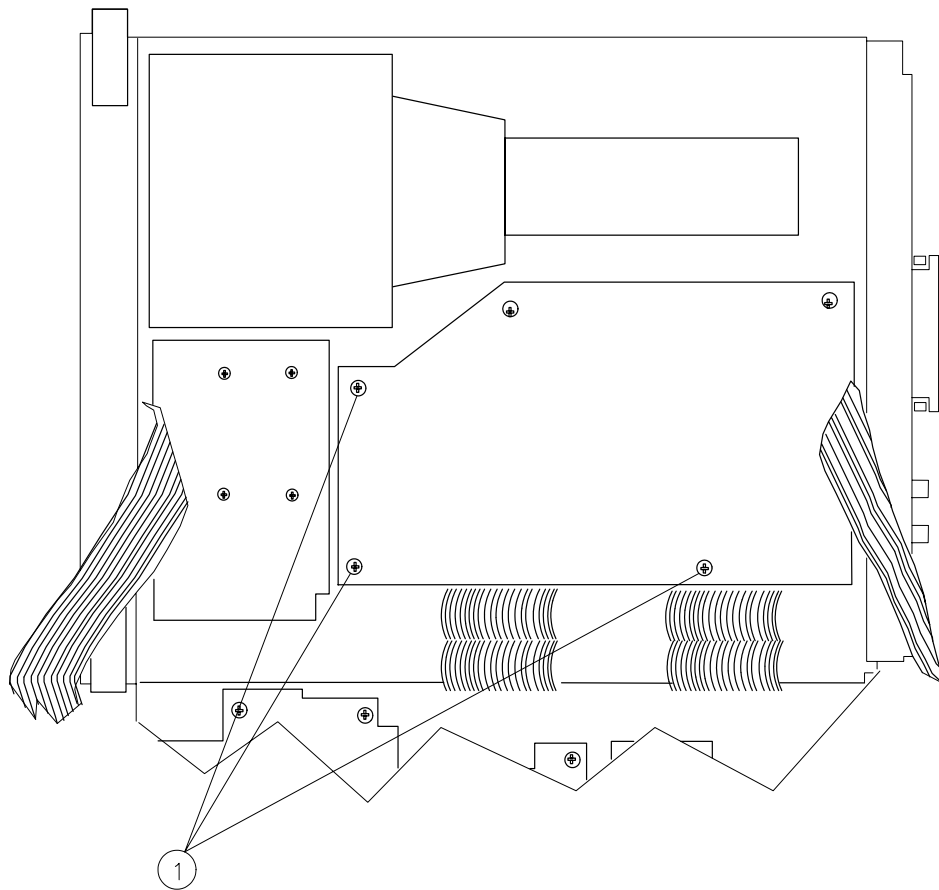
SP14E

Procedure 7. A6A1 High Voltage Assembly (8562E only)

Removal

<table>
<tr><td>WARNING</td><td>**The A6 power supply and A6A1 high voltage assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before beginning this replacement procedure. Failure to follow this precaution can represent a shock hazard which may result in personal injury.**</td></tr>
</table>

1. Disconnect the power cord from the spectrum analyzer.

2. Remove the spectrum analyzer cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165.

3. Fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

4. Place the spectrum analyzer top-side-up on the work bench.

<table>
<tr><td>WARNING</td><td>**The voltage potential at A6A1W3 is +9 kV. Disconnect at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument.**</td></tr>
</table>

5. Connect the spectrum analyzer line-power cord to provide proper grounding while discharging the A6A1W3 post-accelerator cable. Make sure that the spectrum analyzer line-power switch is in the off position.

6. Connect a high voltage probe (1000:1), such as the 34111A to a voltmeter with a 10 megohm input.

7. Connect the clip lead of the probe (ground) to the chassis of the spectrum analyzer.

8. Slip the tip of the high voltage probe under the rubber shroud of the A6A1W3 post-accelerator cable to obtain a reading on the voltmeter. See Figure 4-3 on page 179.

9. Keep the high voltage probe on the post-accelerator connector until the voltage has dropped to a voltmeter reading of less than 5 mV (less than 5 V at the connector). This normally takes about 30 seconds.

10. Disconnect the line-power cord from the spectrum analyzer.

11. Using a small screwdriver with the shank in contact with the CRT shield assembly, slip the tip of the screwdriver under the rubber shroud of the A6A1W3 post-accelerator cable and short the cable to ground on the CRT shield assembly. See Figure 4-3 on page 179.

12. Pry out the black grommet protecting post-accelerator cable A6A1W3 from the CRT shield assembly.

13. Carefully unsnap the A6A1W3 post-accelerator cable from the CRT and discharge it by shorting the cable to chassis ground on the CRT shield assembly.

14. Remove the three screws securing the power supply shield to the power supply and remove the shield.

15. Remove the three screws securing the A6A1 high voltage assembly to the A6 power supply assembly.

16. Disconnect ribbon cable A6A1W1 from A6J5. See Figure 4-17 on page 200.

17. *For Option 007 spectrum analyzers:* Remove the two screws (1) securing two board-mounting posts to the left side frame and remove the posts. See Figure 4-19 on page 204.

18. Remove the two left side frame screws (2) securing the A17 assembly (and A16 assembly in Option 007). *For Option 007 spectrum analyzers:* Lift up the A16 FADC assembly and swing it out of the spectrum analyzer. Do not remove any cables.

19. Lift up the A17 CRT driver assembly and disconnect A6A1W2 from A17J6. Do not remove any other cables from the A17 assembly.

20. Disconnect the tie wraps from the A6A1 assembly cables and remove the A6A1 high voltage assembly from the spectrum analyzer.

Figure 4-19   A16 Fast ADC and A17 CRT Driver Mounting Screws

s l 1 1 5 e
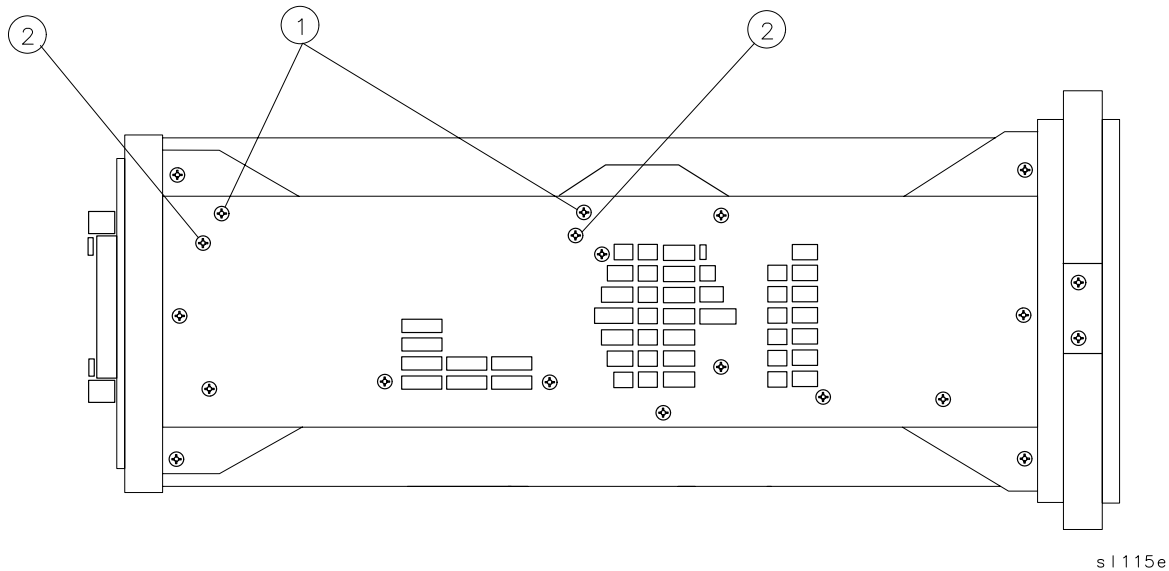
Replacement

1. Secure the A6A1 high voltage assembly to the A6 power supply using three panhead screws. Connect ribbon cable A6A1W1 to A6J5.

2. Snap post-accelerator cable A6A1W3 to the CRT assembly.

3. Place the black grommet protecting the post-accelerator cable into the CRT shield.

4. Ensure that all cables are safely routed and will not be damaged when securing the A6 cover.

5. Secure the power supply cover shield to the power supply using three flathead screws (1). See Figure 4-16 on page 197. One end of the cover fits into a slot provided in the rear frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove.

6. Connect A6A1W2 to A17J6.

7. Place the A17 CRT Driver assembly into the center-deck mounting slot nearest the CRT. Use caution when routing cables to avoid damage.

8. **For Option 007 spectrum analyzers:** Place the A16 FADC assembly into the center-deck mounting slot nearest the left side frame. Ensure that the A16 FADC assembly is properly seated in the right end of the slot.

9. Secure the A17 assembly (and A16 assembly in Option 007) with the two flathead screws removed in step 18 under "Removal." See Figure 4-19 on page 204 (2).

10. **For Option 007 spectrum analyzers:** Connect the two mounting posts to the left side frame using the two screws removed in step 17 under "Removal." See Figure 4-19 on page 204 (1).

11. Fold the A2, A3, A4, and A5 assemblies into the spectrum analyzer and secure the spectrum analyzer cover assembly as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

Procedure 8. A7 through A13 Assemblies

A separate replacement procedure is supplied for each assembly listed below. Before beginning a procedure, do the following:

Fold out the A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217.

If the A11 YTO or A10 assembly (SYTF or RYTHM) is being removed, also fold down the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

— A7 First LO Distribution Amplifier
— A8 Low Band Mixer
— A9 Input Attenuator
— A10 YIG-Tuned Filter/Mixer (RYTHM)
— A11 YTO
— A13 Second Converter

Figure 4-20 on page 207 illustrates the location of assemblies and major cable locations.

NOTE

Use a torque wrench to tighten all SMA connectors to 113 N-cm (10 in-lb). Part number 8710-1655 can be used for this purpose. The style of torque wrench may vary, but in all cases do not tighten the connectors beyond the point at which the torque wrench "clicks" or "breaks-away."

Figure 4-20   8562E/EC Assembly Locations
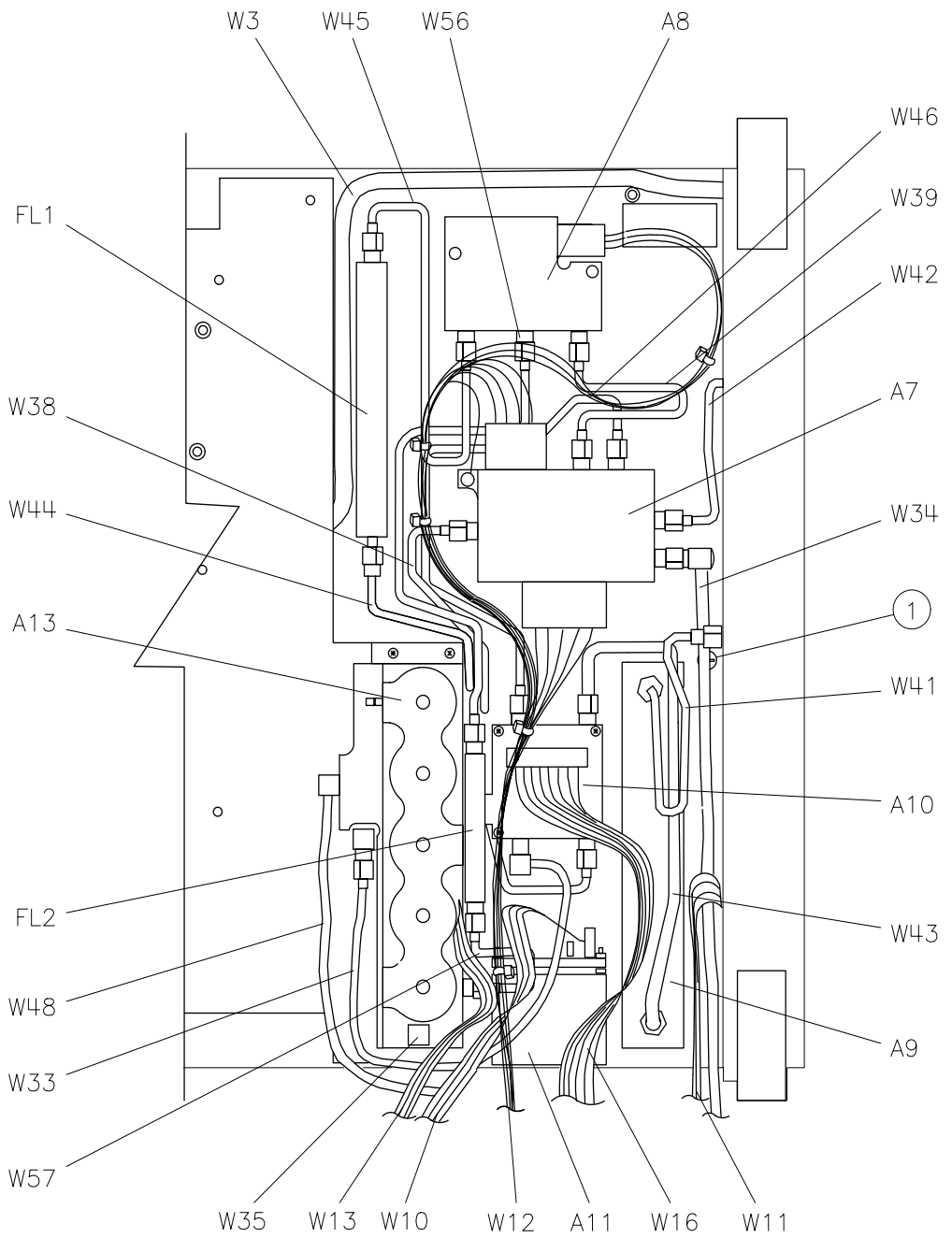
s l 1 1 e

A7 First LO Distribution Amplifier

Removal

1. Remove the two screws securing the assembly to the spectrum analyzer center deck.

2. Use a 5/16-inch wrench to disconnect W38 and W39 at A7J1 and A7J2.

3. Disconnect W46 at A7J3.

4. Disconnect W42 at the front panel First LO OUTPUT connector. Loosen W42 at A7J5.

5. Remove W12 from the A7 assembly.

6. Remove the assembly and disconnect W34.

Replacement

1. Use a 5/16-inch wrench to attach W34 to A7J4 and W42 to A7J5.

2. Connect W38 to A7J1 and connect W39 to A7J2.

3. Connect W46 to A7J3.

4. Connect W42 to the front panel First LO OUTPUT connector.

5. Connect cable W12 to the A7 assembly.

6. Use two panhead screws to secure A7 to the center deck. Be sure to attach the ground lug on the screw near the LO IN connector of A7.

7. Torque all RF cable connections to 113 N-cm (10 in-lb).

A8 Low Band Mixer

Removal

1. Place the spectrum analyzer upside-down on the work bench with A14 and A15 folded out to the left.

2. Use a 5/16-inch wrench to remove W45 from FL1 and A8J1.

3. Loosen W56 and W39 at A8J2, and A8J3.

4. Remove the two screws securing A8 to the center deck.

5. Remove W56 and W39 from the A8 assembly.

6. Disconnect W12 from A8.

Replacement

1. Place A8 on the center deck and attach W56 and W39, using caution to avoid damaging any of the cables' center conductor pins.

2. Use two panhead screws to secure A8 to the center deck. Reconnect W45 to FL1 and A8.

3. Tighten all semirigid coax connections on A8 and FL1; torque them to 113 N-cm (10 in-lb).

A9 Input Attenuator

Removal

1. Place the spectrum analyzer upside-down on the work bench.

2. Remove W41 and W43.

3. Disconnect W34 from A7 and move this cable out of the way.

4. Remove screw (1) securing the attenuator to the front frame center support. See Figure 4-20 on page 207.

5. Remove screw (1) securing the A9 input attenuator to the right side frame. See Figure 4-21 on page 211.

6. Remove the attenuator and disconnect the attenuator ribbon cable.

Replacement

1. Ensure that the bracket that secures the attenuator to the front frame center support is attached to the attenuator. The bracket should be on the same end as the ribbon cable connector.

2. Connect the attenuator-control ribbon cable to the A9 input attenuator.

3. Place the A9 input attenuator into the spectrum analyzer with the A9 mounting brackets resting against the front frame center support and the right side frame. Use caution to avoid damaging any cables.

4. Attach the attenuator to the center support with one panhead screw (1). See Figure 4-20 on page 207.

5. Attach the attenuator to the right side frame with one flathead screw (1). See Figure 4-21 on page 211.

6. Reconnect W34 to A7.

7. Connect semirigid cables W41 and W43 to A9, A10, and the RF input connector. Torque all SMA connections to 113 N-cm (10 in-lb).

Figure 4-21 A9 Mounting Screw at Right Side Frame
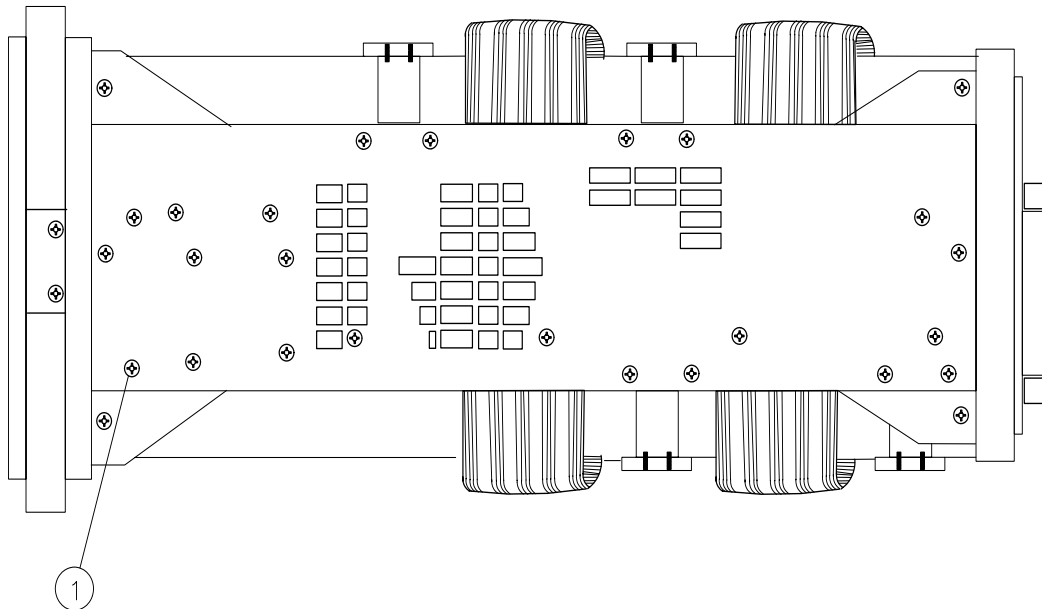
sl113e

A10 YIG-Tuned Filter/Mixer (RYTHM)

Removal

CAUTION   Do NOT remove the brackets from the A10 assembly. If these brackets are removed and reinstalled, the performance of A10 will be altered. A new or rebuilt A10 assembly includes new mounting brackets already attached to it.

1. Disconnect W16 ribbon cable from the A10 assembly.

2. Use a 5/16-inch wrench to remove W43, W44, and W46 from A10J3, J2, and J4, respectively.

3. Remove W56/FL2/W57 (as a unit) and disconnect W48 from A10J1.

4. Remove four screws (1) securing A10 to the center deck. These screws are located on the top-side of the center deck as illustrated in Figure 4-22 on page 212.

Figure 4-22   A10 Mounting Screws
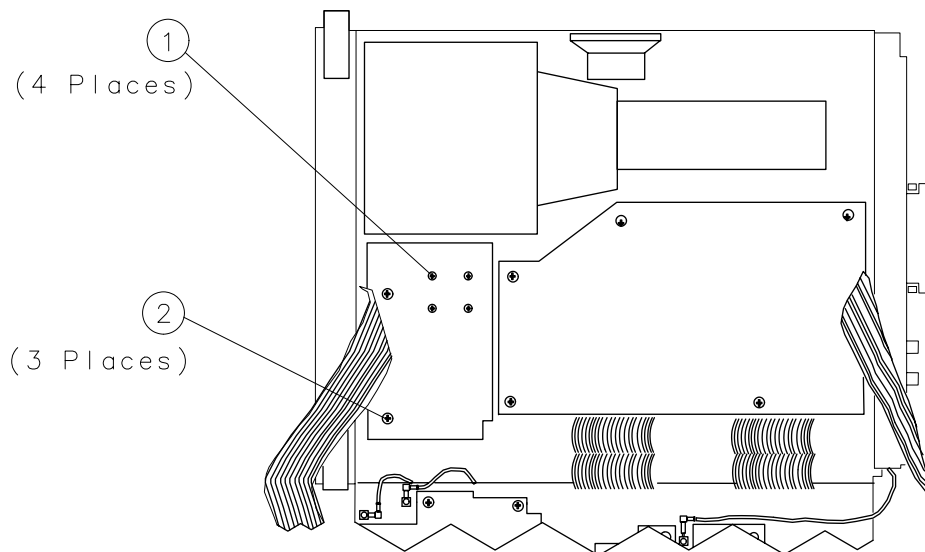
sl129e

Replacement

1. Orient the A10 assembly for the proper cable connections.

2. Connect W43, 44 and 46 to A10J3, J2, and J4, respectively.

3. Connect W48 (gray cable) to A10J1.

4. Connect W16 ribbon cable to the A10 assembly.

5. Install W56/FL2/W57 and ensure that all cable connections are tight. Torque them to 113 N-cm (10 in-lb).

6. Secure A10 to the spectrum analyzer center deck using four screws.

A11 YTO

Removal

1. Disconnect W16 ribbon cable from the A10 assembly and move it out of the way.

2. Remove W56/FL2/W57 (as a unit) and disconnect W38 at the A11 assembly.

3. Remove four screws (1) securing A11 to the right side frame. See Figure 4-23 on page 215. Remove the screws while holding onto A11.

4. Disconnect W10 ribbon cable from the A11 YTO assembly.

Replacement

1. Connect W10 ribbon cable to the A11 YTO assembly.

2. Orient the A11 assembly in the spectrum analyzer so its four mounting holes line up with the holes in the right side frame and the output connector is lined up with W38.

3. Secure the A11 assembly to the right side frame using four screws.

4. Connect W38 to A11.

5. Install W56/FL2/W57 between A8J2 and A13J1.

6. Reconnect W16 ribbon cable to the A10 assembly.

7. Torque all SMA connections to 113 N-cm (10 in-lb).

Figure 4-23   8562E/EC A11 Mounting Screws at Right Side Frame
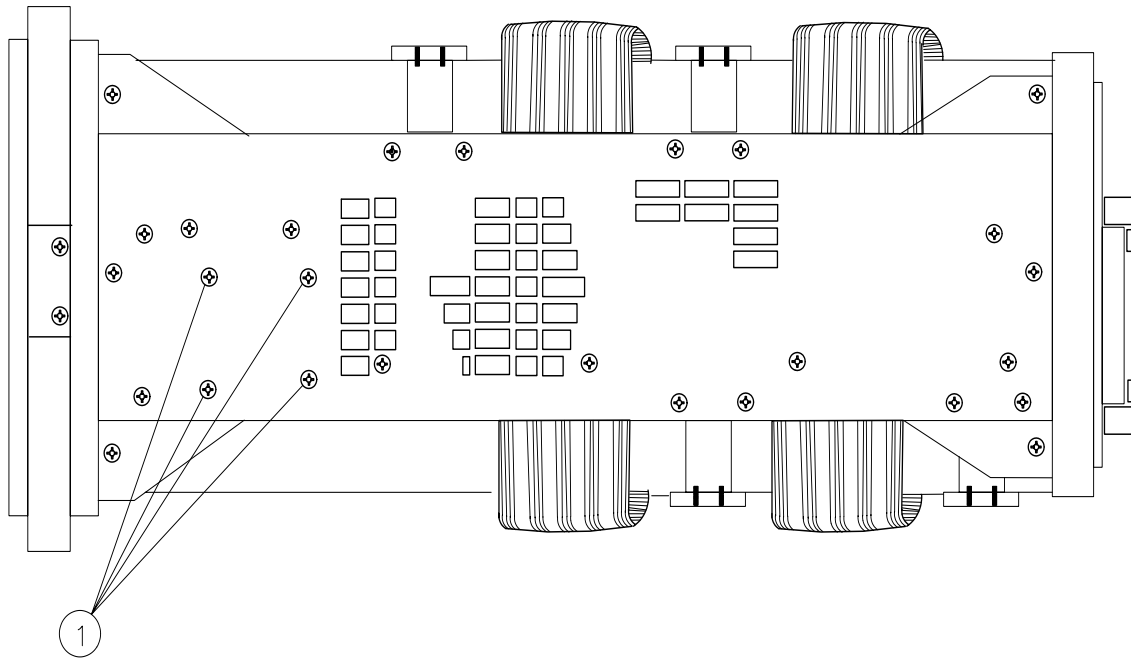
sl114e

A13 Second Converter

Turn off the spectrum analyzer power when replacing the A13 second converter assembly. Failure to turn off the power may result in damage to the assembly.

Removal

1. Place the spectrum analyzer upside-down on the work bench.

2. Disconnect W33, coax 81, and W35, coax 92, from the A13 assembly.

3. Disconnect W48, coax 8, from A13J3.

4. Disconnect W57 from A13J1.

5. Remove the four screws securing A13 to the main deck and remove the assembly.

6. Disconnect ribbon cable W13 from the A13 assembly.

Replacement

1. Connect ribbon cable W13 to the A13 assembly.

2. Secure A13 to the spectrum analyzer main deck, using four panhead screws.

3. Connect W33, coax 81, to A13J4 600 MHz IN jack.

4. Connect W35, coax 92, to A13J2 310.7 MHz OUT jack.

5. Connect W48, coax 8, to A13J3. Route W48 under W35, coax 92.

6. Connect W57 to A13J1. Ensure that all of the connections on W56/FL2/W57 and on W48 are torqued to 113 N-cm (10 in-lb).

Procedure 9. A14 and A15 Assemblies

Removal

1. Remove the spectrum analyzer cover as described in "Procedure 1. Spectrum Analyzer Cover" on page 165.

2. Place the spectrum analyzer on its right side frame.

3. Remove the eight screws (1) holding the A14 and A15 assemblies to the bottom of the spectrum analyzer. See Figure 4-24 on page 217.

Figure 4-24   A14 and A15 Assembly Removal
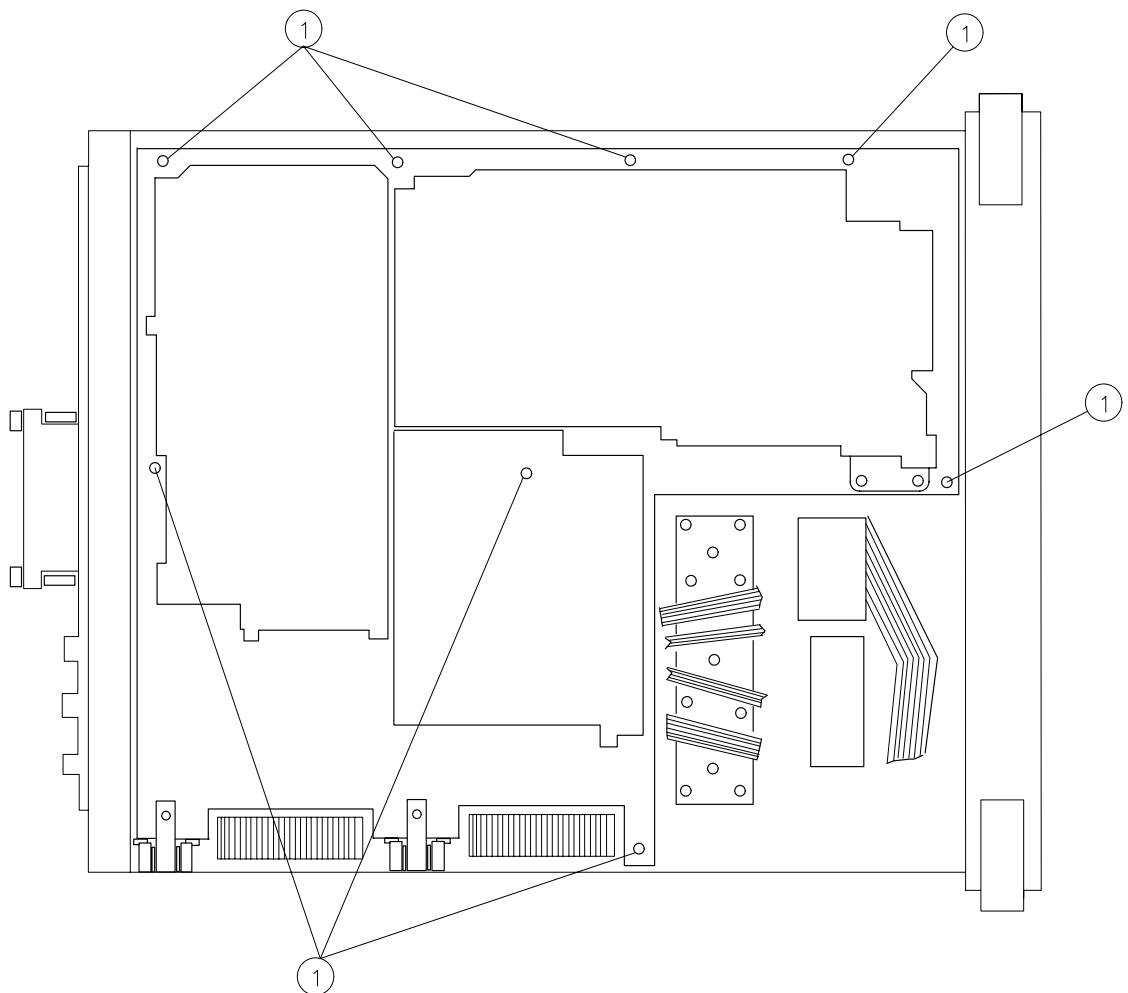
sl112e

CAUTION   Washers are not captive. Loose washers in instrument may cause internal damage.

CAUTION   DO NOT fold the board assemblies out of the spectrum analyzer one at a time. Always fold the A14 and A15 assemblies as a unit. Folding out one assembly at a time binds the hinges attaching the assemblies and may damage an assembly and hinge.

4. The board assemblies are attached to the right side frame of the spectrum analyzer with two hinges. Fold both the A14 and A15 assemblies out of the spectrum analyzer as a unit.

5. Remove all cables from the assembly being removed.

6. Remove the two screws that attach the assembly being removed to its two mounting hinges.

CAUTION   DO NOT torque shield screws to more than 5 inch-pounds. Applying excessive torque will cause the screws to stretch.

Replacement

1. Attach the removed assembly to the two chassis hinges with two panhead screws.

2. Attach all cables to the assembly as illustrated in Figure 4-25 on page 219. Torque the W34/A15 SMA connection to 113 N-cm (10 in-lb).

3. Lay the A14 and A15 assemblies flat against each other in the folded out position. Make sure that no cables become pinched between the two assemblies. Ensure that all coaxial cables are clear of hinges and standoffs before continuing onto the next step.

4. Fold both board assemblies into the spectrum analyzer as a unit. Use caution to avoid damaging any cable assemblies.

5. Secure the assemblies using the eight screws removed in "Removal" step 3. See Figure 4-24 on page 217.

6. Secure the spectrum analyzer cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165.

Figure 4-25   A14 and A15 Assembly Cables
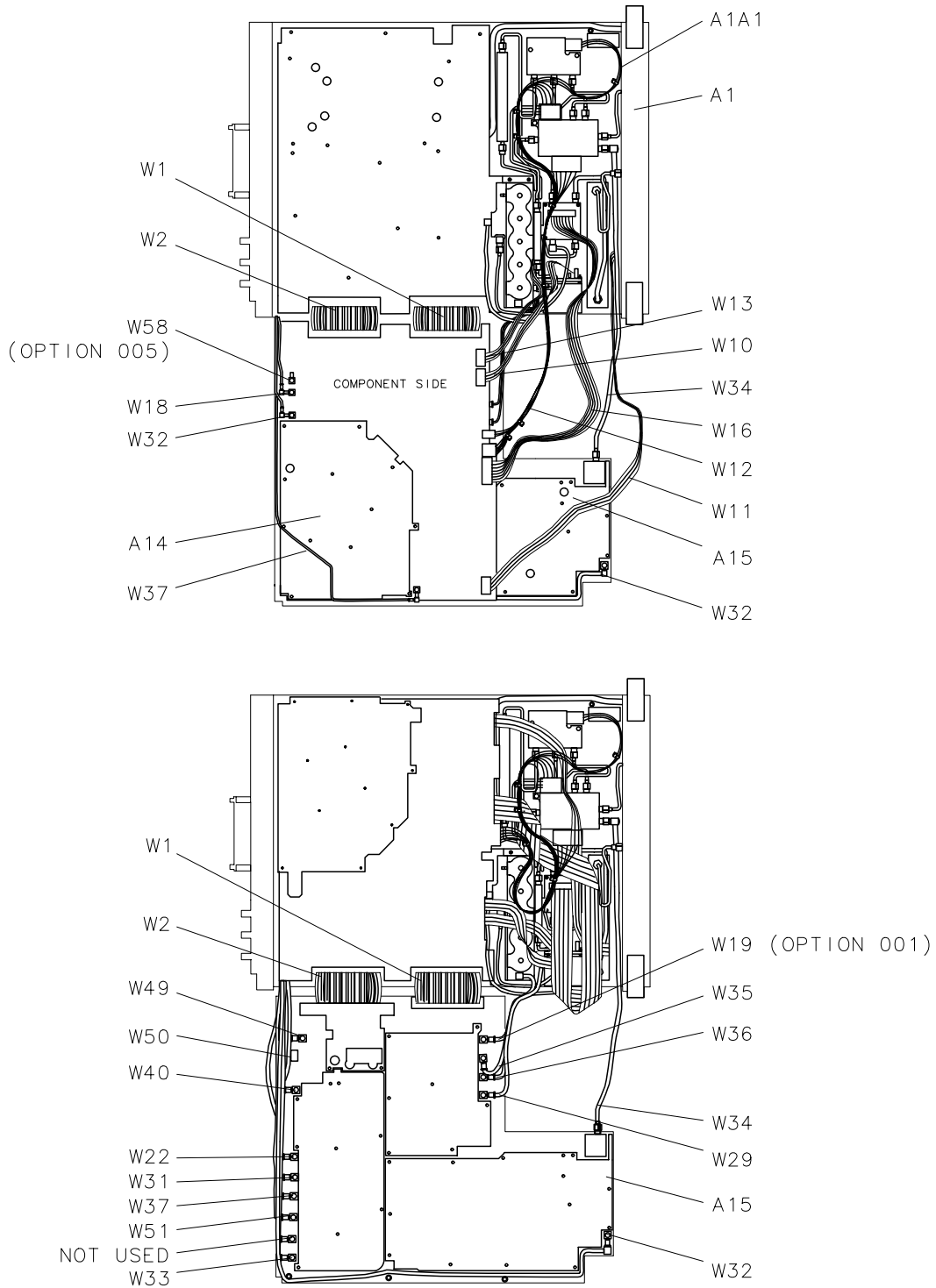
Procedure 10. A16 Fast ADC and A17 CRT Driver (8562E)

Removal

1. Remove the spectrum analyzer cover assembly and fold out the A2, A3, A4, and A5 assemblies as described in steps 3 through 6 under "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

2. Place the spectrum analyzer top-side-up on the work bench with A2, A3, A4, and A5 folded out to the right.

3. **For Option 007 spectrum analyzers:** Remove two screws (1) securing the two board-mounting posts to the left side frame, and remove the posts. See Figure 4-26 on page 221.

4. Remove two screws (2) securing the A17 assembly (and A16 assembly in Option 007) to the left side frame. Remove the two spacers (non-Option 007).

5. Pull the A17 assembly out of the spectrum analyzer.

6. **For Option 007 spectrum analyzers:** Pull the A16 assembly out of the spectrum analyzer.

7. Disconnect W7, W8, W9, A6A1W2, and A18W1 from the A17 CRT driver assembly.

8. **For Option 007 spectrum analyzers:** Disconnect all cables from the A16 Fast ADC assembly.

Figure 4-26   A16 and A17 Mounting Screws
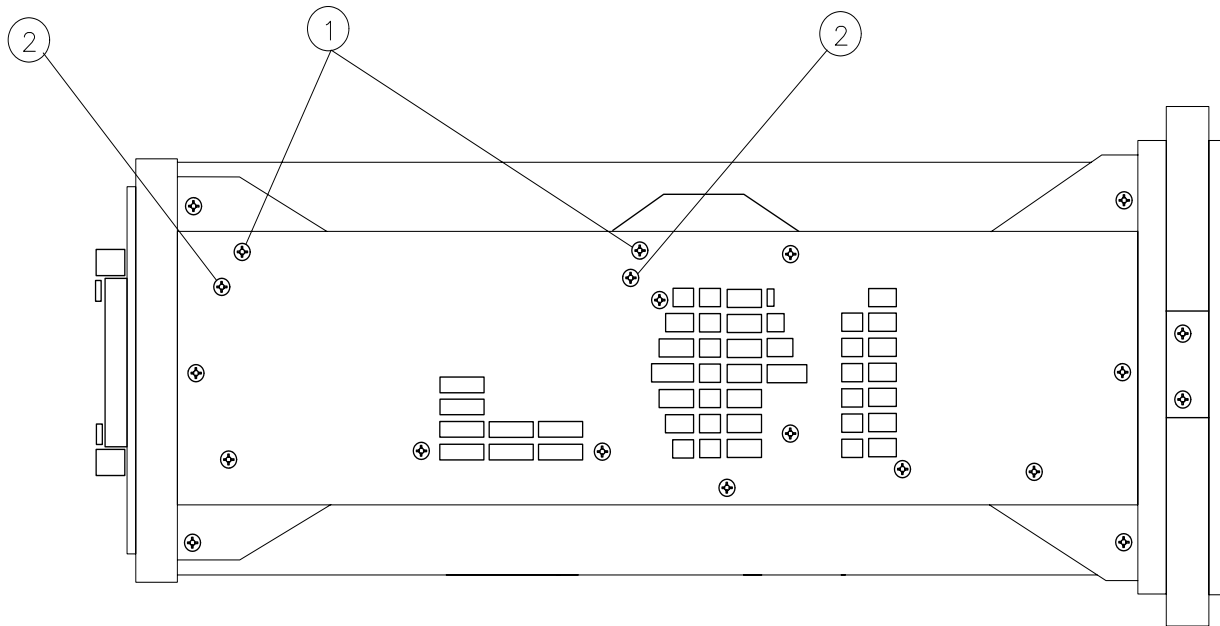
s l 1 1 5 e

Replacement

1. Connect W7, W8, W9, A6A1W2, and A18W1 to the A17 CRT driver assembly. Place the assembly into the center-deck mounting slot next to the CRT assembly.

2. *For Option 007 spectrum analyzers:* Connect all A16 assembly cables as illustrated in Figure 4-27 on page 222 which shows the left side frame removed so that proper A16 assembly cable routing may be viewed. Place the A16 assembly into the center-deck mounting slot nearest the left side frame.

3. Secure the A17 assembly (and A16 assembly in Option 007) to the left side frame using two flathead screws (and two spacers in non-Option 007). *For Option 007:* Attach the board mounts to the left side frame using two flathead screws (1). See Figure 4-26 on page 221.

4. Place the spectrum analyzer on its right side frame.

5. Fold the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188. Secure the spectrum analyzer cover assembly.

Figure 4-27   A16 Cable Routing

W20
COAX 6

W7

W59
COAX 839

W5
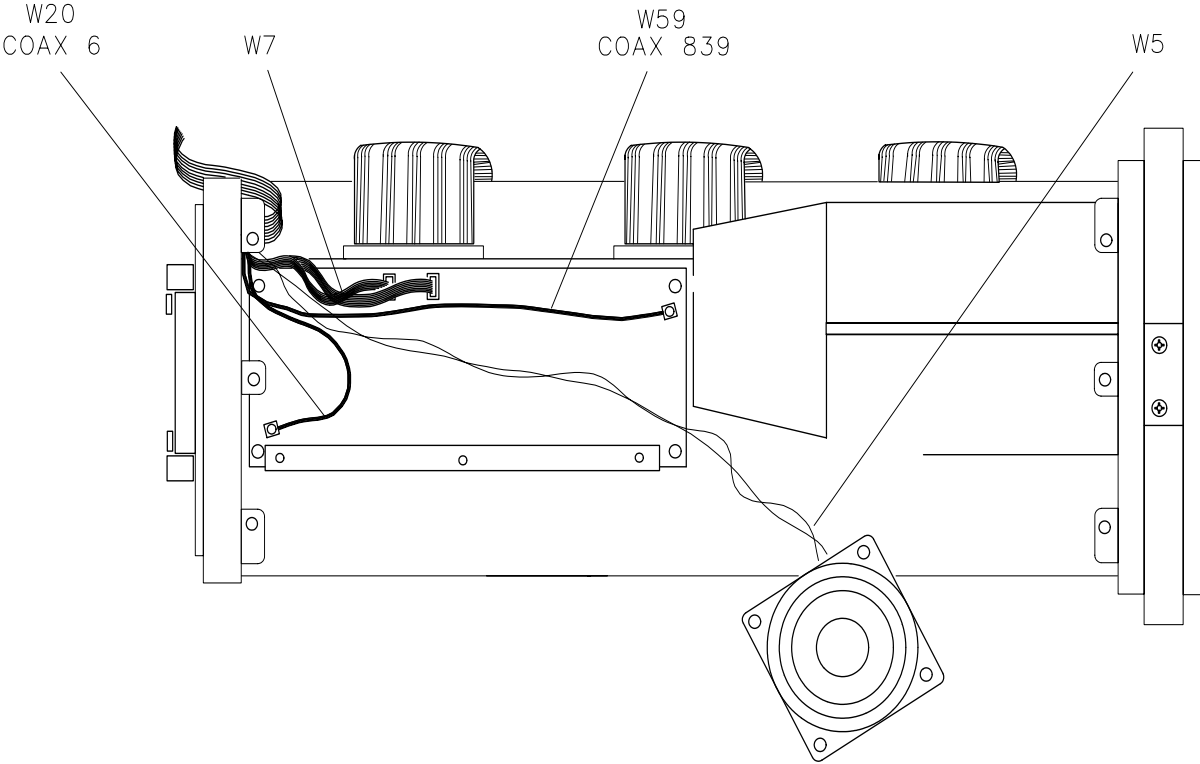
sj138e

Procedure 11. B1 Fan

Removal/Replacement

WARNING **Always disconnect the power cord from the instrument before beginning this replacement procedure. Failure to follow this precaution can present a shock hazard which may result in personal injury.**

1. Remove the four screws securing the fan assembly to the rear frame.

2. Remove the fan and disconnect the fan wire from the A6 power supply assembly.

3. To reinstall the fan, connect the fan wire to A6J3 and place the wire into the channel provided on the left side of the rear frame opening. Secure the fan to the rear frame using four panhead screws.

NOTE The fan must be installed so that the air enters through the front and sides of the instrument and exits out the rear of the instrument.

Procedure 12. BT1 Battery

WARNING   **Battery BT1 contains lithium polycarbon monofluoride. Do not incinerate or puncture this battery. Dispose of discharged battery in a safe manner.**

CAUTION   To avoid loss of the calibration constants stored on the A2 controller assembly, connect the spectrum analyzer to the main power source and turn on before removing the battery.

The battery used in this instrument is designed to last several years. An output voltage of +3.0 V is maintained for most of its useful life. Once this voltage drops to +2.6 V, its life and use are limited and the output voltage will deteriorate quickly. When the instrument is turned off, stored states and traces will only be retained for a short time and may be lost. Refer to "State- and Trace-Storage Problems" on page 522. The battery should be replaced if its voltage is +2.6 V or less.

Removal/Replacement

1. Remove any option module attached to the rear panel.

2. Locate the battery assembly cover on the spectrum analyzer rear panel. Use a screwdriver to remove the two flathead screws securing the cover to the spectrum analyzer.

3. Remove the old battery and replace it with the new one, ensuring proper polarity.

4. Measure the voltage across the new battery. Nominal new battery voltage is approximately +3.0 V. If this is not the case, check the battery cable and A2 controller assembly.

5. Secure the battery assembly into the spectrum analyzer.

Procedure 13. Rear Frame/Rear Dress Panel

Removal

WARNING **The A6 power supply (in E-series and EC-series instruments) and the A6A1 high voltage (in E-series instruments) assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before beginning this replacement procedure. Failure to follow this precaution can present a shock hazard which may result in personal injury.**

NOTE Diagrams that illustrate features common to E-series and EC-series instruments are shown with E-series instruments. Where features differ for E-series and EC-series instruments, separate diagrams are provided.

1. Disconnect the line-power cord from the spectrum analyzer.

2. Remove the spectrum analyzer cover, and place the spectrum analyzer on its right side frame.

3. Fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 3 through 5.

4. Disconnect the GPIB cable at A2J5.

5. Place the spectrum analyzer top-side-up on the work bench with A2 through A5 folded out to the right.

   For EC-series instruments, proceed to step 13. For E-series instruments proceed to step 6.

WARNING **The voltage potential at A6A1W3 is +9 kV. Disconnect at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument.**

6. Connect the spectrum analyzer line-power cord to provide proper grounding while discharging the A6A1W3 post-accelerator cable. Make sure that the spectrum analyzer line-power switch is in the off position.

7. Connect a high-voltage probe (1000:1), such as the 34111A to a voltmeter with a 10 megohm input.

8. Connect the clip lead of the probe (ground) to the chassis of the spectrum analyzer.

9. Slip the tip of the high-voltage probe under the A6A1W3 post-accelerator cable's rubber shroud to obtain a reading on the voltmeter. See Figure 4-3 on page 179.

10. Keep the high-voltage probe on the post-accelerator connector until the voltage has dropped to a voltmeter reading of less than 5 mV (less than 5 V at the connector). This normally takes about 30 seconds.

11. Disconnect the line-power cord from the spectrum analyzer.

12. Using a small screwdriver with the shank in contact with the CRT shield assembly, slip the tip of the screwdriver under the A6A1W3 post-accelerator cable's rubber shroud and short the cable to ground on the CRT shield assembly. See Figure 4-3 on page 179.

13. Remove the three screws securing the power-supply shield to the power supply, and remove the shield. See (1) in Figure 4-1 on page 165.

14. Disconnect the fan and line-power cables from A6J3 and A6J101 on the A6 power supply assembly.

15. Remove the two flathead screws that secure the rear-panel battery assembly, and remove the assembly. Remove the battery and unsolder the two wires attached to the battery assembly.

16. Use a 9/16-inch nut driver to remove the dress nuts holding the BNC connectors to the rear frame. If necessary, drill out the nut driver to fit over the BNC connectors, and cover it with heatshrink tubing or tape to avoid scratching the dress panel.

17. Remove four screws that secure the rear frame to the main deck. See (1) in Figure 4-28 on page 227.

18. Remove the six screws that secure the rear frame to the left and right side frames.

19. Remove the knurled nut that secures the earphone jack. Carefully remove the jack using caution to avoid losing the lock washer located on the inside of the rear-frame assembly. Replace the washer and nut onto the jack for safekeeping.

20. Remove the rear-frame assembly.

21. To remove the rear dress panel, remove the two nuts located on the inside of the rear frame near the display adjustment holes.

Figure 4-28   Main Deck Screws
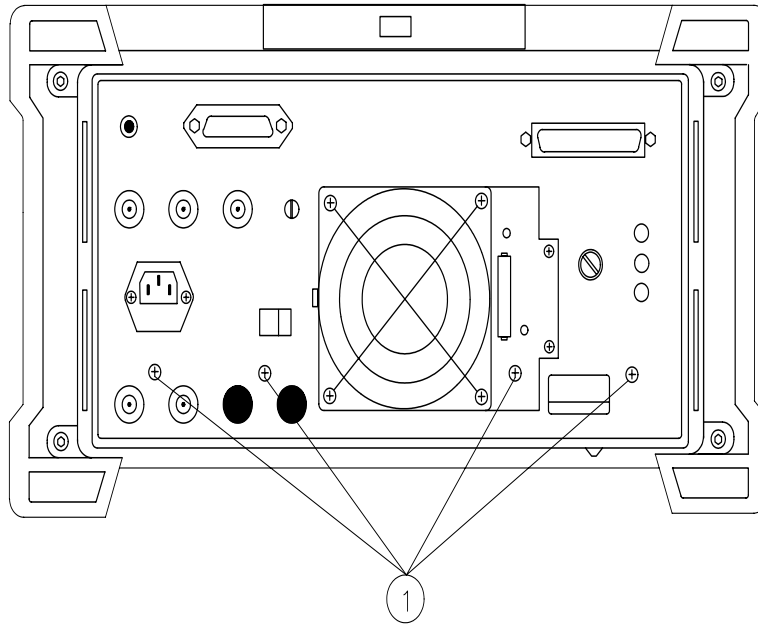
SK147

Replacement

1. If the rear dress panel is removed, secure it to the rear frame using two nuts. Ensure that the dress panel is aligned with the frame.

2. Place the spectrum analyzer on its front panel allowing easy access to the rear-frame area.

3. Place the rear frame on the spectrum analyzer and secure the knurled nut on the earphone jack. A lock washer should be used on the inside of the rear frame and a flat washer on the outside.

4. Place the coax cable's BNC connectors into the appropriate rear-frame holes as described below. Use a 9/16-inch nut driver to attach the dress nuts holding the BNC connectors to the rear frame.

Rear Panel Jack		
EC-series	**E-series**	**RF Cable**
J1	n/a	W64
n/a	J1	W55
J4	J4	W24, coax 5
J5	J5	W23, coax 93
J6	J6	W25, coax 4
J7	n/a	W55
J8	J8	W18, coax 97
J9	J9	W31, coax 8
J11	J11	W58, coax 8

5. Secure the rear frame to the spectrum analyzer main deck, using four panhead screws (1). See Figure 4-28 on page 227.

6. Secure the rear frame to the spectrum analyzer side frames using three flathead screws per side. Use caution to avoid damaging any coaxial cables.

7. Place the spectrum analyzer top-side-up on the work bench.

8. Pull the red and black battery wires through the rear-frame's battery-assembly hole. Solder the red wire to the battery-assembly's positive lug and the black wire to the negative lug. Replace the battery.

9. Secure the battery assembly to the rear frame, using two flathead screws.

10. Connect the fan and line-power cables to A6J3 and A6J101 on the A6 power supply.

    For EC-series instruments, proceed to step 13. For E-series instruments proceed to step 11.

11. Snap the A6A1W3 post-accelerator cable to the CRT assembly.

12. Snap the black grommet protecting A6A1W3 into the CRT shield.

13. Ensure that all cables are safely routed and will not be damaged when securing the A6 cover.

14. Secure the power-supply cover shield to the power supply, using three flathead screws (1). One end of the cover fits into a slot provided in the rear-frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove. See Figure 4-29 on page 229.

15. Connect the GPIB cable to A2J5.

16. Fold the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188.

Figure 4-29   A6 Power Supply Cover
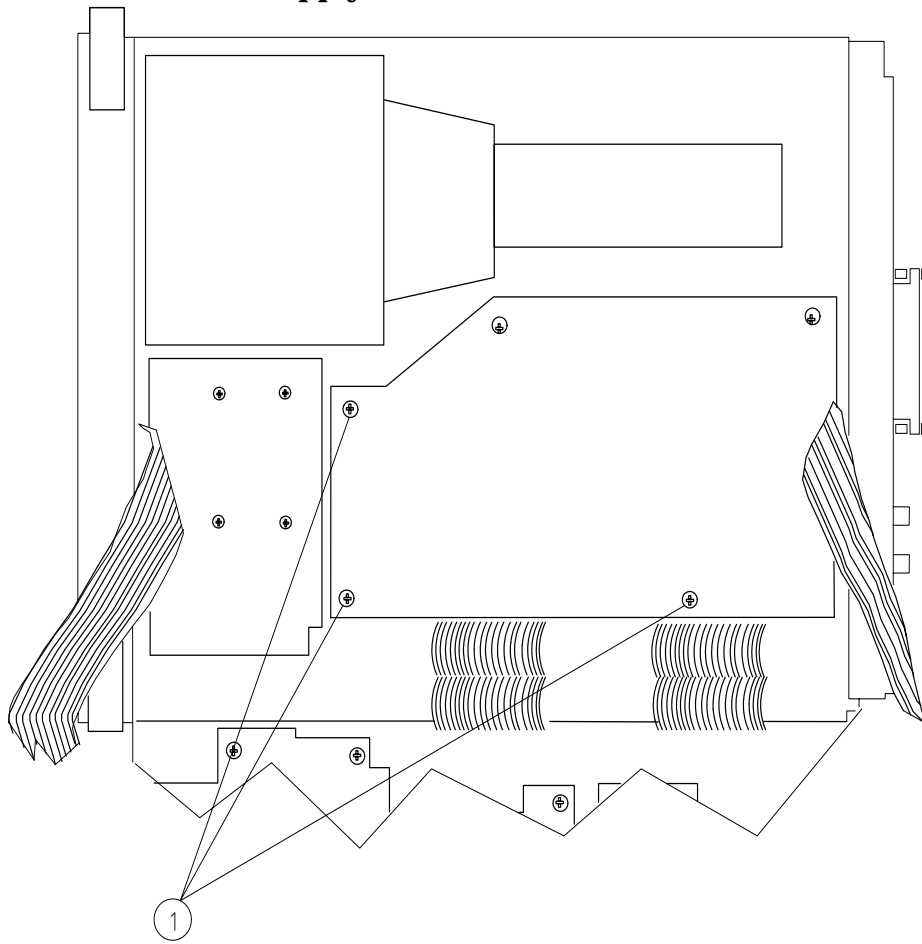
SP14E

Procedure 14. W3 Line Switch Cable (8562E)

See "Removal of the Line Switch from the Front Panel" on page 169 for the line switch removal procedure for 8562EC instruments.

Removal

WARNING   **Due to possible contact with high voltages, disconnect the spectrum analyzer line-power cord before performing this procedure.**

1. Remove the spectrum analyzer cover assembly as described in "Procedure 1. Spectrum Analyzer Cover" on page 165.

2. Fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 3 through 5.

3. Disconnect A1A1W1 from A3J602.

4. Place the spectrum analyzer top-side-up on the work bench with A2 through A5 folded out to the right.

WARNING   **The voltage potential at A6A1W3 is +9 kV. Disconnect at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument.**

5. Connect the spectrum analyzer line-power cord to provide proper grounding while discharging the A6A1W3 post-accelerator cable. Make sure that the spectrum analyzer line-power switch is in the off position.

6. Connect a high voltage probe (1000:1), such as the 34111A to a voltmeter with a 10 megohm input.

7. Connect the clip lead of the probe (ground) to the chassis of the spectrum analyzer.

8. Slip the tip of the high voltage probe under the rubber shroud of the A6A1W3 post-accelerator cable to obtain a reading on the voltmeter. See Figure 4-3 on page 179.

9. Keep the high voltage probe on the post-accelerator connector until the voltage has dropped to a voltmeter reading of less than 5 mV (less than 5 V at the connector). This normally takes about 30 seconds.

10. Disconnect the line-power cord from the spectrum analyzer.

11. Using a small screwdriver with the shank in contact with the CRT shield assembly, slip the tip of the screwdriver under the rubber shroud of the A6A1W3 post-accelerator cable and short the cable to ground on the CRT shield assembly. See Figure 4-3 on page 179.

12. Remove the three screws securing the power supply shield to the power supply, and remove the shield.

13. Pull the cable tie (1), Figure 4-30 on page 232, to free W9 and the post-accelerator cables.

14. Disconnect W3 from A6J2.

15. Pull W3 up from between the power supply and the CRT assembly to release it from the cable clamp.

16. Place the spectrum analyzer on its right side frame.

17. Fold out the A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217 steps 3 and 4.

18. Loosen the screw (1) securing W3, the line switch assembly, to the front frame. The screw is captive. See Figure 4-31 on page 234.

Figure 4-30   W3 Dress and Connection to A6 Power Supply
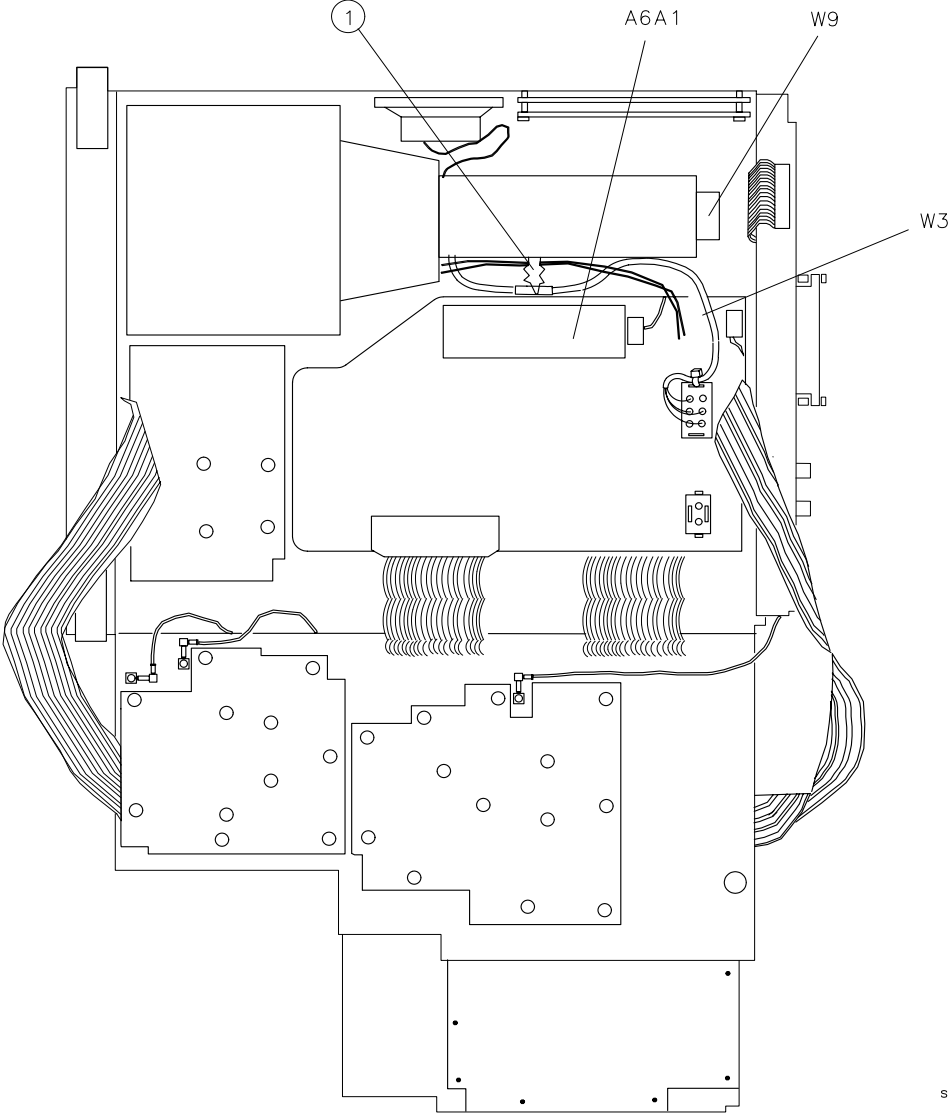
sl111e

19.Remove A1W1 and A1W1DS1 from the line-switch assembly. Let each hang freely.

NOTE

If contact removal tool, part number 8710-1791, is available, complete assembly removal by performing "Removal," steps 20 and 21. If not, skip to "Removal," step 22.

20.With wire cutters, clip the tie wrap holding the cable to the contact housing. From the top side of the spectrum analyzer, use contact removal tool, Part Number 8710-1791, to remove the four wires from the W3 connector. See Figure 4-32 on page 235.

21.Completely remove the cable from the instrument.

NOTE

If steps 20 and 21 have been performed, stop the procedure here; do not perform steps 22, 23, and 24.

22.Remove the A1 front frame assembly and A18 CRT assembly as described in "Procedure 2B. A1 Front Frame/A18 CRT (8562E)" on page 177 steps 16 through 29.

23.Remove the left side frame from the spectrum analyzer using the hardware listed below. (The side frame will still be attached by the speaker wires. Do not let it hang freely.)

Screw   **Quantity**
(1) SCREW-MACH M4 X 0.7 8 mm-LG FLAT HD 3
(2) SCREW-MACH M3 X 0.5 35 mm-LG FLAT HD 2
(3) SCREW-MACH M3 X 0.5 6 mm-LG FLAT HD 6

24.Remove the line-switch cable assembly.

Figure 4-31   **Line-Switch Mounting Screw and Cable Dress**
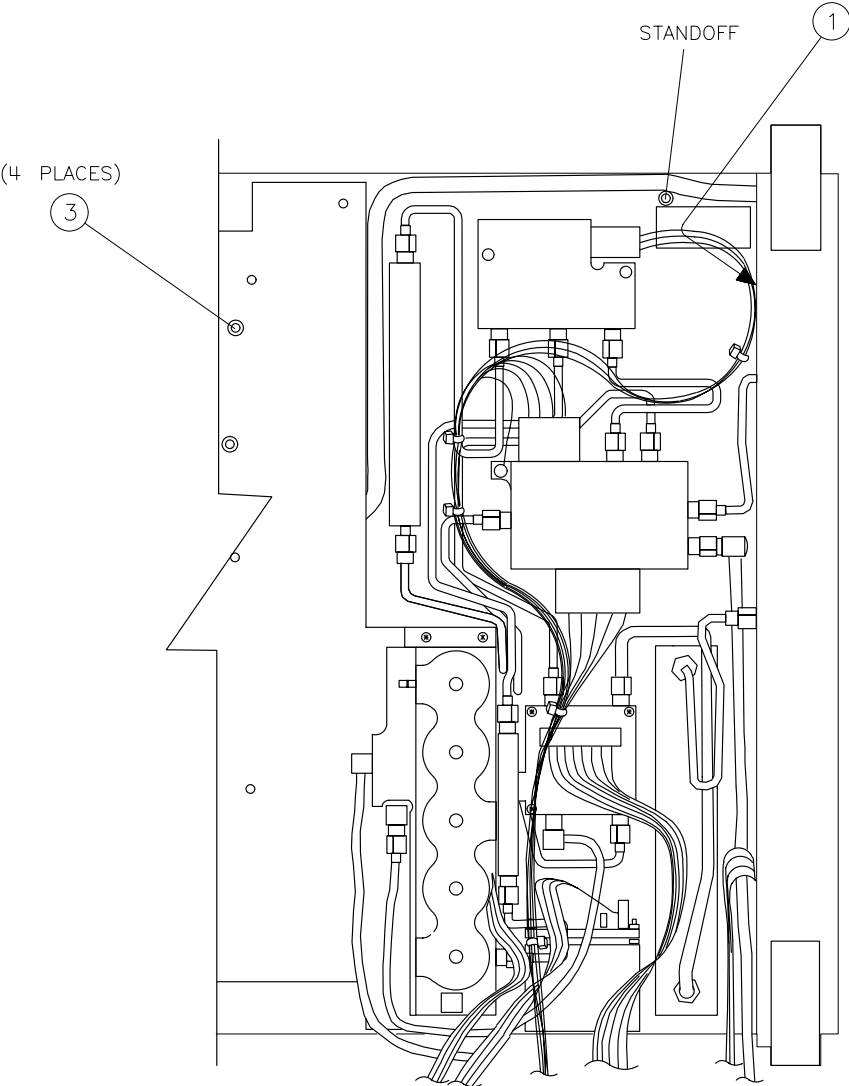
sl13e

Figure 4-32   W3 Cable Connector

CONNECTOR

POSITION OF
TIE WRAP KNUCKLE

WIRE (98)

WIRE (928)

WIRE (8)

WIRE (918)

PLUNGER PUSHES CONTACT OUT

CONNECTOR BODY

CONTACT REMOVAL TOOL
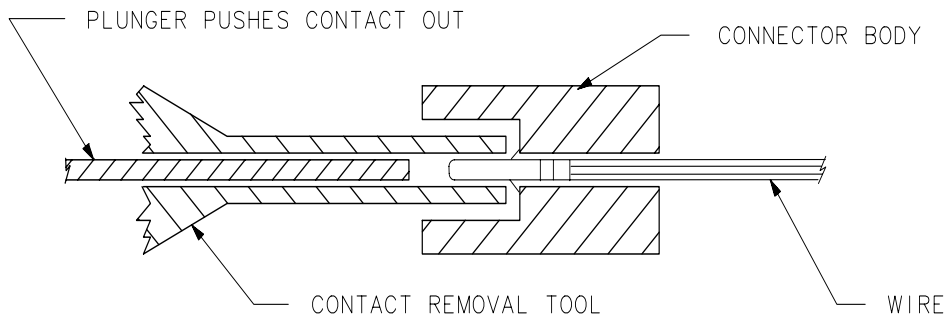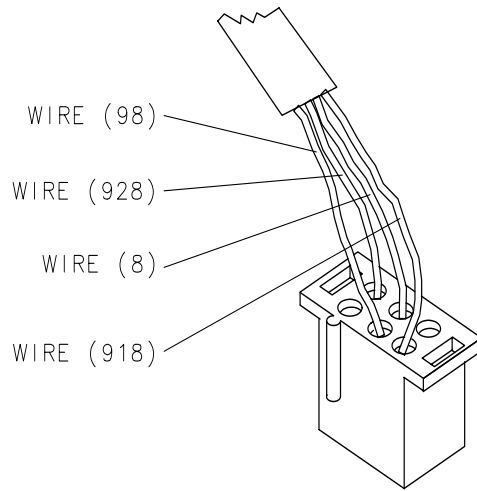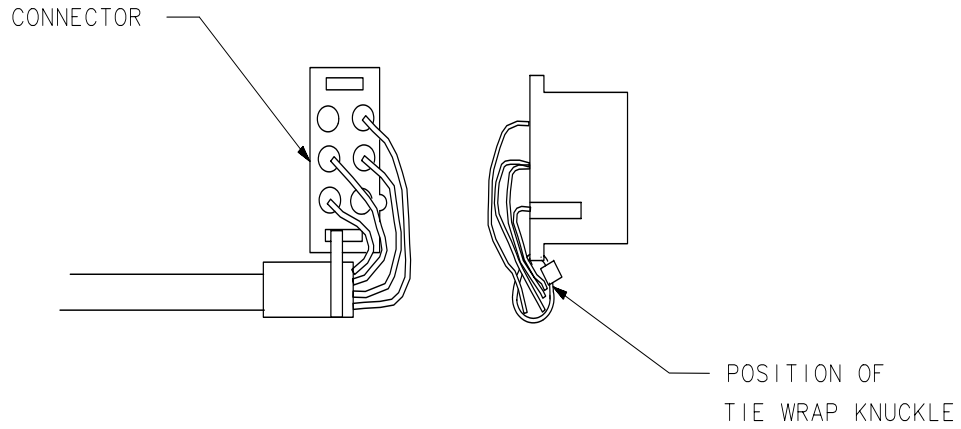
WIRE

SK151

Replacement (Using Contact Removal Tool, part number 8710-1791)

1. Ensure that the action of the switch is working properly. With a pair of wire cutters, clip the tie wrap holding the cable to the contact housing of the replacement W3 assembly.

2. Using the contact removal tool, remove the four wires from the replacement cable assembly connector.

3. From the bottom side of the spectrum analyzer, insert the contact end of W3 through the slotted opening in the main deck. W3 should come through to the top side of the spectrum analyzer between the A18 CRT assembly and the post-accelerator cable.

4. Place LED A1W1DS1 into the line-switch assembly.

5. Attach the line-switch assembly into the front frame, using the captive panhead screw. Ensure the connection of the line-switch grounding lug to the screw.

6. Dress W3 between the main deck standoff and the side frame. See Figure 4-31 on page 234.

7. On the top side of the spectrum analyzer, redress W3.

8. Insert the four contacts into the W3 connector.

9. Attach the cable to the connector housing using the supplied tie wrap.

10. Connect W3 to A6J2. Dress W3 into the slotted opening in the deck.

11. Connect A1A1W1 to A3J602.

12. Secure the power-supply cover shield to the power supply, using three flathead screws. One end of the cover fits into a slot provided in the rear frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove.

13. Redress W3 and the other cable assemblies down between the CRT assembly and the power supply cover such that the W9 wires are below the surface of the power-supply cover.

14. Fold up the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 5 through 10.

15. Fold up A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217 steps 9 through 11.

Replacement (without Contact Removal Tool)

1. Lay the replacement line-switch cable assembly between the side frame and main deck. Ensure that the action of the switch is working properly.

2. Attach the left side frame to the deck and rear frame. See Figure 4-33 on page 237.

   Screw   **Quantity**
   (1) SCREW-MACH M4 X 0.7 8 mm-LG FLAT HD 3
   (2) SCREW-MACH M3 X 0.5 35 mm-LG FLAT HD 2
   (3) SCREW-MACH M3 X 0.5 6 mm-LG FLAT HD 6

3. Dress W3 between the main deck standoff and the side frame. See Figure 4-31 on page 234.

4. Attach the A1 Front Frame assembly and the A18 CRT assembly as described in "Procedure 2B. A1 Front Frame/A18 CRT (8562E)" on page 177 steps 1 through 15.

5. Place LED A1W1DS1 into the line-switch assembly.

6. Attach the line-switch assembly into the front frame using the captive panhead screw. Be sure to connect the line-switch grounding lug with the screw.

Figure 4-33   **Side Frame Mounting Screws**
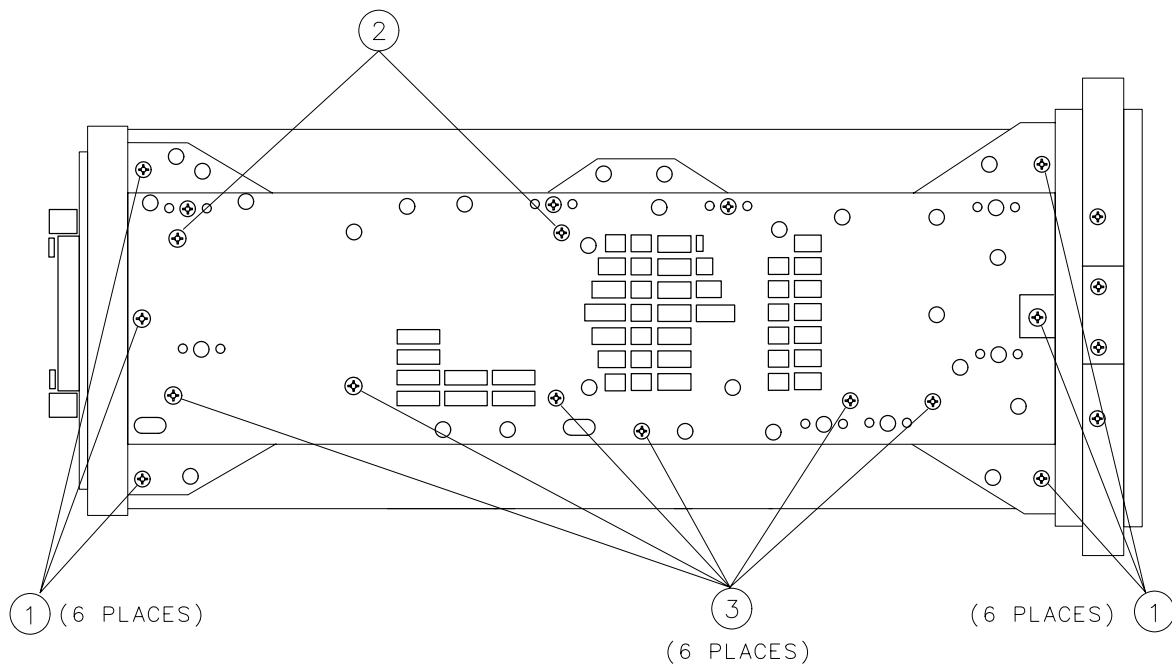
sm113e

7. On the top side of the spectrum analyzer, redress W3.

8. Connect W3 to A6J2. Dress W3 into the slotted opening in the deck.

9. Connect A1A1W1 to A3J602.

10. Secure the power-supply cover shield to the power supply using three flathead screws. One end of the cover fits into a slot provided in the rear frame assembly. Ensure that the extended portion of the cover shield is seated in the shield wall groove. See Figure 4-18 on page 201.

11. Place W3 and the other cable assemblies between the CRT assembly and the power supply cover so the W9 wires are below the surface of the power-supply cover.

12. Fold up the A2, A3, A4, and A5 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 5 through 10.

13. Fold up A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217 steps 3 through 5.

14. Replace the spectrum analyzer cover assembly.

15. Connect the line-power cord and switch the spectrum analyzer power on. If the spectrum analyzer does not operate properly, turn off the spectrum analyzer power, disconnect the line cord, and recheck the spectrum analyzer.

Procedure 15. EEROM

Removal/Replacement

CAUTION

The EEROM is replaced with the power on. Use a nonmetallic tool to remove the defective EEROM and install the new EEROM.

NOTE

In EC-series analyzers the EEROM reference designator is U23. In newer E-series analyzers the EEROM reference designator is U500. In older spectrum analyzers the EEROM reference designator is U501.

1. Turn the 8562E/EC **LINE** switch off. Remove the spectrum analyzer cover assembly and fold out the A2, A3, A4, and A5 assemblies as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188 steps 3 through 5.

2. Turn the 8562E/EC **LINE** switch on.

3. Set the WR PROT/WR ENA jumper on the A2 controller assembly to the WR ENA position.

4. Press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **COPY EEROM**. The spectrum analyzer will store the contents of the EEROM into the program RAM.

5. Using a nonmetallic tool, carefully remove the defective EEROM.

6. Carefully install a new EEROM.

7. Press **COPY TO EEROM**. The spectrum analyzer will store the contents of the program RAM into the new EEROM.

8. Turn the 8562E/EC **LINE** switch off, then on, cycling the spectrum analyzer power. Allow the power-on sequence to finish.

9. If error message 701, 702, or 703 is displayed, press **RECALL**, **MORE**, and **RECALL ERRORS**. Use the STEP keys to view any other errors.

10. If error message 701 or 703 is displayed, perform "9. Frequency Response Adjustment" on page 93. (If a TAM is available, perform the module "Low Band Flatness" and "High Band Flatness and YTF" adjustments. Press **MODULE**, **ADJUST** to enter the adjust menu of the TAM.)

11. If error message 704 is displayed, press **SAVE**, **SAVE PRSEL PK**, and **PRESET**.

12. If there are no errors after cycling the analyzer, the EEROM is working properly, but the frequency response correction data might be invalid. Check the spectrum analyzer frequency response.

13. Place the WR PROT/WR ENA jumper in the WR PROT position.

14. Fold the A2 and A3 assemblies into the spectrum analyzer as described in "Procedure 5. A2, A3, A4, and A5 Assemblies" on page 188. Secure the spectrum analyzer cover assembly.

Procedure 16. A21 OCXO

Removal

1. Remove the rear frame assembly as described in "Procedure 13. Rear Frame/Rear Dress Panel" on page 225 steps 1 through 20.

2. Place the spectrum analyzer on its right side frame.

3. Fold out the A14 and A15 assemblies as described in "Procedure 9. A14 and A15 Assemblies" on page 217 steps 3 and 4.

4. Remove the three screws (1) securing the OCXO to the main deck. See Figure 4-34 on page 242.

5. Disconnect W49, coax 82, from the OCXO and disconnect W50 (orange cable) from the A15 RF assembly. Clip the tie wraps that hold W49 and W50 together and remove the OCXO from the spectrum analyzer (with the orange cable connected).

Figure 4-34 **A21 OCXO Mounting Screws**
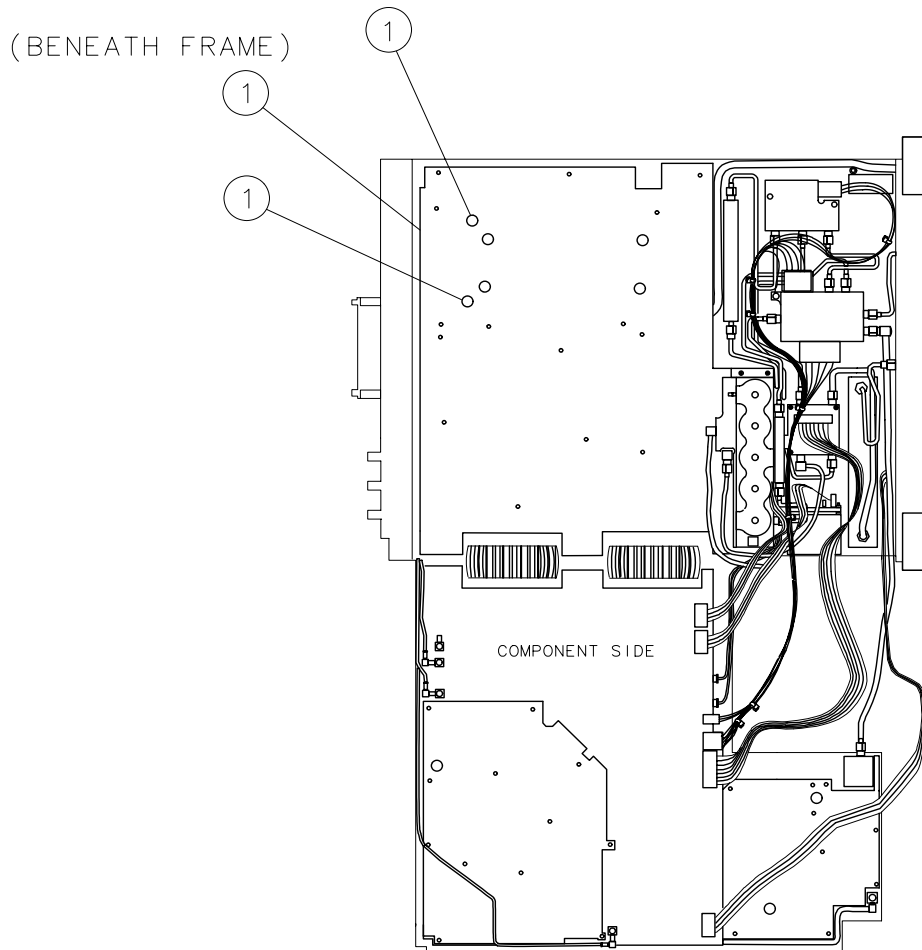
s l 16e

Replacement

1. Connect W49, coax 82, to the OCXO and position the OCXO in the spectrum analyzer. Dress W50, orange cable, next to W49 through the opening in the deck.

2. Secure the OCXO to the spectrum analyzer main deck using three screws (1). See Figure 4-34 on page 242.

3. Connect W50 to A15J306. Install tie wraps to hold W49 and W50 together.

4. Fold the A14 and A15 assemblies into the spectrum analyzer as described in "Procedure 9. A14 and A15 Assemblies" on page 217.

5. Perform the rear frame assembly replacement procedure described in "Procedure 13. Rear Frame/Rear Dress Panel" on page 225.

5 Replaceable Parts

Introduction

This chapter contains information on ordering all replaceable parts and assemblies. Locate the instrument parts in the following figures and tables:

Ordering Information

To order a part or assembly, quote the part number, indicate the quantity required, and address the order to the nearest Agilent Technologies office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, the description and function of the part, and the number of parts required. Address the order to the nearest Agilent Technologies office.

Direct Mail-Order System

Within the USA, Agilent Technologies can supply parts through a direct mail-order system. Advantages of using the system are as follows:

- Direct ordering and shipment from the Agilent Technologies Support Materials Organization in Roseville, California.

- No maximum or minimum on any mail order. (There is a minimum order amount for parts ordered through a local Agilent Technologies office when the orders require billing and invoicing.)

- Prepaid transportation. (There is handling charge for each order.)

- No invoices.

To provide these advantages, a check or money order must accompany each order. Mail-order forms and specific ordering information is available through your local Agilent Technologies Sales and Service office. See Table 1-6 on page 45.

Direct Phone-Order System

Within the USA, a phone order system is available for regular and hotline replacement parts service. A toll-free phone number is available, and Mastercard and Visa are accepted.

Regular Orders: The toll-free phone number, (800) 227-8164, is available 6 am to 5 pm, Pacific standard time, Monday through Friday. Regular orders have a four-day delivery time.

Hotline Orders: Hotline service for ordering emergency parts is available 24 hours a day, 365 days a year. There is an additional hotline charge to cover the cost of freight and special handling.

The toll-free phone number is (800) 227-8164, is available 6 am to 5 pm, Pacific standard time, Monday through Friday and (916) 785-8HOT for after hours, weekends, and holidays. Hotline orders are normally delivered the following business day.

Parts List Format

The following information is listed for each part:

1. The part number.
2. The total quantity (Qty) in the assembly. This quantity is given only once, at the first appearance of the part in the list.
3. The description of the part.
4. A five-digit code indicating a typical manufacturer of the part.
5. The manufacturer part number.

Firmware-Dependent Part Numbers

Refer to the firmware note entitled 8560 Series, 85620A, and 85629B Firmware Note, included with each 8560E-Series spectrum analyzer.

Table 5-1   **Reference Designations**

REFERENCE DESIGNATIONS					
A	Assembly	F	Fuse	RT	Thermistor
AT	Attenuator, Isolator, Limiter, Termination	FL	Filter	S	Switch
		HY	Circulator	T	Transformer
B	Fan, Motor	J	Electrical Connector (Stationary Portion), Jack	TB	Terminal Board
BT	Battery			TC	Thermocouple
C	Capacitor			TP	Test Point
CP	Coupler	K	Relay	U	Integrated Circuit, Microcircuit
CR	Diode, Diode Thyristor, Step Recovery Diode, Varactor	L	Coil, Inductor		
		M	Meter	V	Electron Tube
		MP	Miscellaneous Mechanical Part	VR	Breakdown Diode (Zener), Voltage Regulator
DC	Directional Coupler	P	Electrical Connector (Movable Portion), Plug		
DL	Delay Line			W	Cable, Wire, Jumper
DS	Annunciator, Lamp, Light Emitting Diode (LED), Signaling Device (Visible)			X	Socket
		Q	Silicon Controlled Rectifier (SCR), Transistor, Triode Thyristor	Y	Crystal Unit (Piezoelectric, Quartz)
				Z	Tuned Cavity, Tuned Circuit
E	Miscellaneous Electrical Part	R	Resistor		

Table 5-2 **Abbreviations**

ABBREVIATIONS						
A		**C**		CONT	Contact, Continuous, Control, Controller	
A	Across Flats, Acrylic, Air (Dry Method), Ampere	C	Capacitance, Capacitor, Center Tapped, Cermet, Cold Compression			
				CONV	Converter	
ADJ	Adjust, Adjustment			CPRSN	Compression	
ANSI	American National Standards Institute (formerly USASI-ASA)			CUP-PT	Cup Point	
		CCP	Carbon Composition Plastic	CW	Clockwise, Continuous Wave	
		CD	Cadmium, Card, Cord			
ASSY	Assembly			**D**		
AWG	American Wire Gage	CER	Ceramic			
		CHAM	Chamfer	D	Deep, Depletion, Depth, Diameter, Direct Current	
B		CHAR	Character, Characteristic, Charcoal			
BCD	Binary Coded Decimal			DA	Darlington	
				DAP-GL	Diallyl Phthalate Glass	
BD	Board, Bundle	CMOS	Complementary Metal Oxide Semiconductor			
BE-CU	Beryllium Copper			DBL	Double	
BNC	Type of Connector			DCDR	Decoder	
BRG	Bearing, Boring	CNDCT	Conducting, Conductive, Conductivity Conductor	DEG	Degree	
BRS	Brass			D-HOLE	D-Shaped Hole	
BSC	Basic			DIA	Diameter	
BTN	Button			DIP	Dual In-Line Package	

Table 5-2 **Abbreviations**

D		FDTHRU	Feedthrough	HEX	Hexadecimal, Hexagon, Hexagonal
DIP-SLDR	Dip Solder				
D-MODE	Depletion Mode	FEM	Female		
DO	Package Type Designation	FIL-HD	Fillister Head	HLCL	Helical
		FL	Flash, Flat, Fluid	HP	Hewlett-Packard Company, High Pass
DP	Deep, Depth, Diametric- Pitch, Dip	FLAT-PT	Flat Point		
		FR	Front		
DP3T	Double Pole Three Throw	FREQ	Frequency	I	
		FT	Current Gain Bandwidth Product (Transition Frequency), Feet, Foot	IN	Inch
DWL	Dowell			J	
				JFET	Junction Field Effect Transistor
E					
E-R	E-Ring	FXD	Fixed	K	
EXT	Extended, Extension, External, Extinguish				
		G		K	Kelvin, Key, Kilo, Potassium
F					
		GEN	General, Generator	KNRLD	Knurled
F	Fahrenheit, Farad, Female, Film (Resistor), Fixed, Flange, Frequency	GND	Ground	KVDC	Kilovolts Direct Current
		GP	General Purpose, Group		
		H		L	
FC	Carbon Film/ Composition, Edge of Cutoff Frequency, Face			LED	Light Emitting Diode
		H	Henry, High		
		HDW	Hardware	LG	Length, Long
		HEX	Hexadecimal,	LIN	Linear, Linearity

Table 5-2 **Abbreviations**

L		N		PC	Printed Circuit
LK	Link, Lock	N	Nano, None	PCB	Printed Circuit Board
LKG	Leakage, Locking	N-CHAN	N-Channel		
LUM	Luminous	NH	Nanohenry	P-CHAN	P-Channel
		NM	Nanometer, Nonmetallic	PD	Pad, Power Dissipation
M		NO	Normally Open, Number	PF	Picofarad, Power Factor
M	Male, Maximum, Mega, Mil, Milli, Mode	NOM	Nominal	PKG	Package
		NPN	Negative Positive Negative (Transistor)		
MA	Milliampere			PLSTC	Plastic
MACH	Machined	NS	Nanosecond, Non-Shorting, Nose	PNL	Panel
MAX	Maximum			PNP	Positive Negative Positive (Transistor)
MC	Molded Carbon	NUM	Numeric		
MET	Metal, Metallized	NYL	Nylon (Polyamide)	POLYC	Polycarbonate
MHz	Megahertz	O		POLYE	Polyester
MINTR	Miniature			POT	Potentiometer
MIT	Miter	OA	Over-All	POZI	Pozidriv Recess
MLD	Mold, Molded	OD	Outside Diameter	PREC	Precision
MM	Magnetized Material, Millimeter	OP AMP	Operational Amplifier	PRP	Purple, Purpose
				PSTN	Piston
MOM	Momentary	OPT	Optical, Option, Optional	PT	Part, Point, Pulse Time
MTG	Mounting				
MTLC	Metallic			PW	Pulse Width
SMA	Subminiature	P			
MW	Milliwatt				
		PA	Picoampere, Power Amplifier	Q	
		PAN-HD	Pan Head	Q	Figure of Merit

Table 5-2   Abbreviations

	R	SPST	Single Pole Single Throw	UF	Microfarad
R	Range, Red, Resistance, Resistor, Right, Ring			UH	Microhenry
		SQ	Square	UL	Microliter, Underwriters' Laboratories, Inc.
		SST	Stainless Steel		
REF	Reference	STL	Steel		
RES	Resistance, Resistor			UNHDND	Unhardened
RF	Radio Frequency	**T**		**V**	
RGD	Rigid				
RND	Round	T	Teeth, Temperature, Thickness, Time, Typical	V	Variable, Violet, Volt, Voltage
RR	Rear			VAC	Vacuum, Volts—Alternating Current
S					
SAWR	Surface Acoustic Wave Resonator				
		PB	Lead (Metal),	VAR	Variable
SEG	Segment	TA	Ambient Temperature, Tantalum	VDC	Volts—Direct Current
SGL	Single			**W**	
SI	Silicon, Square Inch	TC	Temperature Coefficient	W	Watt, Wattage, White, Wide, Width
SL	Slide, Slow				
SLT	Slot, Slotted	THD	Thread, Threaded	W/SW	With Switch
SMA	Subminiature A Type (Threaded Connector)	THK	Thick	WW	Wire Wound
		TO	Package Type Designation	**X**	
SMB	Subminiature B Type (Slip-on Connector)	TPG	Tapping	X	By (Used with Dimensions), Reactance
		TR-HD	Truss Head		
		TRMR	Trimmer		
SMC	Subminiature C-Type (Threaded Connector)	TRN	Turn, Turns	**Y**	
		TRSN	Torsion		
		U		YIG	Yttrium-Iron-Garnet
SPCG	Spacing			**Z**	
SPDT	Single Pole	UCD	Microcandela	ZNR	Zener

Table 5-3 Multipliers

MULTIPLIERS					
Abbreviation	**Prefix**	**Multiple**	**Abbreviation**	**Prefix**	**Multiple**
T	tera	10^{12}	m	milli	10^{-3}
G	giga	10^9	μ	micro	10^{-6}
M	mega	10^6	n	nano	10^{-9}
k	kilo	10^3	p	pico	10^{-12}
da	deka	10	f	femto	10^{-15}
d	deci	10^{-1}	a	atto	10^{-18}
c	centi	10^{-2}			

Manufacturers Code List

Refer to the Manufacturers Code List in the *8560 E-Series and EC-Series Spectrum Analyzer Component-Level Information*.

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
			ACCESSORIES SUPPLIED		
	1810-0118	1	TERMINATION-COAX SMA; 0.5W; 50Ω	16179	2003-6113-02
	1250-0780	1	ADAPTER-COAX F-BNC M-N	24931	29JP104-2
	10502A	1	50Ω COAX CABLE WITH BNC MALE	28480	10502A
	8710-1755	3	WRENCH-HEX KEY	55719	AWML4
			OPTION 908		
	5062-0800	1	RACK KIT WITH FLANGES		
			(Includes Parts Listed Below)		
	5001-8739	2	PANEL-DRESS	28480	5001-8739
	5001-8740	2	PANEL-SUB	28480	5001-8740
	5001-8742	2	SUPPORT-REAR	28480	5001-8742
	5021-5807	2	FRAME-FRONT	28480	5021-5807
	5021-5808	2	FRAME-REAR	28480	5021-5808
	5021-5836	5	CORNER-STRUT	28480	5021-5836
	0510-1148	10	RETAINER-PUSH-ON KB-TO-SHFT EXT	11591	669
	0515-0886	16	SCREW-MACH M3 × 0.5 6MM-LG PAN-HD	28480	0515-0886
	0515-0887	8	SCREW-MACH M3.5 × 0.6 6MM-LG PAN-HD	28480	0515-0887
	0515-0889	12	SCREW-MACH M3.5 × 0.6 6MM-LG	28480	0515-0889
	0515-1241	8	SCREW-MACH M5 × 0.8 12 MM-LG PAN-HD	28480	0515-1241
	0515-1331	22	SCREW-METRIC SPECIALTY M4 × 0.7 THD; 7MM	28480	0515-1331
	5061-9679	2	MOUNT FLANGE	28480	5061-9679
	0515-1114	6	SCREW-MACH M4 × 0.7 10MM-LG PAN-HD	28480	0515-1114
	8710-1755		WRENCH-HEX KEY	55719	AWML4
	5958-6573	2	ASSEMBLY INSTRUCTIONS	28480	5958-6573
			OPTION 909		
	5062-1900	1	RACK KIT WITH FLANGES AND HANDLES		
			(Includes Parts Listed Below)		
	5001-8739		PANEL-DRESS	28480	5001-8739
	5001-8740		PANEL-SUB	28480	5001-8740
	5001-8742		SUPPORT-REAR	28480	5001-8742
	5021-5807		FRAME-FRONT	28480	5021-5807
	5021-5808		FRAME-REAR	28480	5021-5808
	5021-5836		CORNER-STRUT	28480	5021-5836
	0510-1148		RETAINER-PUSH-ON KB-TO-SHFT EXT	11591	669
	0515-0886		SCREW-MACH M3 × 0.5 6MM-LG PAN-HD	28480	0515-0886
	0515-0887		SCREW-MACH M3.5 × 0.6 6MM-LG PAN-HD	28480	0515-0887
	0515-0889		SCREW-MACH M3.5 × 0.6 6MM-LG	28480	0515-0889
	0515-1241		SCREW-MACH M5 × 0.8 12MM-LG PAN-HD	28480	0515-1241
	0515-1331		SCREW-METRIC SPECIALTY M4 × 0.7 THD; 7MM	28480	0515-1331
	5061-9501	2	FRONT HANDLE ASS'Y	28480	5061-9501
	5061-9685	2	MOUNT FLANGE	28480	5061-9685

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
	0515-1106	6	SCREW-MACH M4 × 0.7 16MM-LG PAN-HD	28480	0515-1106
	8710-1755		WRENCH-HEX KEY	55719	AWML4
	5958-6573		ASSEMBLY INSTRUCTIONS	28480	5958-6573
			RACK SLIDE KIT		
	1494-0060	1	SLIDE-CHAS 25-IN-LG 21.84-IN-TRVL	01561	C858-2
			(Includes Parts Listed Below. Slides Cannot be Ordered Separately.)		
	0515-0949	4	SCREW-MACH M5 × 0.8 14MM-LG PAN-HD	28480	0515-0949
	0515-1013	9	SCREW-MACH M4 × 0.7 12MM-LG	28480	0515-1013
	0515-0909	4	SCREW-MACH M4 × 0.7 12MM-LG PAN-HD	28480	0515-0909
	0535-0080	8	NUT-CHANNEL M4 × 0.7 3.5MM-THK 10.3MM-WD	28480	0535-0080
			MAJOR ASSEMBLIES		
A1			FRONT FRAME ASSEMBLY (not available as a field replacement)		
(The A1 assembly includes the front frame, front faceplate, front-panel keys, and other hardware. Refer to Figure 5-5 on page 275 and Figure 5-8 on page 281 for individual part numbers.)					
A1A1	08563-60162	1	BD AY-KEYBOARD	28480	08563-60162
A1A1	08562-60140	1	BD AY-KEYBOARD	28480	08562-60140
A1A1W1	5062-8259	1	CABLE ASSEMBLY, RIBBON, KEYBOARD (A1A1J1 to A3J602)	28480	5062-8259
A1A2 for S/N ≤3632A00517	1290-1525	1	RPG ASSEMBLY (Includes Cable)	28480	1290-1525
A1A2 for S/N ≥3632A00518	0960-0745	1	RPG ASSEMBLY (Includes Cable)	28480	0960-0745
A1W1	8120-8153	1	CABLE ASSEMBLY PROBE POWER/LED	28480	8120-8153
A2 (8562EC)	08563-60160	1	CONTROLLER ASSEMBLY	28480	08563-60160
A2 (8562E)	08564-60010	1	CONTROLLER ASSEMBLY *	28480	08564-60010
A3	08563-60098	1	INTERFACE ASSEMBLY	28480	08563-60098
A4	08563-60076	1	LOG AMPLIFIER/CAL OSC. ASSY.*	28480	08563-60076
A5	08563-60023	1	IF FILTER ASSEMBLY	28480	08563-60023
A6	08564-60008	1	POWER SUPPLY ASSEMBLY* (Includes A6A2, does not include A6A1)	28480	08564-60008
A6A1	5062-7089	1	HIGH VOLTAGE ASSEMBLY	28480	5062-7089
A6A2	08564-60009	1	REGULATOR BOARD ASSEMBLY	28480	08564-60009
A7	5086-7885	1	SWITCHED LO DISTRIBUTION AMP	28480	5086-7885
	5086-6885		REBUILT A7, EXCHANGE REQUIRED	28480	5086-6885
A8	5086-7982	1	LOW BAND MIXER	28480	5086-7982
A9	5086-7822	1	PORT ATTENUATOR	28480	5086-7822
* These board assemblies are part of the rebuilt board exchange program. To order a rebuilt board, use the same number as that of the new board with the exception of the 7th digit which should be a 9. Example: New board number is 08562-60094. Therefore, the rebuilt board number will be 08562-69094.					

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
			MAJOR ASSEMBLIES (continued)		
A10	5086-7981	1	YIG-TUNED FILTER/MIXER (RYTHM)	28480	5086-7981
	5086-6981		REBUILT A10, EXCHANGE REQUIRED	28480	5086-6981
A11	5086-7906	1	PORTABLE LVLD YTO	28480	5086-7906
	5086-6906		REBUILT A11, EXCHANGE REQUIRED	28480	5086-6906
A13	5086-7959	1	SECOND CONVERTER	28480	5086-7959
A14	08563-60090	1	FREQUENCY CONTROL ASSEMBLY*	28480	08563-60090
A15 Standard	08563-60091	1	RF ASSEMBLY (STANDARD)*	28480	08563-60091
A15 Option103	08563-60092	1	RF ASSEMBLY (TCXO)*	28480	08563-60092
A15 Option008	08563-60093	1	RF ASSEMBLY (SIG ID)*	28480	08563-60093
A15 Option 103	08563-60092	1	RF ASSEMBLY (TCXO/SIG ID)*	28480	08563-60092
A15U100	5086-7806	1	SAMPLER	28480	5086-7806
A16 Option 007 (8562E)	08563-60030	1	FAST ADC ASSEMBLY	28480	08563-60030
A17 (8562EC)	08562-60161	1	LCD DRIVER	28480	08562-60161
A17A1 (8562EC)	0950-3644	1	LCD INVERTER BOARD	28480	0950-3644
A17 (8562E)	08563-60101	1	CRT ASSEMBLY	28480	08563-60101
A18 (8562EC)	08563-60170	1	LCD ASSEMBLY-Includes LCD, LCD MOUNT, LCD GLASS, and LCD BACKLIGHTS	28480	08563-60170
A18DS1 and A18DS2	2090-0380	1	Replaceable LCD Backlight Cartridge (part of LCD ASSEMBLY)	28480	2090-0380
A18 (8562E)		1	CRT ASSEMBLY (Order by Individual Parts)		
A18MP (8562E)	5062-7095	1	CRT WIRING ASSEM. (Includes Shield A18L1, and A18W1)	28480	5062-7095
A18MP2 (8562E)	5041-3987	1	SPACER, CRT	28480	5041-3987
A18V1 (8562E)	2090-0225	1	TUBE, CRT 6.7 IN	28480	2090-0225
A18W1 (8562E)			CABLE ASSEMBLY, TWO WIRE, TRACE ALIGN (P/O A18MP1, A17J5 to A18L1)		
A19	08562-60042	1	GPIB ASSEMBLY	28480	08562-60042
A19W1	5061-9031	1	CABLE ASSEMBLY, RIBBON, GPIB (A2J5 to Rear Panel J2)	28480	5061-9031
A20	5062-7755	1	BATTERY ASSY (Includes W6)	28480	5062-7755
A21 Standard	5063-0245	1	OCXO 10.0 MHz	28480	5063-0245
B1	5061-9036	1	FAN ASSEMBLY (Includes Wire)	28480	5083-9036

* These board assemblies are part of the rebuilt board exchange program. To order a rebuilt board, use the same number as that of the new board with the exception of the 7th digit which should be a 9. Example: New board number is 08562-60094. Therefore, the rebuilt board number will be 08562-6909.

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
BT1	1420-0341	1	BATTERY 3.0 V 1.2 A-HR LITHIUM POLYCARBON MONOFLORIDE	08709	BR 213 A 55P
F1	2110-0709	1	THIONYL FUSE 5A 250V NTD FE IEC (230 VAC Operation)	16428	GDA-5
F1	2110-0756	1	FUSE 5A 125V NTD UL (115 VAC Operation)	28480	2110-0756
FL1	0955-0703	1	LOW-PASS FILTER	28480	0955-0703
FL2	0955-0519	1	LOW-PASS FILTER, 4.4 GHz	28480	0955-0519
FL3			NOT ASSIGNED		
FL4	5061-9032	1	LINE FILTER ASSEMBLY	28480	5061-9032
LS1	9160-0282	1	LOUDSPEAKER 2.5 IN SQ (Part of W5)	28480	9160-0282
			CHASSIS MECHANICAL PARTS		
(See Figure 5-1 on page 260 through Figure 5-9 on page 283 for a listing of all mechanical chassis parts.)					
			ASSEMBLY SHIELDS		
A3 Assembly	5021-6723	1	PEAK DETECTOR (TOP)	28480	5021-6723
	5021-6724	1	PEAK DETECTOR (BOTTOM)	28480	5021-6724
	0515-2080	2	SCREW M2.5 14L	28480	0515-2080
	0515-1486	10	SCREW M2.5 9.5L	28480	0515-1486
	0905-0375	12	0-RING 0.070ID	28480	0905-0375
	2190-0583	12	WSHR LK M2.5ID	28480	2190-0583
A4 Assembly	5063-0220	1	AMP 1 (BOTTOM)	28480	5063-0220
	5063-0221	1	AMP 1 (TOP)	28480	5063-0221
	5063-0219	1	AMP 2 (TOP)	28480	5063-0219
	5063-0222	1	AMP 2 (BOTTOM)	28480	5063-0222
	0515-1486	4	SCREW SMM 2.5 10 PNTROX	28480	0515- 1486
	0515-2080	23	SCREW M2.5 14L	28480	0515-2080
	2190-0583	23	WSHR LK M2.5ID	28480	2190-0583
	0905-0375	23	0-RING 0.070ID	28480	0905-0375
A5 Assembly	5021-6729	1	IF 1 (TOP)	28480	5021-6729
	5021-6730	1	IF 1 (BOTTOM)	28480	5021-6730
	5021-6731	1	IF 2 (TOP)	28480	5021-6731
	5021-6732	1	IF 2 (BOTTOM)	28480	5021-6732
	0515-2081	16	SCREW 5MM 2.5 16 PNPDS	28480	0515-2081
	0905-0375	16	0-RING 0.070ID	28480	0905-0375
	2190-0583	16	WSHR LK M2.5ID	28480	2190-0583
A14 Assembly	5063-0209	1	FC (TOP)	28480	5063-0209
	5063-0210	1	FC (BOTTOM)	28480	5063-0210
	0515-0951	13	SCREW 5MM 2.5 16 PNPDS	28480	0515-0951
	0905-0375	13	0-RING 0.070ID	28480	0905-0375
	2190-0583	13	WSHR LK M2.5ID	28480	2190-0583
A15 Assembly	5021-6735	1	REF (TOP)	28480	5021-6735
	5021-6736	1	REF (BOTTOM)	28480	5021-6736

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
	5022-0047	1	SYNTHZR (TOP)	28480	5022-0047
	5022-0046	1	SYNTHZR (BOTTOM)	28480	5022-0046
	5021-6739	1	SIGPATH (TOP)	28480	5021-6739
	5021-6740	1	SIGPATH (BOTTOM)	28480	5021-6740
	5002-0631	1	BRACE, RF BD	28480	5002-0631
	0515-2081	2	SCREW	28480	0515-2081
	0515-2081	34	SCREW 5MM 2.5 16 PNPDS	28480	0515-2081
	0905-0375	36	0-RING 0.070ID	28480	0905-0375
	2190-0583	36	WSHR LK M2.5 ID	28480	2190-0583
	0515-0367	2	SCREW 2.5M X 8MM LG TORX	28480	0515- 0367
			CABLE ASSEMBLIES		
W1	8120-5682	1	POWER CABLE, RIBBON	28480	8120-5682
W2	5061-9025	1	CONTROL CABLE, RIBBON	28480	5061-9025
W3	5062-0728	1	CABLE ASSEMBLY LINE SWITCH	28480	5062-0728
W4	5061-9033	1	CABLE ASSEMBLY, RIBBON, OPTION MODULE (A2J6 to Rear Panel J3)	28480	5061-9033
W5	5062-4838	1	CABLE ASSEMBLY, SPEAKER	28480	5062-4838
W6	5062-0767	1	CABLE ASSEMBLY, BATTERY (A2J9 to Rear Panel Battery Holder)	28480	5062-0767
W7	8120-5697	1	CABLE ASSEMBLY, RIBBON, DISPLAY/CAL OSC (A2J3 to A17J1)	28480	8120-5697
W7 Option 007	8120-6172	1	CABLE ASSEMBLY, RIBBON, DISPLAY/CAL OSC/FADC (A2J3 to A17J1, A16J1, and A16J2)	28480	8120-6172
W8	5061-9030	1	CABLE ASSEMBLY, DISPLAY POWER (A6J4 to A17J2)	28480	5061-9030
W9	5062-6482	1	CABLE ASSEMBLY, CRT, YOKE (A17J3 and J7 to A18V1)	28480	5062-6482
W10	5062-0742	1	CABLE ASSEMBLY, RIBBON, A11 YTO DRIVE (A14J3 to A11J1)	28480	5062-0742
W11	08562-60064	1	CABLE ASSEMBLY, RIBBON, A9 ATTEN. DRIVE (A14J6 to A9)	28480	08562-60064
W12	08562-60187	1	CABLE ASSEMBLY, A7/A8 DRIVE (A14J10 to A7 and A8) Part of Cable Assembly- Microcircuit, 08562-60045)	28480	08562-60187
W13	5062-0743	1	CABLE ASSEMBLY, RIBBON, A13 2ND CONV DRIVE (A14J12 to A13) (Part of Cable Assembly Microcircuit, 08562-60045)	28480	5062-0743
W14			NOT ASSIGNED		
W15			NOT ASSIGNED		
W16	8120-5676	1	CABLE ASSEMBLY, A10 RYTHM DRIVE (A14J9 to A10)	28480	8120-5676
W18	5062-0721	1	CABLE ASSEMBLY, COAX 97, LO SWEEP 0.5 V/GHz (A14J7 to Rear Panel J8)	28480	5062-0721

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
			CABLE ASSEMBLIES (continued)		
W19 Option 001	5062-0723	1	CABLE ASSEMBLY, COAX 83 2ND IF OUT (A15J803 to Rear Panel J10)	28480	5062-0723
W20	5062-0717	1	CABLE ASSEMBLY, COAX 6, 0 SPAN VIDEO (A3J103 to A2J4)	28480	5062-0717
W22	5062-0709	1	CABLE ASSEMBLY, COAX 0, 10 MHz FREQ. COUNT (A15J302 to A2J8)	28480	5062-0709
W23	5062-0719	1	CABLE ASSEMBLY, COAX 93, EXT TRIG IN (Rear Panel J5 to A3J600)	28480	5062-0719
W24*	5062-0720	1	CABLE ASSEMBLY, COAX, 5 VIDEO OUT (A3J102 to Rear Panel J4)	28480	5062-0720
W25	5062-0718	1	CABLE ASSEMBLY, COAX 4, BLANKING OUT (A3J601 to Rear Panel J6)	28480	5062-0718
W27	5062-0714	1	CABLE ASSEMBLY, FILTER 10.7 MHz (A5J5 to A4J3)	28480	5062-0714
W29	5062-0711	1	CABLE ASSEMBLY, COAX 7, 10.7 IF (A15J601 to A5J3)	28480	5062-0711
W31 Option 005	5062-0722	1	CABLE ASSEMBLY, COAX 8, REF IN/OUT (A15J301 to Rear Panel J9)	28480	5062-0722
W32	5062-0705	1	CABLE ASSEMBLY, COAX 87, SAMPLER IF (A15J101 to A14J501)	28480	5062-0705
W32, for S/N ≥3720A99999	5063-1683	1	CABLE ASSEMBLY, COAX 87, SAMPLER IF (A15J101 to A14J501)	28480	5063-1683
W33	5062-0706	1	CABLE ASSEMBLY, COAX 81, 2ND LO DRIVE (A15J701 to A13J4)	28480	5062-0706
W34	8120-5446	1	CABLE ASSEMBLY, COAX 0, 1ST LO SAMP. (A7J4 to A15A2J1)	28480	8120-5446
W35	5062-0710	1	CABLE ASSEMBLY, COAX 92, INT 2ND IF (A13J2 to A15J801)	28480	5062-0710
W36*	5062-0725	1	CABLE ASSEMBLY, COAX 86, EXT 2ND IF (Front Panel J3 to A15J802)	28480	5062-0725
W37	5062-0707	1	CABLE ASSEMBLY, COAX 85, 10 MHz REF 1 (A15J303 to A14J301)	28480	5062-0707
W38	5022-0183	1	CABLE ASSEMBLY, SEMI-RIGID, 1ST LO (A11J2 to A7J1)	28480	5022-0183
W39	5022-1081	1	CABLE ASSEMBLY, SEMI-RIGID, 1ST MIXER LO (A7J2 to A8J3)	28480	5022-1081
W40	5062-0724	1	CABLE ASSEMBLY, COAX 89, CAL OUT (A15J501 to Front Panel J5)	28480	5062-0724
W41	5022-0169	1	CABLE ASSEMBLY, SEMI-RIGID, RF INPUT (Front panel J1 to A9J1)	28480	5022-0169
W42	5022-0189	1	CABLE ASSEMBLY, SEMI-RIGID, 1ST LO OUT (A7J5 to Front Panel J4)	28480	5022-0189
W43	5022-0186	1	CABLE ASSEMBLY, SEMI-RIGID	28480	5022-0186
*Not present in Option 327. †Not present in Option 10.					

Table 5-4 Replaceable Parts

Reference Designation	Part Number	Qty	Description	Mfr Code	Mfr Part Number
			CABLE ASSEMBLIES (CONTINUED)		
W44	5022-1124	1	CABLE ASSEMBLY, SEMI-RIGID	28480	5022-1124
W45	5022-1080	1	CABLE ASSEMBLY, SEMI-RIGID	28480	5022-1080
W46	5022-2819	1	CABLE ASSEMBLY, SEMI-RIGID (A7J3 to A10J4)	28480	5022-2819
W47			NOT ASSIGNED		
W48	8120-5660	1	CABLE ASSEMBLY, COAX 8, 1ST IF HI BAND (A10J1 to A13J3)	28480	8120-5660
W49[†]	5062-4892	1	CABLE ASSEMBLY, COAX 82, A21 OCXO (A21 to A15J305)	28480	5062-4892
W50[†]	5063-0245	1	CABLE ASSEMBLY, OCXO (A21 to A15) (Includes A21)	28480	5063-0245
W51	5062-6478	1	CABLE ASSEMBLY, COAX 84, 10 MHz REF2 (A15J304 to A4J7)	28480	5062-6478
W52	5062-6477	1	CABLE ASSEMBLY, COAX 9, 10.7 MHz CAL SIG (A5J4 to A4J8)	28480	5062-6477
W53	5062-6476	1	CABLE ASSEMBLY, COAX 1, FREQ COUNTER (A2J7 to A4J5)	28480	5062-6476
W54	5062-6475	1	CABLE ASSEMBLY, COAX 2, VIDEO(A3J101 to A4J4)	28480	5062-6475
W55	5062-6471	1	CABLE ASSEMBLY, AUDIO (A4J6 to LSI J1 and Rear Panel J1)	28480	5062-6471
W56	5022-1082	1	CABLE ASSEMBLY, SEMI-RIGID (A8J2 to FL2)	28480	5022-1082
W57	5022-0184	1	CABLE ASSEMBLY, SEMI-RIGID (FL2 to A13J1)	28480	5022-0184
W60	8120-6919	1	DISPLAY CABLE, RIBBON (A2J8 to A17J1)	28480	8120-6919
W61	8120-5026	1	CABLE, COAX (A2J9to A17J7)	28480	8120-5026
W62	8120-8482	1	CABLE, RIBBON (A17J6 to A17A1)	28480	8120-8482
W63	8120-8409	1	CABLE, RIBBON (A17J5 to A18)	28480	8120-8409
W64	8121-0062	1	VGA CABLE ASSEMBLY (A17J4 to J1 on rear panel)	28480	8121-0062
[†]Not present in Option 103.					

Figure 5-1 **Parts Identification, Assembly Mounting**
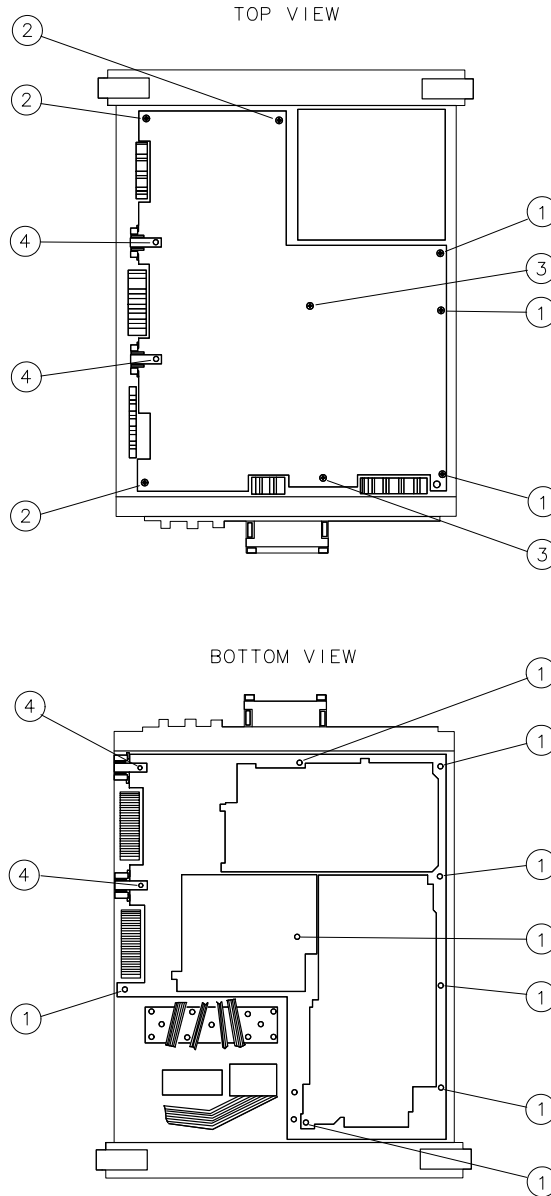
sp126e

Table 5-5 **Parts List, Assembly Mounting – 8562EC and 8562E (see Figure 5-1)**

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-1349	11	SCREW-MACH M3 X 30MM-LG PAN-HD TORX	28480	0515-1349
2	0515-2310	3	SCREW-MACH M3 X 60MM-LG PAN-HD TORX	28480	0515-2310
3	0515-3208	2	SCREW-MACH M3 X 100MM-LG PAN-HD TORX	28480	0515-2308
4	0515-2332	12	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-2332
4	0515-0664	2	SCREW-MACH M3 X 12MM-LG PAN-HD TORX	28480	0515-0664

Table 5-6   Parts List, Cover Assembly – 8562EC and 8562E (see Figure 5-2)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	5041-8911	1	BAIL HANDLE	28480	5041-8911
2	5041-8912	2	TRIM CAP	28480	5041-8912
3	0515-1114	4	SCREW MACH M4 X 10MM-LG PAN-HD	28480	0515-1114
4	1460-2164	2	SPRING-CPRSN 0.845 IN-OD 1.25-1N-OA-LG	28480	1460-2164
5	5021-6343	2	RING GEAR	28480	5021-6343
6	5021-6344	2	SOCKET GEAR	28480	5021-6344
7	5021-8667	2	HANDLE PLATE	28480	5021-8667
8	5001-8728	2	BACKUP PLATE	28480	5001-8728
9	0515-1367	6	SCREW MACH M4 X 8MM-LG 90DEG-FLH-HD	28480	0515-1367
10	0515-1133	2	SCREW-MACH M5 X 16MM-LG	28480	0515-1133
11	5001-8800	1	COVER	28480	5001-8800
12	5041-7238	1	MOISTURE DEFLECTOR-LF	28480	5041-7238
13	5041-3989	1	MOISTURE DEFLECTOR-RT	28480	5041-3989
14	5041-8913	2	SIDE TRIM	28480	5041-8913
15	0515-1114	2	SCREW-MACH M4 X 10MM-LG PAN-HD	28480	0515-1114
16	5041-8907	2	REAR FOOT	28480	5041-8907
17	0900-0024	4	O-RING 0.145-1N-XSECT-DIA SIL	51633	A5568-007
18	2190-0587	4	WASHER-LK HLCL 5.0 MM 5.1-MM-ID	28480	2190-0587
19	0515-1218	4	SCREW-SKT-HD-CAP M5 X 40MM-LG	28480	0515-1218
20	08562-80028	1	INSULATOR 292 X 355 MM 0.51 THK	28480	08562-80028

Table 5-7   Parts List, Main Chassis – 8562EC (see Figure 5-7)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-2145	4	SCREW-MACH M3 X 8MM-LG PAN-HD TORX	28480	0515-2145
5	5002-1010	1	COVER, A6 POWER SUPPLY (Includes label)	28480	5002-1010
6	0515-2309	3	SCREW-MACH M3 X 0.5 45MM-LG TORX	28480	0515-2309
14	5002-1008	1	MAIN DECK	28480	5002-1008
15	5002-1002	1	FRONT END DECK	28480	5002-1002
16	0515-1101	4	SCREW-MACH M4 X 8MM-LG FLH-HD TORX	28480	0515-1101
17	0515-1227	2	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
18	5021-7464	2	SIDE FRAME	28480	5021-7464
19	0515-1101	12	SCREW-MACH M4 X 8MM-LG FLH-HD TORX	28480	0515-1101
20	0515-1227	12	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
21	0515-1227	8	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
22	0515-1227	5	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
23	5021-5484	5	MOUNTING POST	28480	5021-5484
24	5062-0750	2	HINGE, 2 BOARD	28480	5062-0750
25	5062-0751	2	HINGE, 4 BOARD	28480	5062-0751
26	5041-7250	1	CABLE CLAMP	28480	5041-7250
28	0515-1227	2	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
30	5063-0269	1	SHIELD WALL, TOP	28480	5063-0269
31	5063-0268	1	SHIELD WALL, BOTTOM	28480	5063-0268

Table 5-7 **Parts List, Main Chassis – 8562EC (see Figure 5-7)**

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
33	0515-0430	2	SCREW-INVERTER BOARD	28480	0515-0430
34	0515-0372	4	SCREW-DISPLAY DRIVER	28480	0515-0372
35	0400-0333	4	STANDOFF CUSHIONS	28480	0400-0333
36	1000-1014	1	LCD GLASS PLATE	28480	1000-1014
37	5041-9632	1	LCD MOUNT	28480	5041-9632
38	5000-8314	1	LCD BACKPLATE	28480	5000-8314
39	5022-3667	1	LCD DRIVER SHIELD	28480	5022-3667
A17	08562-6016	1	LCD DRIVER BOARD	28480	08562-6016
A17A1	0950-60166	1	INVERTER BOARD	28480	0950-60166
A18	2090-0379	1	LCD ASSEMBLY - INCLUDES LCD GLASS, LCD MOUNT, AND A18DS1 and A18DS2 BACKLIGHTS	28480	2090-0379

Table 5-8 **Parts List, Main Chassis – 8562E (see Figure 5-3)**

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-2145	4	SCREW-MACH M3 X 8MM-LG PAN-HD TORX	28480	0515-2145
3	0515-1715	3	SCREW-MACH M3 X 35MM-LG PAN-HD TORX	28480	0515-1715
4	0380-2052	2	SPACER 0.937LG 0.166ID	28480	0380-2052
5	5002-1010	1	COVER, A6 POWER SUPPLY (Includes label)	28480	5002-1010
6	0515-2309	3	SCREW-MACH M3 X 0.5 45MM-LG TORX	28480	0515-2309
7	5041-7246	1	BOARD MOUNT	28480	5041-7246
8	0515-0372	2	SCREW-MACH M3 X 8MM-LG PAN-HD TORX	28480	0515-0372
9	5041-8961	1	COVER, A17	28480	5041-8961
10	5021-5486	2	CRT MOUNT	28480	5021-5486
11	5001-5870	2	CRT MOUNT STRAP	28480	5001-5870
13	0515-0372	4	SCREW-MACH M3 X 8MM-LG PAN-HD TORX	28480	0515-0372
14	5002-1008	1	MAIN DECK	28480	5002-1008
15	5002-1002	1	FRONT END DECK	28480	5002-1002
16	0515-1101	4	SCREW-MACH M4 X 8MM-LG FLH-HD TORX	28480	0515-1101
17	0515-1227	2	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
18	5021-7464	2	SIDE FRAME	28480	5021-7464
19	0515-1101	12	SCREW-MACH M4 X 8MM-LG FLH-HD TORX	28480	0515-1101
20	0515-1227	12	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
21	0515-1227	8	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
22	0515-1227	5	SCREW MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
23	5021-5484	5	MOUNTING POST	28480	5021-5484
24	5062-0750	2	HINGE, 2 BOARD	28480	5062-0750
25	5062-0751	2	HINGE, 4 BOARD	28480	5062-0751
26	5041-7250	1	CABLE CLAMP	28480	5041-7250
27	0515-2164	2	SCREW-MACH M3 X 35MM-LG TORX	28480	0515-2164
28	0515-1227	2	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
29	5181-5040	1	LABEL, ASSEMBLY LOCATIONS	28480	5181-5040
30	5063-0269	1	SHIELD WALL, TOP	28480	5063-0269
31	5063-0268	1	SHIELD WALL, BOTTOM	28480	5063-0268

Table 5-8   Parts List, Main Chassis – 8562E (see Figure 5-3)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
A18MP1	5062-7095	1	CRT WIRING ASSY (INCLUDES A18L1, A18W1)	28480	5062-7095
A18MP2	5041-3987	1	SPACER, CRT	28480	5041-3987
A18 V1	2090-0225	1	TUBE, CRT	28480	2090-0225
A18W1			P/O A18MP1		

Table 5-9   Parts List, RF Section – 8562EC and 8562E (see Figure 5-4)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-1032	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-1032
2	0515-2332	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-2332
3	0515-2332	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-2332
4	5021-7467	1	FILTER CLAMP	28480	5021-7467
6	0515-2332	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-2332
7	5002-1008	1	MAIN DECK	28480	5002-1008
8	0515-1227	2	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
9	5002-1002	1	FRONT END DECK	28480	5002-1002
11	0515-1227	4	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
12	2360-0461	4	SCREW-MACH 6-32 0.375-IN-LG TORX	28480	2360-0461
13	0515-0372	1	SCREW-MACH M3 X 8MM-LG PAN-HD TORX	28480	0515-0372
14	0515-1250	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-1250
15	5001-8731	1	ATTENUATOR BRACKET	28480	5001-8731
18	08560-00002	1	ATTENUATOR BRACKET	28480	08560-00002
19	0515-1250	2	SCREW-MACH M3 X 6MM-LG PAN-HD TORX	28480	0515-1250
20	0515-1227	1	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
22	0515-1227	4	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1227
23	0515-1410	2	SCREW-MACH M3 X 6MM-LG FLH-HD TORX	28480	0515-1410

Table 5-10 **Parts List, Front Frame – 8562EC (see Figure 5-8)**

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	08562-80208	1	DRESS PANEL OVERLAY	28480	08562-80208
2	5181-8245		CONNECTOR OVERLAY	28480	5181-8245
4	0370-3069	1	KNOB BASE 1-1/8 JGK .252-IN-IO (INCLUDES ITEM 5)	28480	0370-3069
5	3030-0022	2	SCREW-SET 6-32 .125-IN-LG SMALL CUP-PT	00000	DESCRIBE
6	2950-0043	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	DESCRIBE
7	2190-0016	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
8	5181-8246	1	FRONT PANEL-DRESS	28480	5181-8246
9	5060-0467	1	PROBE POWER JACK	28480	5060-0467
10	0590-1251	1	NUT-SPCLY 15/32-32-THD .1-IN-THK .562-WD	00000	DESCRIBE
	6960-0171	1	PLUG-HOLE (Opt. 327)(not shown)	28480	6960-0171
11	1250-1666	2	ADAPTOR COAX STR F-SMA F-SMA	28480	1250-1666
12	0515-2145	12	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD TX	28480	0515-2145
13	5062-4806	1	BUMPER KIT (Includes 4 bumpers)	28480	5062-4806
15	5021-5483	2	CATCH LATCH	28480	5021-5483
16	0515-0366	4	SCREW-MACH M2.5 X 0.45 6MM-LG PAN-HD TX	28480	0515-0366
17	5022-0199	1	FRONT FRAME	28480	5022-0199
18	8160-0520	1	RFI ROUND STRIP STL MSH/SIL RBR CU/SN	28480	8160-0520
19	2950-0154	1	NUT	28480	2950-0154
20	2190-0016	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
21	2950-0043	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	DESCRIBE
22	1250-1811	1	ADAPTER N(f) SMA (f) (Standard)	28480	1250-2191
22	1250-1811	2	ADAPTER N(f) SMA (f) (Option 002)	28480	1250-2191
23	5022-3711	1	WASHER	28480	0515-0430
24	5041-9630		RUBBER KEYPAD (INCLUDES KEYCAPS)	28480	5041-9630
25	1990-1131	1	LED-LAMP LUM-INT=560UCD IF=20MA-MAX	2M627	LD-101MG
26	5063-3966	1	LINE SWITCH CABLE ASSEMBLY	28480	5063-3966
27	0900-0010	1	O-RING .101-IN-ID .07-IN-XSECT-DIA NTRL	51633	AS568-005
28	0515-0664	1	SCREW-MACHINE ASSEMBLYM3 X0.5 12MM-LG	28480	0515-0664
31	0515-1934	7	SCREW-MACH M2.5 X 0.45 6MM-LG PAN-HD TX (P/O A1W1)	28480	0515-1934
32	2100-4232	1	R-VC 20K 20% LOG	28480	2100-4232
33	3050-0014	2	WASHER-FL .250ID12	28480	3050-0014
34	2190-0067	1	WASHER-LK INTL .256-IN-ID	28480	2190-0067
35	2950-0072	1	NUT-HEX 1/4-32 THD	28480	2950-0072
36	0370-3079	1	KNOB RND .125 JG	28480	0370-3079

Table 5-11   Parts List, Front Frame – 8562E (see Figure 5-5)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-1622	4	SCREW-SKT-HD-CAP M4 X 0.7 8MM-LG	28480	0515-1622
2	5041-8906	1	CRT BEZEL	28480	5041-8906
3	1000-0897	1	RFI CRT FACEPLATE	28480	1000-0897
4	0370-3069	1	KNOB BASE 1-1/8 JGK 0.252-IN-IO (INCLUDES ITEM 5)	28480	0370-3069
5	3030-0022	2	SCREW-SET 6-32 0.125-IN-LG SMALL CUP-PT	00000	DESCRIBE
6	2950-0043	1	NUT-HEX-DBL-CHAM 3/8-32-THD 0.094-IN-THK	00000	DESCRIBE
7	2190-0016	1	WASHER-LK INTL T 3/8 IN 0.377-IN-ID	28480	2190-0016
8	08562-00030	1	FRONT PANEL-DRESS (8562E)	28480	08562-00030
9	5060-0467	1	PROBE POWER JACK	28480	5060-0467
10	0590-1251	1	NUT-SPCLY 15/32-32-THD 0.1-IN-THK .562-WD	00000	DESCRIBE
	6960-0171	1	PLUG-HOLE (Opt. 327)(not shown)	28480	6960-0171
11	1250-1666	2	ADAPTOR COAX STR F-SMA F-SMA	28480	1250-1666
12	0515-2145	12	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD TX	28480	0515-2145
13	5062-4806	1	BUMPER KIT (Includes 4 bumpers)	28480	5062-4806
14	0905-1018	4	O-RING 0.126TD	28480	0905-1018
15	5021-5483	2	CATCH LATCH	28480	5021-5483
16	0515-0366	4	SCREW-MACH M2.5 X 0.45 6MM-LG PAN-HD TX	28480	0515-0366
17	5022-0199	1	FRONT FRAME	28480	5022-0199
18	8160-0520	1	RFI ROUND STRIP STL MSH/SIL RBR CU/SN	28480	8160-0520
19	0535-0082	3	NVTM W LKWR M4	28480	0535-0082
20	2190-0016	1	WASHER-LK INTL T 3/8 IN 0.377-IN-ID	28480	2190-0016
21	2950-0043	1	NUT-HEX-DBL-CHAM 3/8-32-THD 0.094-IN-THK	00000	DESCRIBE
22	5086-7895	1	RF INPUT ASSEMBLY (Standard)	28480	5086-7895
22	08673-60040	1	RF INPUT ASSEMBLY (Option 026)	28480	08673-60040
23	0515-2145	2	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD TX	28480	0515-2145
24	5041-8985	1	RUBBER KEYPAD (INCLUDES KEYCAPS)	28480	5041-8985
25	1990-1131	1	LED-LAMP LUM-INT=560UCD IF=20MA-MAX	2M627	LD-101MG
26	5041-1682	1	KEYCAP "LINE"	28480	5041-1682
27	0900-0010	1	O-RING 0.101-IN-ID 0.07-IN-XSECT-DIA NTRL	51633	AS568-005
28	0515-0664	1	SCREW-MACHINE ASSEMBLY M3 X 0.5 12MM-LG	28480	0515-0664
29	5021-5482	1	SUPPORT CENTER	28480	5021-5482
30	0515-1143	2	SCREW-MACH M4 X 0.7 16MM-LG PAN-HD TX	28480	0515-1143
31	0515-1934	9	SCREW-MACH M2.5 X 0.45 6MM-LG PAN-HD TX (P/O A1W1)	28480	0515-1934
32	2100-4232	1	R-VC 20K 20% LOG	28480	2100-4232
33	3050-0014	2	WASHER-FL 0.250ID12	28480	3050-0014
34	2190-0067	1	WASHER-LK INTL 0.256-IN-ID	28480	2190-0067
35	2950-0072	1	NUT-HEX 1/4-32 THD	28480	2950-0072
36	0370-3079	1	KNOB RND 0.125 JG	28480	0370-3079
	5021-9320	2	FLANGE MOUNT (Opt. 026 – not shown)	28480	5021-9320

Table 5-12   Parts List, Rear Frame – 8562EC (see Figure 5-9)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-1946	2	SCREW-MACH M3 6MM-LG FLH-HD TORX	28480	0515-1946
2	5062-7755	1	BATTERY HOLDER (INCLUDES WIRES)	28480	5062-7755
3	0515-2216	4	SCREW-MACH M4 40MM-LG PAN-HD TORX	28480	0515-2216
4	3160-0309	1	FAN GRILL	28480	3160-0309
5	0380-0012	4	SPACER-RND 0.875-IN-ID	28480	0380-0012
6			NOT ASSIGNED		
7	6960-0002	1	PLUG-HOLE TR-HD FOR 0.5-D-HOLE STL	05093	SS-48152
8	6960-0023	1	PLUG-HOLE DOME-HD FOR 0.312-D-HOLE STL	04213	D-2730-LC2
9	1250-1753	1	ADAPTOR-COAX STR F-SMA OPT 001 (INCLUDES WASHER AND NUT)	28480	1250-1753
10	0515-1946	4	SCREW-MACH M3 6MM-LG FLH-HD TORX	28480	0515-1946
11	0515-0684	1	SCREW-MACH M3 6MM-LG PAN-HD TORX	28480	0515-0684
12	2950-0035	1	NUT HEX 15/32THD	28480	2950-0035
13	1252-0995	1	CONNECTOR-TEL 2-CKT 0.141-SHK-DIA (INCLUDES NUT AND JACK)	28480	1252-0995
14	5002-4049	1	REAR PANEL-DRESS	28480	5002-4049
15	0515-2145	4	SCREW-MACH M3 6MMLG PAN-HD TORX	28480	0515-2145
16	8160-0520	1	RFI ROUND STRIP STL SPIRA 0.150	28480	8160-0520
17	5022-3778	1	REAR FRAME	28480	5022-3778
18	5021-6391	2	SCREW-CONNECTOR GPIB	28480	5021-6391
19	2200-0225	2	SCREW-MACH 4-40 0.25-IN-LG TORX	28480	2200-0225
20	0535-0082	2	NUT M4.0 W/LOCKWR	28480	0535-0082
21	0515-0433	1	SCREW-MACH M3 6MM-LG PAN-HD TORX	28480	0515-0433
22	0535-0023	2	NUT-HEX DBL-CHAM M4 X 0.7 3.2MM-THK	28480	0535-0023
23	8121-0062	1	VGA CONNETOR AND CABLE		8121-0062
B1	5061-9036	1	FAN ASSEMBLY (INCLUDES WIRE)	28480	5061-9036
BT1	1420-0341	1	BATTERY 3.0V 1.2A-HR LITHIUM POLYCARBONMONOFLUORIDE	08709	BR 2/3A SSP
FL4	5061-9034	1	LINE FILTER MODULE	28480	5061-9034

Table 5-13   Parts List, Rear Frame – 8562E (see Figure 5-6)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
1	0515-1946	2	SCREW-MACH M3 6MM-LG FLH-HD TORX	28480	0515-1946
2	5062-7755	1	BATTERY HOLDER (INCLUDES WIRES)	28480	5062-7755
3	0515-2216	4	SCREW-MACH M4 40MM-LG PAN-HD TORX	28480	0515-2216
4	3160-0309	1	FAN GRILL	28480	3160-0309
5	0380-0012	4	SPACER-RND 0.875-IN-ID	28480	0380-0012
6			NOT ASSIGNED		
7	6960-0002	1	PLUG-HOLE TR-HD FOR 0.5-D-HOLE STL	05093	SS-48152
8	6960-0023	1	PLUG-HOLE DOME-HD FOR 0.312-D-HOLE STL	04213	D-2730-LC2
9	1250-1753	1	ADAPTOR-COAX STR F-SMA OPT 001 (INCLUDES WASHER AND NUT)	28480	1250-1753

Table 5-13   Parts List, Rear Frame – 8562E (see Figure 5-6)

Item	Part Number	Qty	Description	Mfr Code	Mfr Part Number
10	0515-1946	4	SCREW-MACH M3 6MM-LG FLH-HD TORX	28480	0515-1946
11	0515-0684	1	SCREW-MACH M3 6MM-LG PAN-HD TORX	28480	0515-0684
12	2950-0035	1	NUT HEX 15/32THD	28480	2950-0035
13	1252-0995	1	CONNECTOR-TEL 2-CKT 0.141-SHK-DIA (INCLUDES NUT AND JACK)	28480	1252-0995
14	5002-1012	1	REAR PANEL-DRESS	28480	5002-1012
15	0515-2145	4	SCREW-MACH M3 6MMLG PAN-HD TORX	28480	0515-2145
16	8160-0520	1	RFI ROUND STRIP STL SPIRA .150	28480	8160-0520
17	5021-5479	1	REAR FRAME	28480	5021-5479
18	5021-6391	2	SCREW-CONNECTOR GPIB	28480	5021-6391
19	2200-0225	2	SCREW-MACH 4-40 0.25-IN-LG TORX	28480	2200-0225
20	0535-0082	2	NUT M4.0 W/LOCKWR	28480	0535-0082
21	0515-0433	1	SCREW-MACH M3 6MM-LG PAN-HD TORX	28480	0515-0433
22	0535-0023	2	NUT-HEX DBL-CHAM M4 X 0.7 3.2MM-THK	28480	0535-0023
B1	5061-9036	1	FAN ASSEMBLY (INCLUDES WIRE)	28480	5061-9036
BT1	1420-0341	1	BATTERY 3.0V 1.2A-HR LITHIUM POLYCARBONMONOFLUORIDE	08709	BR 2/3A SSP
FL4	5061-9034	1	LINE FILTER MODULE	28480	5061-9034
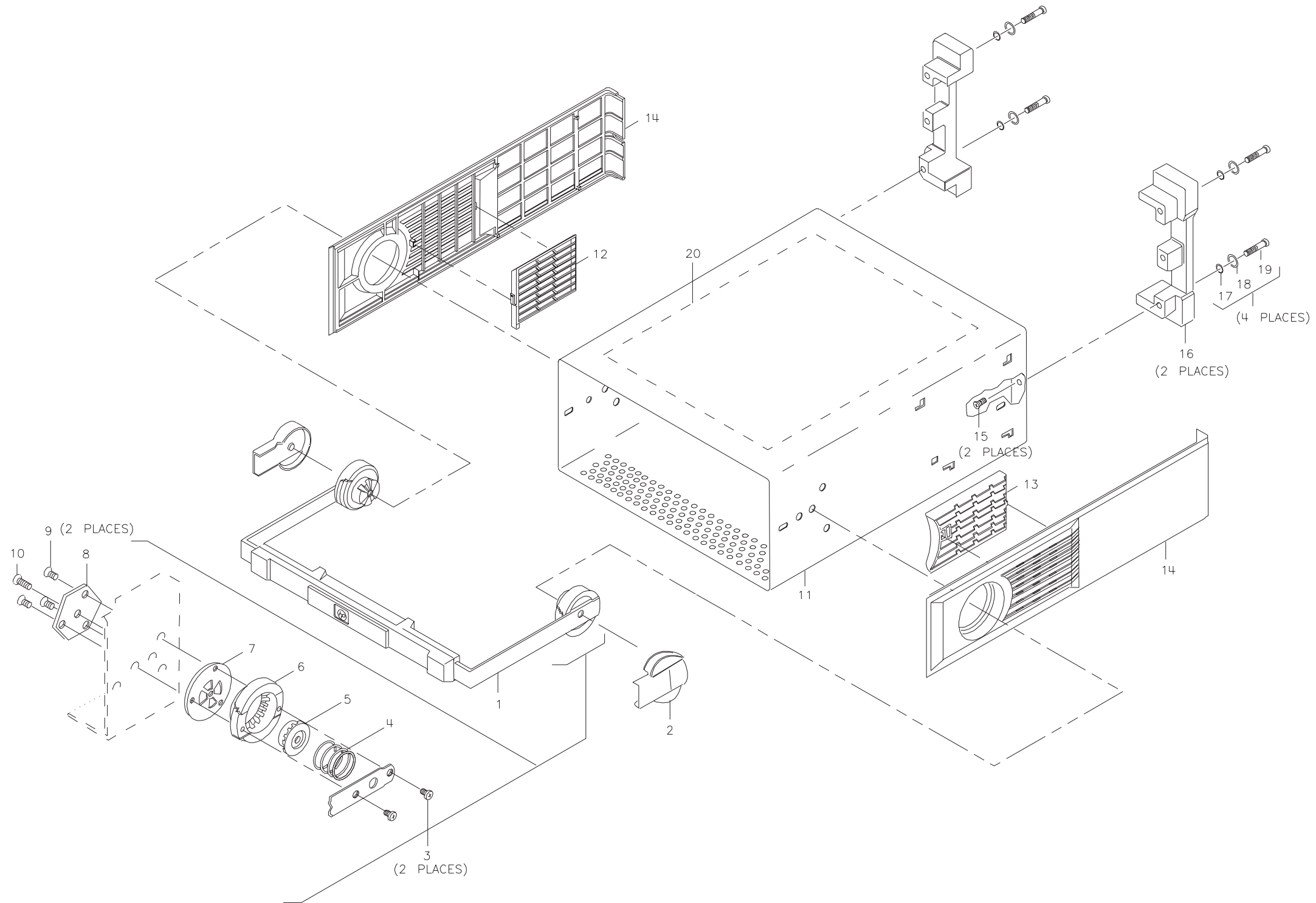
Figure 5-2. Parts Identification, Cover Assembly

FIGURE 5-3. PARTS IDENTIFICATION, MAIN CHASSIS
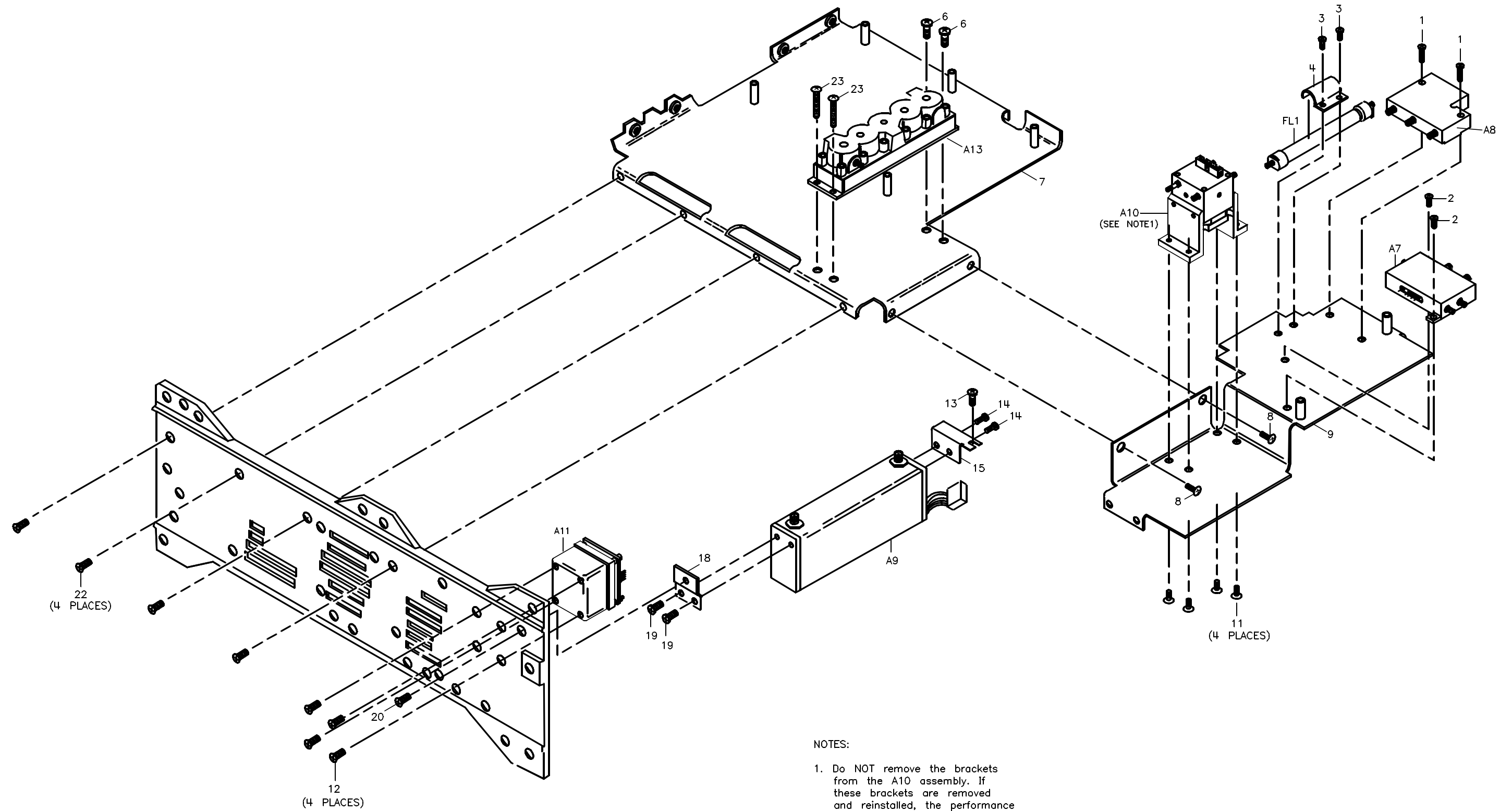
NOTES:

1. Do NOT remove the brackets
   from the A10 assembly. If
   these brackets are removed
   and reinstalled, the performance
   of A10 will be altered. A
   new or rebuilt A10 assembly
   includes new mounting brackets
   already attached to it.

Figure 5-4. Parts Identification, RF Section

8562E
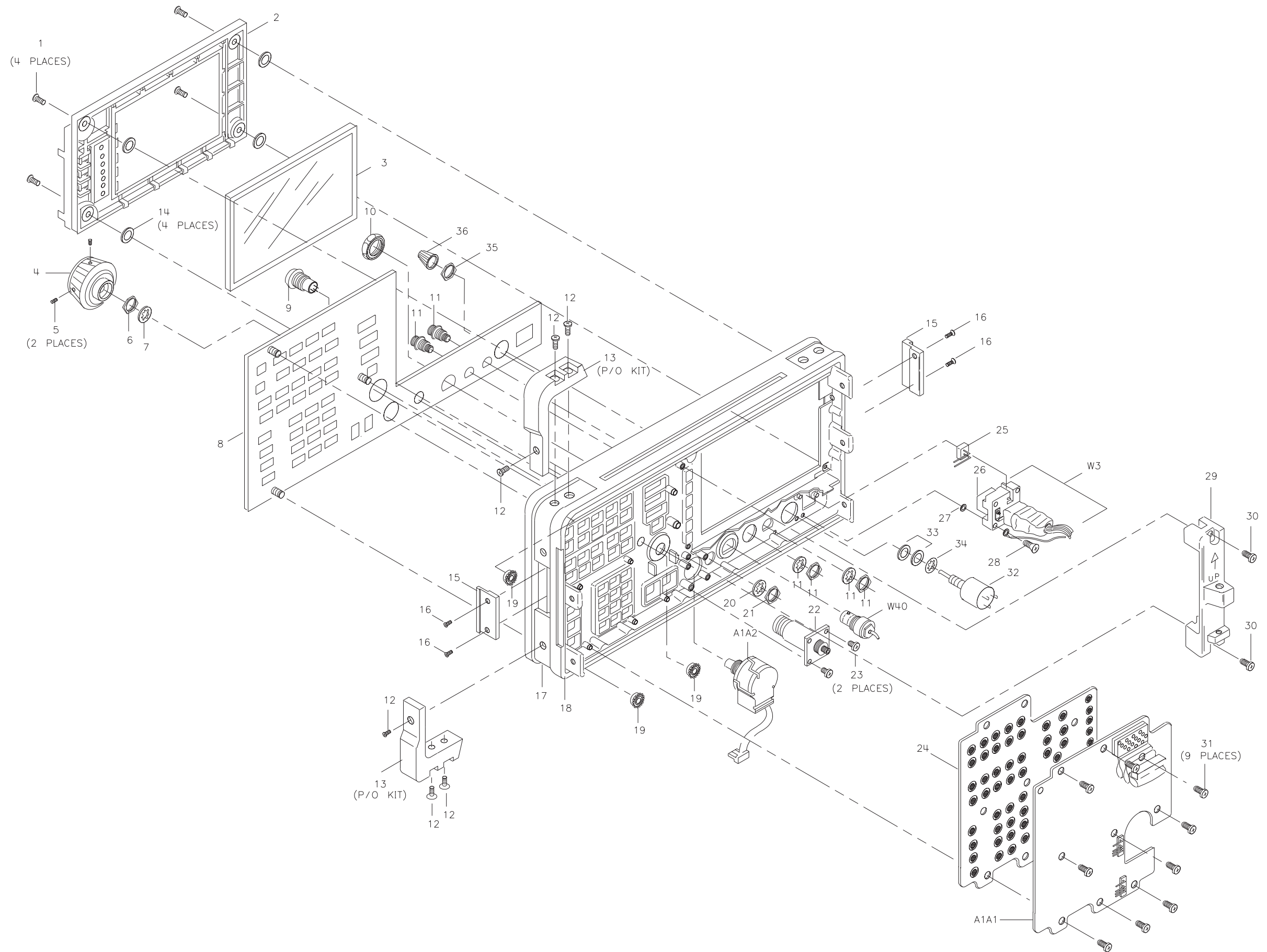
Figure 5-5. Parts Identification, Front Frame

sl128e
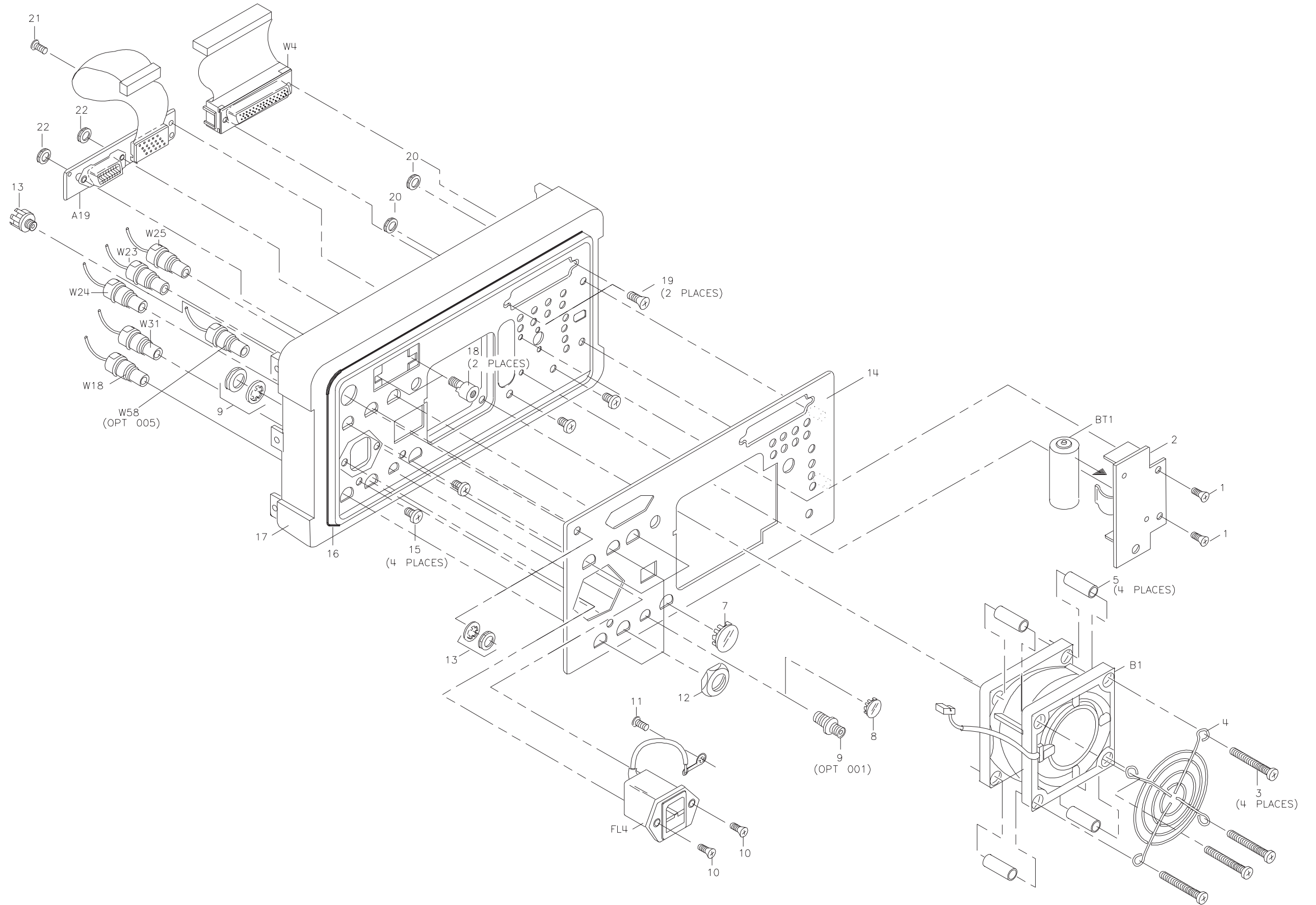
Figure 5-6. Parts Identification, Rear Frame

s1127c

8560 EC-SERIES

FIGURE 5-7. PARTS IDENTIFICATION, MAIN CHASSIS

s1119c

Note: Refer to EC-Series Chassis Diagram for Detail of LCD Assembly
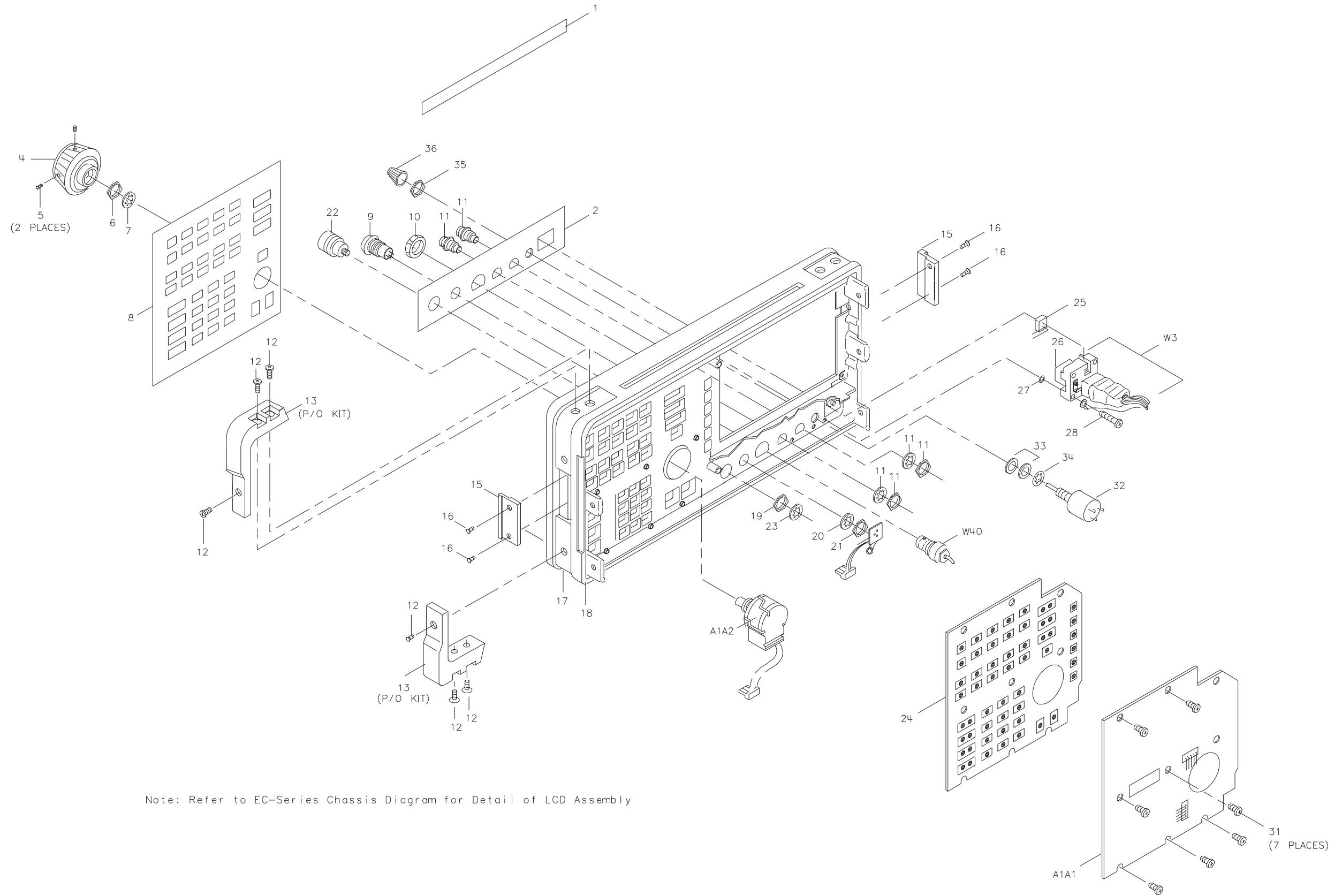
Figure 5-8. Parts Identification, Front Frame
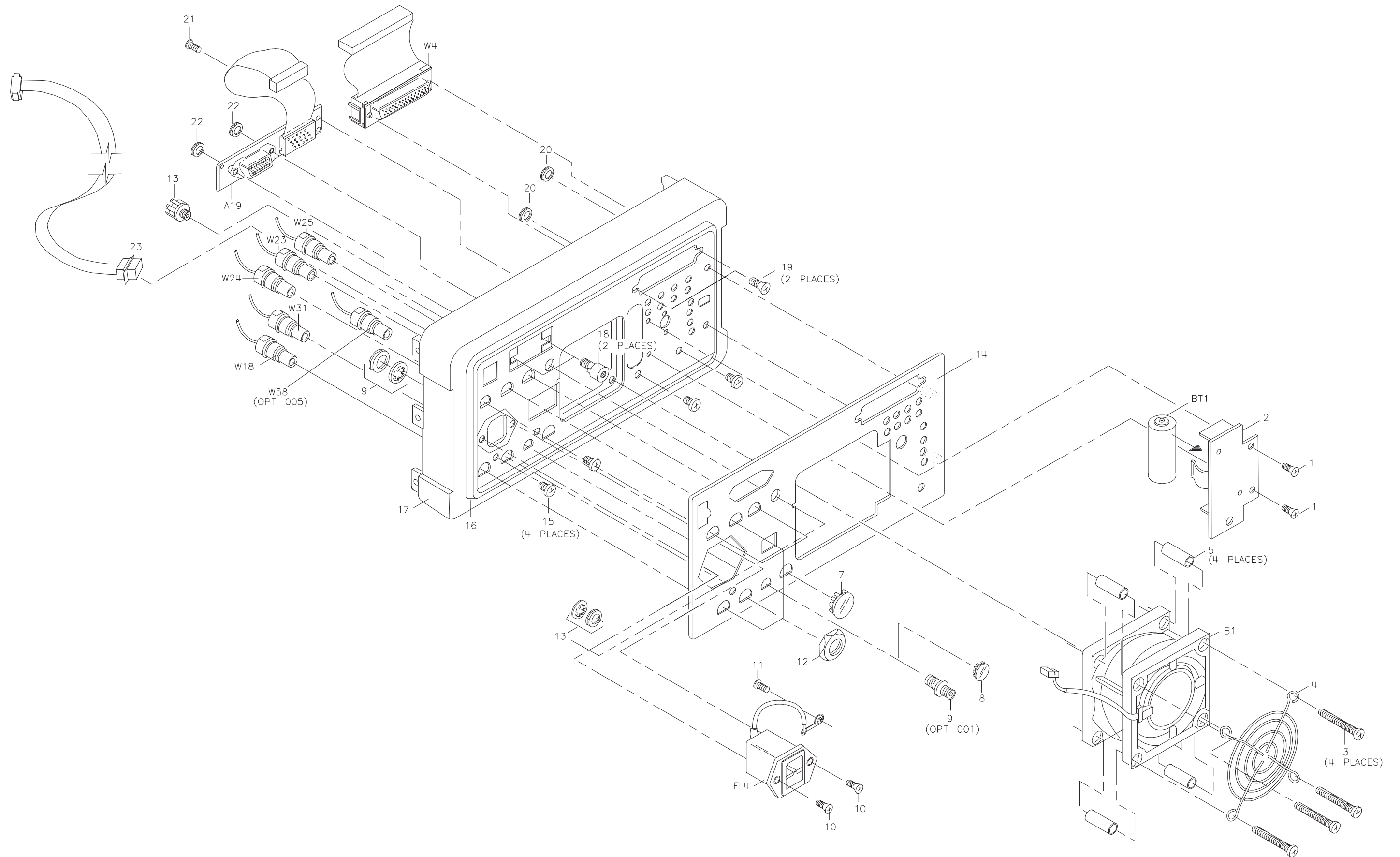
Figure 5-9. Parts Identification, Rear Frame

s1117c

6 Major Assembly and Cable Locations

Introduction

This chapter identifies the instrument assemblies and cables and contains the following figures:

Use the list below to determine the figure illustrating the desired assembly or cable.

Assemblies .... **Figure**
A1 front frame 6-8
A1A1 keyboard 6-8
A2 controller (8562EC) 6-2, 6-3
A2 controller (8562E) 6-4, 6-5
A3 interface 6-3, 6-4
A4 log amplifier/cal oscillator 6-3, 6-5
A5 IF filter 6-3, 6-6
A6 power supply 6-6
A6A1 high voltage module 6-6
A7 first LO distribution amplifier (SLODA) 6-10
A8 low band mixer 6-10
A9 RF attenuator 6-10
A10 YIG-tuned filter/mixer (RYTHM) 6-10
A11 YTO 6-10
A12 .... (NOT ASSIGNED)
A13 second converter 6-10
A14 frequency control 6-3, 6-8
A15 RF 6-3, 6-7, 6-8
A16 fast ADC (Option 007) 6-9
A17 LCD driver (8562EC)..6-4,6-5
A17 CRT driver (8562E) 6-6
A17A1 LCD Inverter board (8562EC)..
A18 LCD Assembly (8562EC)..6-4,6-5
A18 CRT assembly (8562E) 6-6
A19 GPIB 6-6
A20 battery assembly 6-11

Figure 6-1   **Hinged Assemblies**
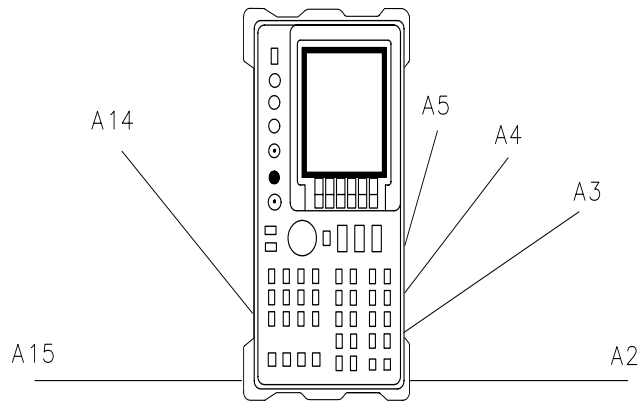
SK155

NOTE   Figure 6-1 shows an 8560 E-series instrument. EC-series instruments
are identical except the A2 board is smaller.

NOTE   Parts common to E-series and EC-series instruments are illustrated in
              diagrams that show E-series instruments. Where there are differences
              between E-series and EC-series instruments, separate diagrams are
              provided.

Figure 6-2   Top View (A2 and A3 Unfolded) – EC-Series
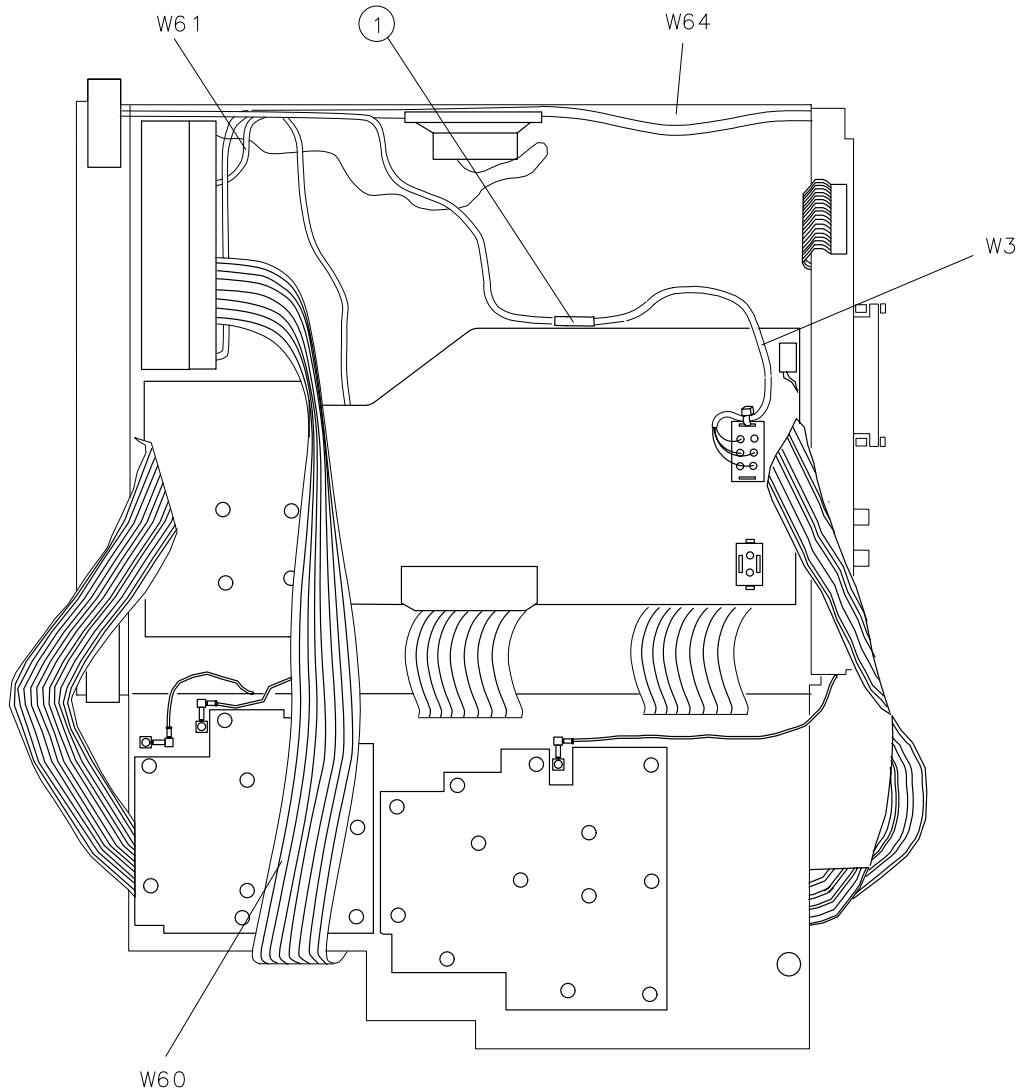
sl115c

Figure 6-3   **Top View (A2, A3. A4, and A5 Unfolded) – EC-Series**
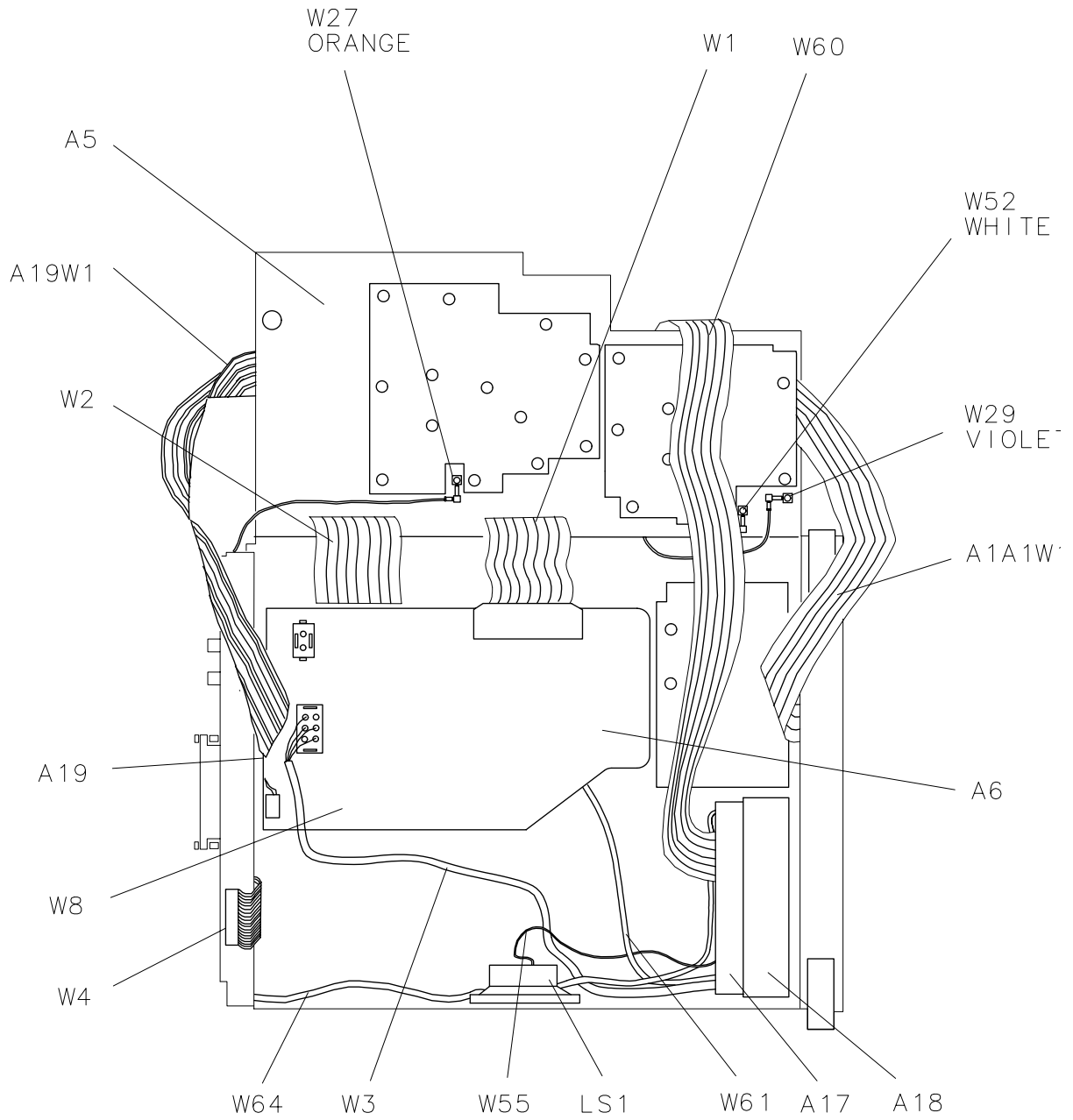
Figure 6-4   Top View (A2 Unfolded) – E-Series
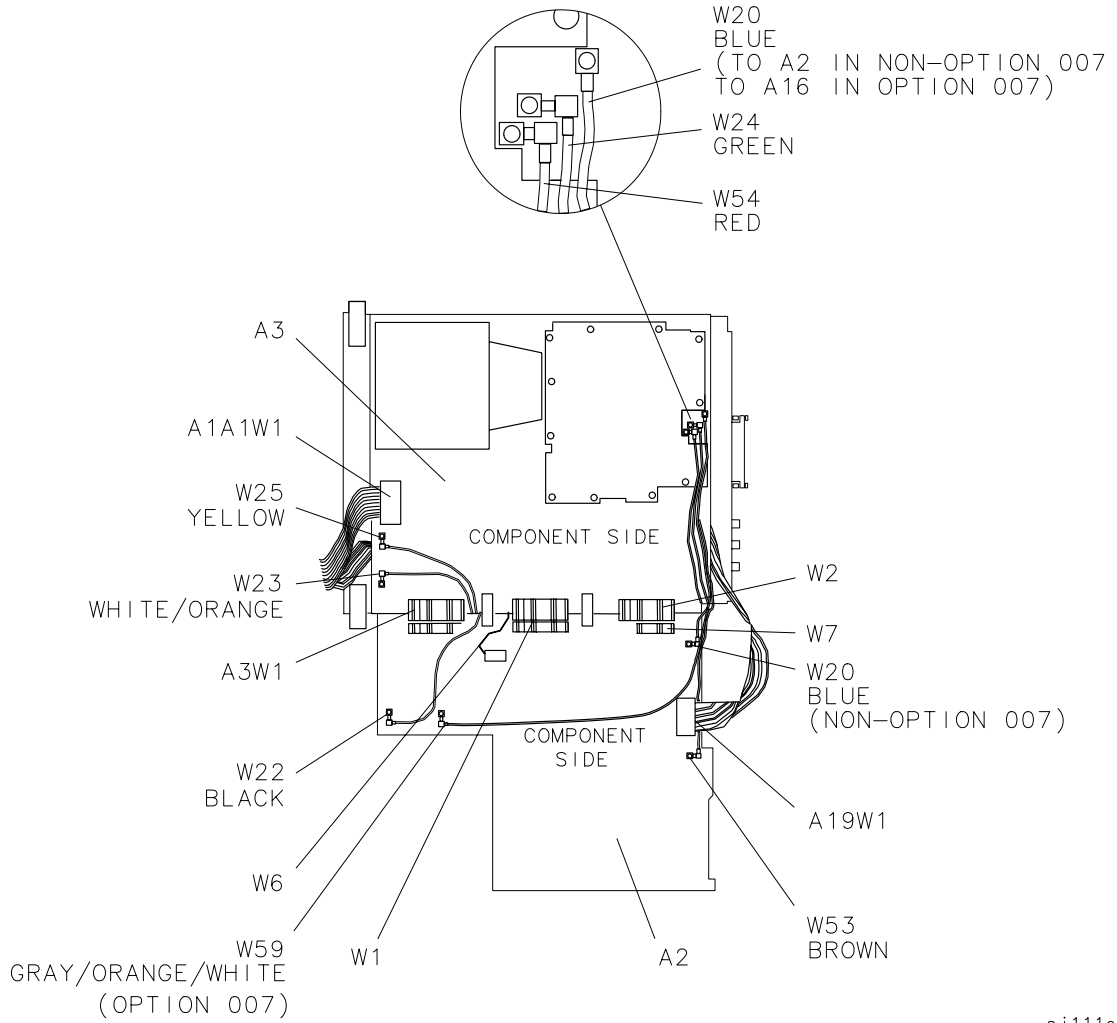
sj111e

Figure 6-5 **Top View (A2 and A3 Unfolded) – E-series**
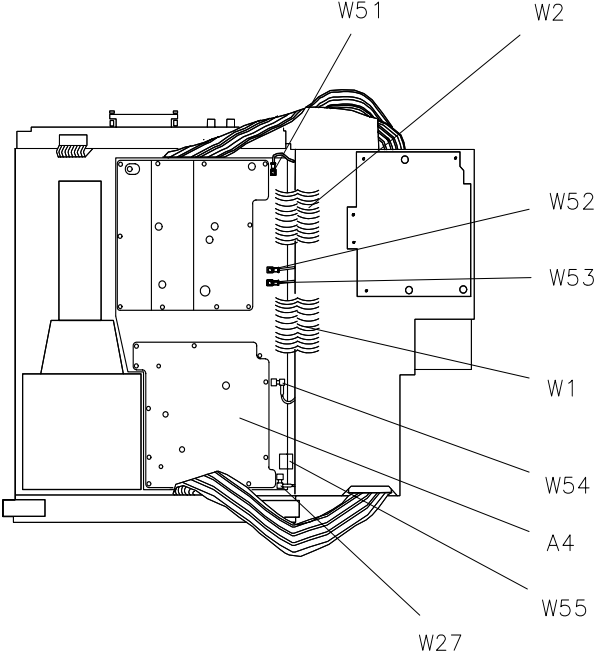
Figure 6-6   **Top View (A2, A3, A4, and A5 Unfolded) – E -Series**
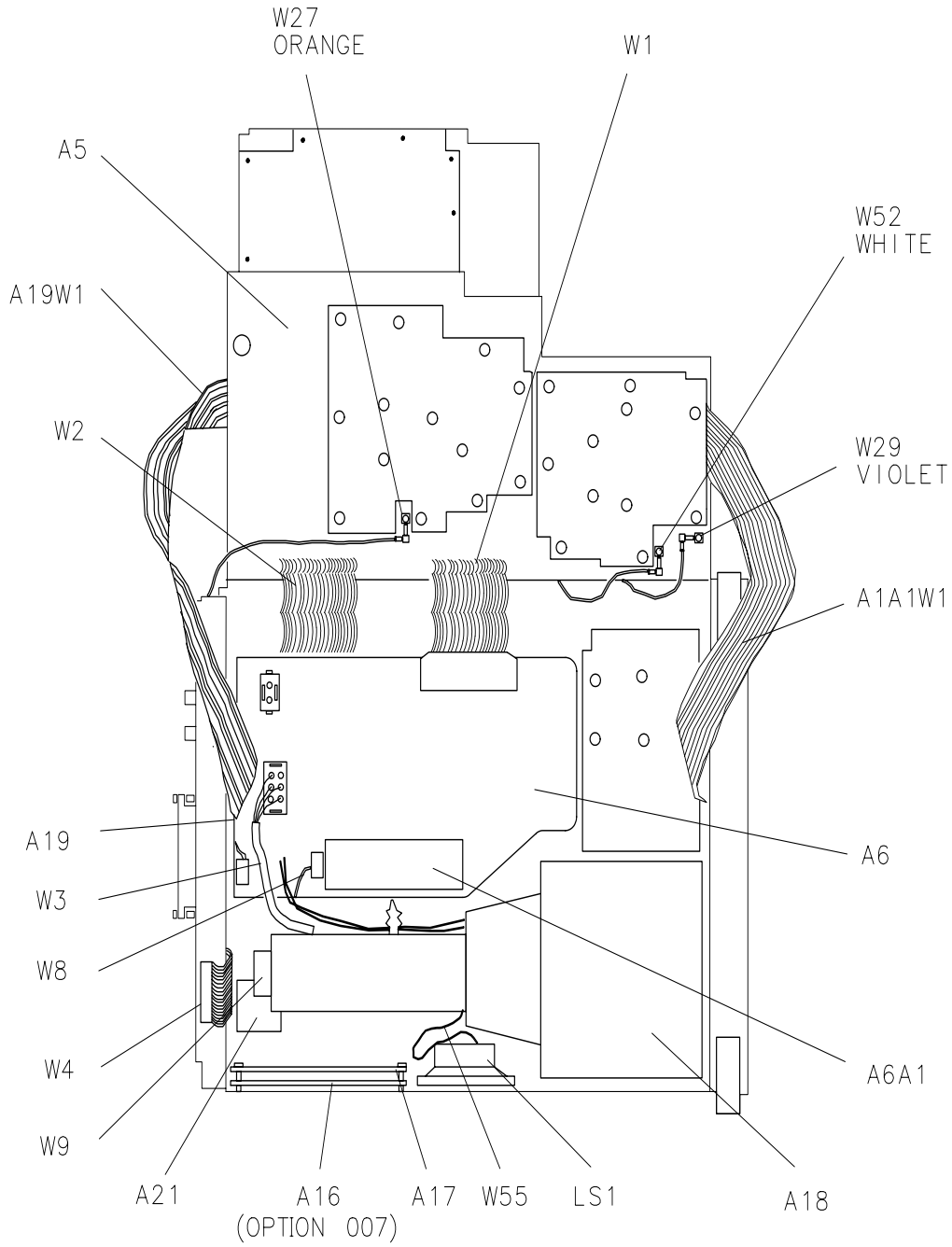
SP110E

Figure 6-7   **Bottom View (A15 Unfolded)**

sp166e
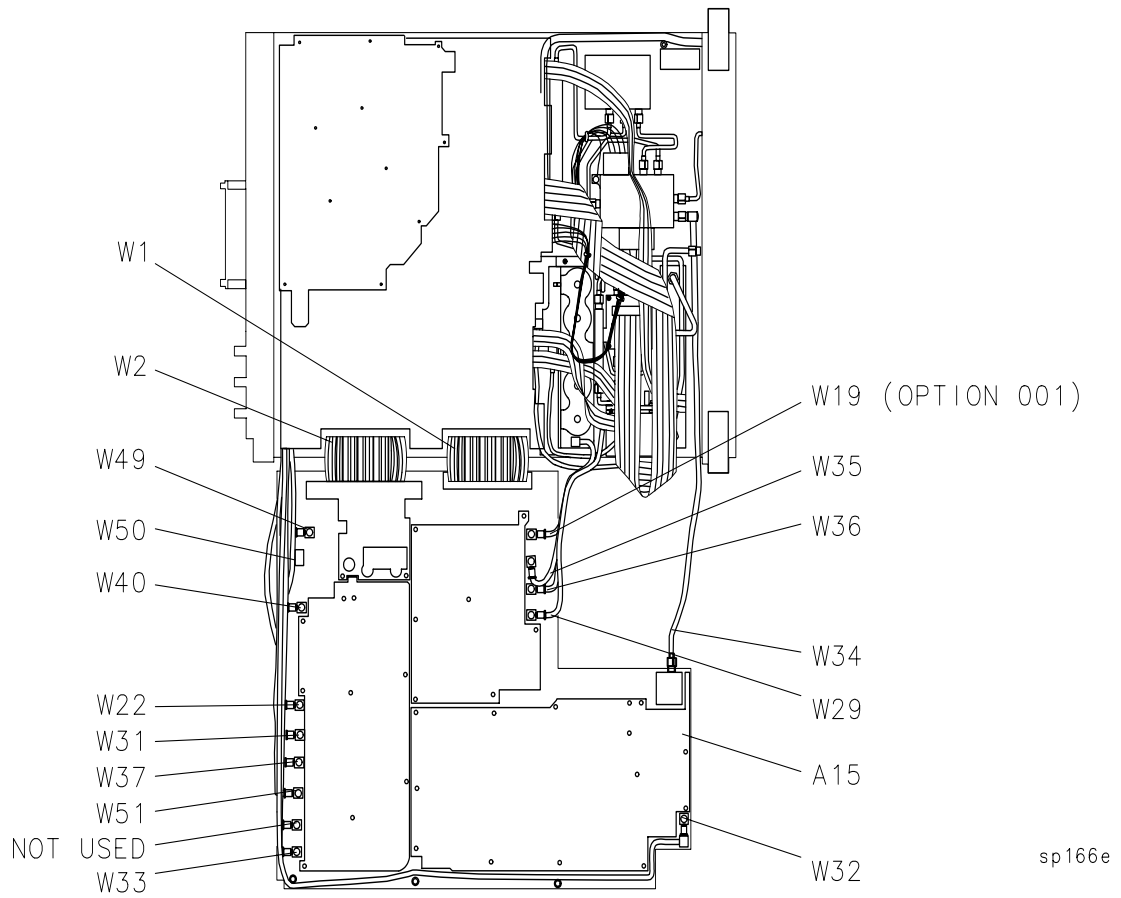
Figure 6-8   Bottom View (A15 and A14 Unfolded)
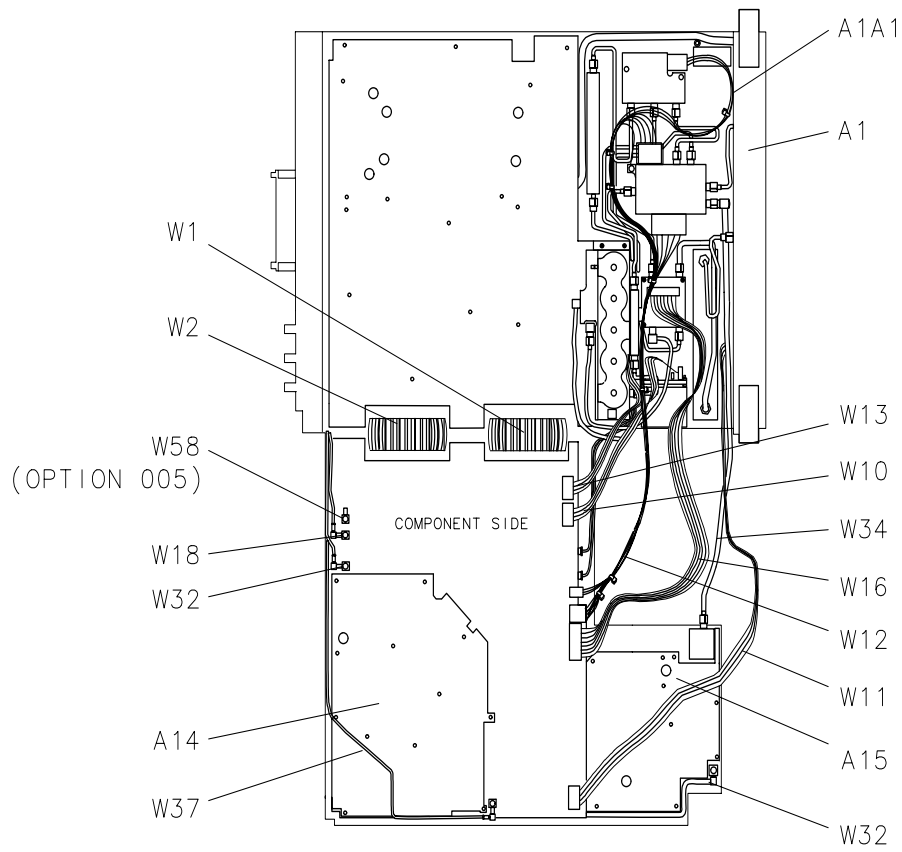
Figure 6-9   **A16 Fast ADC (Option 007)**
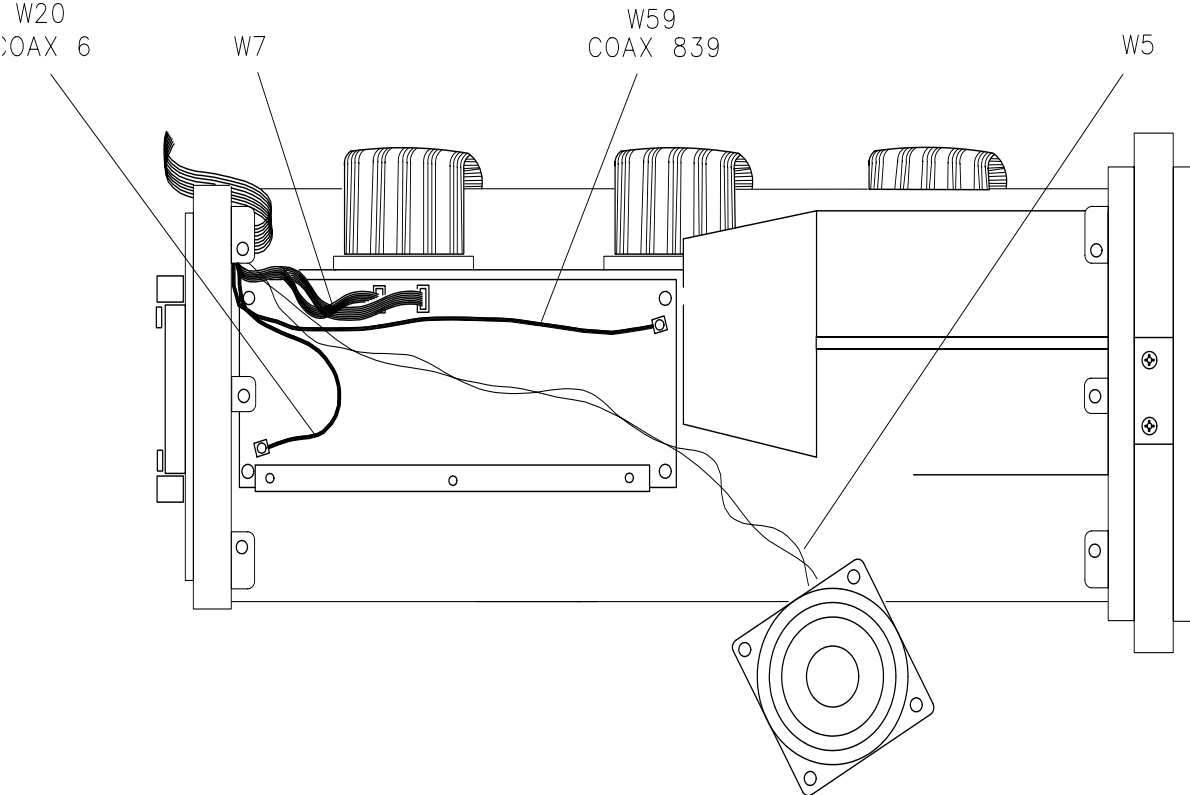
sj138e

Figure 6-10   8562E/EC Front End
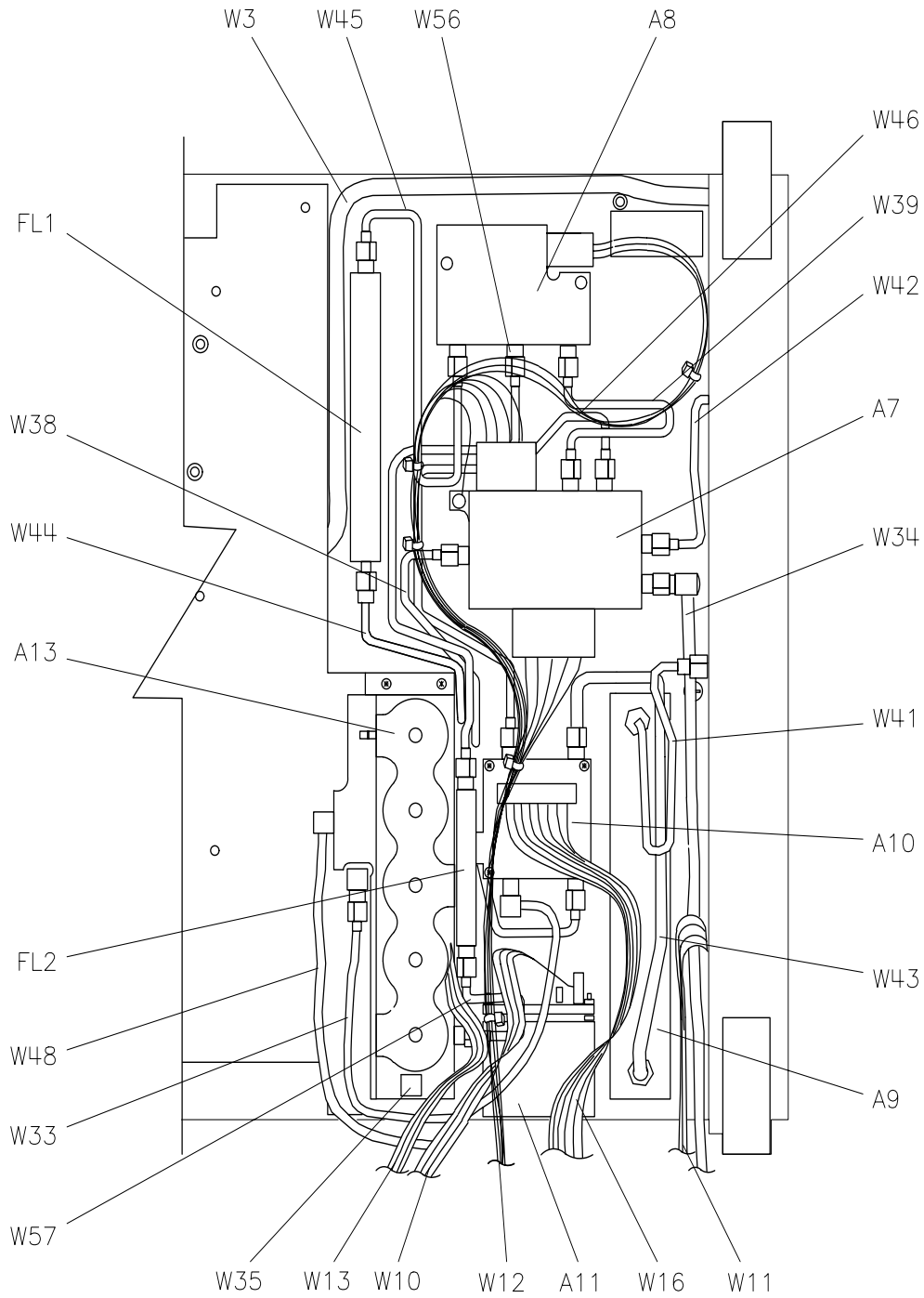
s l 120

Figure 6-11   **Rear View – 8562EC**
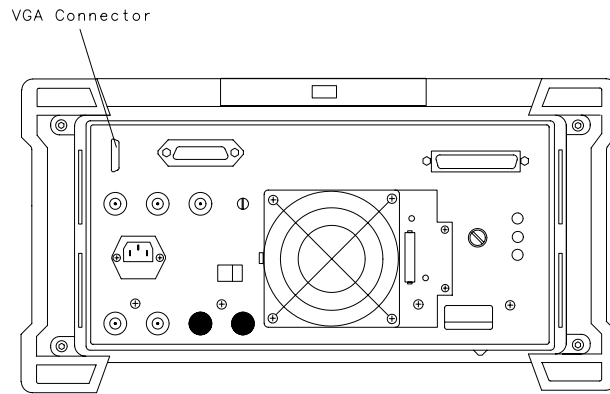
sj142c

Figure 6-12   **Rear View – 8562E**

FL4

BT1/A20

B1

SK162

7   General Troubleshooting
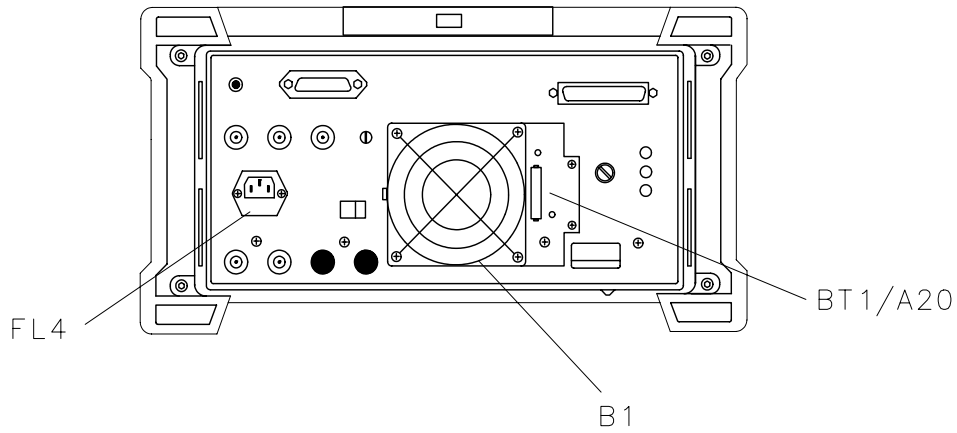
Introduction

This chapter provides information needed to troubleshoot your spectrum analyzer to one of the six major functional sections. Chapters 8 through 13 cover troubleshooting for each of these sections. Before troubleshooting, read the rest of this introduction. To begin troubleshooting, refer to "Troubleshooting to a Functional Section" on page 309.

NOTE When a part or assembly is replaced, adjustment of the affected circuitry is usually required. Refer to Chapter2 , "Adjustment Procedures."

WARNING **Troubleshooting and repair of this instrument without the cover exposes high voltage points that may, if contacted, cause personal injury. Maintenance and repair of this instrument should, therefore, be performed only by a skilled person who knows the hazards involved. Where maintenance can be performed without power applied, the power should be removed. When any repair is completed, be sure that all safety features are intact and functioning and that all necessary parts are connected to their grounds.**

Assembly Level Text

To locate troubleshooting information for an individual assembly, refer to Table 7-1 on page 310.

Block Diagrams

Instrument-level block diagrams are located at the end of this chapter. Power levels and voltages shown on block diagrams are provided as a troubleshooting aid only. They should not be used for making instrument adjustments.

Assembly Test Points

The spectrum analyzer board assemblies contain four types of test points: post, pad, extended component lead, and test jack. Figure 7-1 on page 303 illustrates each type of test point as seen on both block diagrams and circuit boards. The name of the test point will be etched into the circuit board next to the test point (for example, TP2). In some instances, the test point will be identified on the board by its number only.

Pad

Each pad test point uses a square pad and a round pad etched into the board assembly. The square pad is the point being measured. The round pad supplies a grounding point for the test probe.

Test Jack

The test jack is a collection of test points located on a 16-pin jack. There are approximately 20 test jacks used throughout the spectrum analyzer. The 85629B test and adjustment module uses the spectrum analyzer test jacks during diagnostic and adjustment procedures. The pins on the test jack may be manually probed, provided caution is used to prevent accidental shorting between adjacent pins.

Figure 7-1 on page 303 illustrates the pin configuration for the test jack. Line names are the same for all test jacks. The following mnemonics are used: MS (measured signal), TA (test and adjustment module address line), and OS (output signal). Test jack test points are identified on block diagrams by both the jack/pin number and line name.

Ribbon Cables

Ribbon cables are used extensively in the spectrum analyzer. The following five cables use different pin numbering methods on the jacks (signal names remain the same but the pin numbers vary):

W1, power cable
W2, control cable
W4, option cable
A3W1, interface cable
A19W1, GPIB cable

Figure 7-2 on page 304 and Figure 7-3 on page 305 illustrate the pin configurations of these five cables. Cables W1 and W2 use two pin numbering methods on their many jacks. These methods are identified in the interconnect and block diagrams by the letters "A" and "B" next to the jack designator (for example, J1(A)). Board assembly jacks connected to W1 will always be labeled J1. Board assembly jacks connected to W2 will always be labeled J2.

Figure 7-4 on page 306 shows the pin configuration for the 80 pin, W60 cable at J1 on the Display driver board on EC-series instruments. The numbering of the pins is identical on the A2 Controller board and the A17 Display Driver board.

Figure 7-1   Assembly Test Points

TEST POINTS ON BLOCK DIAGRAM

TEST POINTS ON CIRCUIT BOARD ASSEMBLY
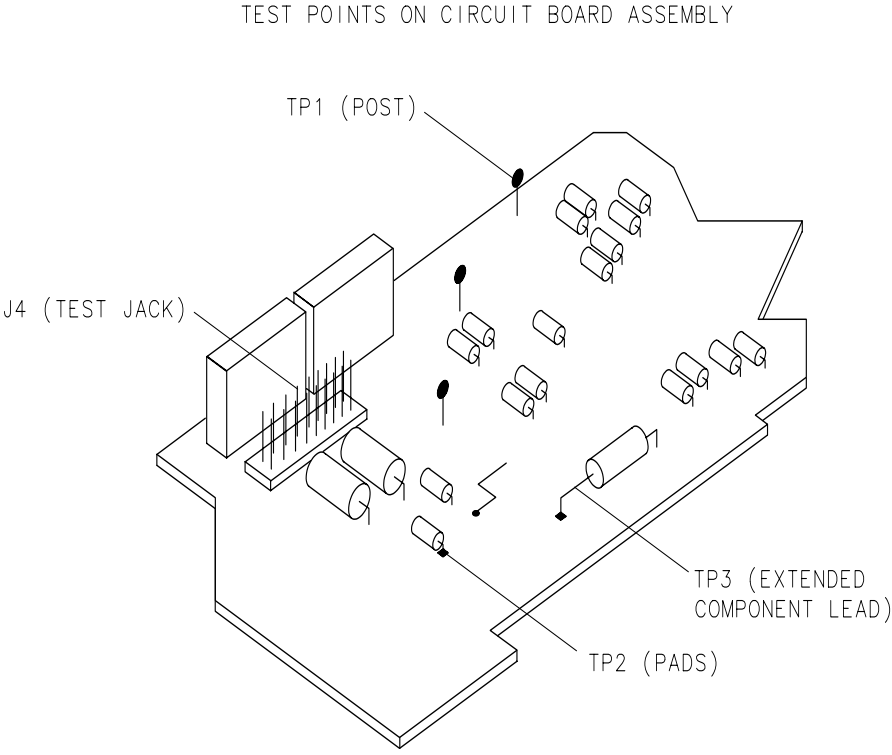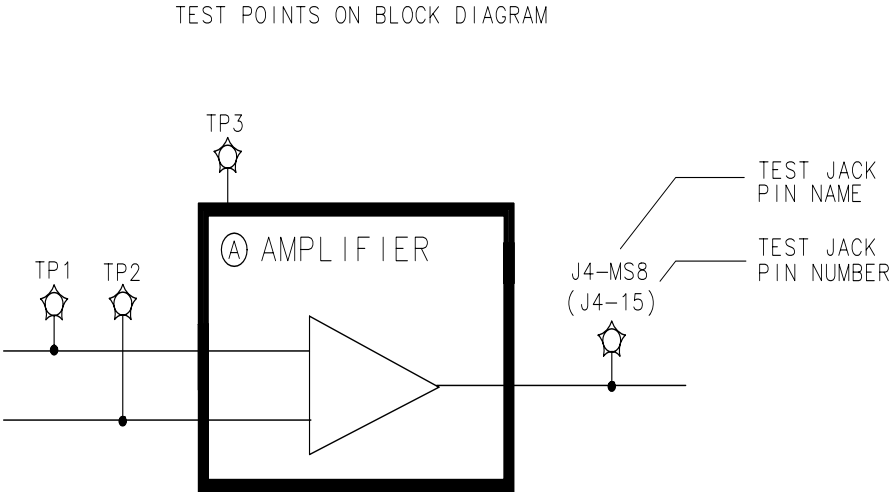
SK163

Figure 7-2   Ribbon Cable Connections (1 of 3)

```
                    A                                              B

        -15   ● 50   49 ● -15V                          -15V  ● 1    2 ● -15V
       +15V   ● 48   47 ● +15V        POWER FOR         +15V  ● 3    4 ● +15V
  LINE TRIG   ● 46   45 ● +28V       CONTROLLER    LINE TRIG  ● 5    6 ● +28V
        +5V   ● 44   43 ● +5V       AND INTERFACE        +5V  ● 7    8 ● +5V
        +5V   ● 42   41 ● +5V           ONLY             +5V  ● 9   10 ● +5V
        +5V   ● 40   39 ● +5V                            +5V  ● 11  12 ● +5V
      D GND   ● 38   37 ● D GND                        D GND  ● 13  14 ● D GND
      D GND   ● 36   35 ● D GND                        D GND  ● 15  16 ● D GND
      A GND   ● 34   33 ● A GND                        A GND  ● 17  18 ● A GND
      D GND   ● 32   31 ● D GND                        D GND  ● 19  20 ● D GND
        +5V   ● 30   29 ● +5V                            +5V  ● 21  22 ● +5V
        +5V   ● 28   27 ● +5V                            +5V  ● 23  24 ● +5V
       +15V   ● 26   25 ● +15V                          +15V ● 25  26 ● +15V
       -15V   ● 24   23 ● -15V                          -15V ● 27  28 ● -15V
     PWR UP   ● 22   21 ● +28V                        PWR UP ● 29  30 ● +28V
       +28V   ● 20   19 ● +15V                         +28V  ● 31  32 ● +15V
      A GND   ● 18   17 ● +15V                        A GND  ● 33  34 ● +15V
       -15V   ● 16   15 ● A GND                        -15V  ● 35  36 ● A GND
       -15V   ● 14   13 ● -12.6V (PROBE POWER)         -15V  ● 37  38 ● -12.6V (PROBE POWER)
      A GND   ● 12   11 ● NC                          A GND  ● 39  40 ● NC
SWEEP INPUT   ● 10    9 ● A GND           SWEEP INPUT        ● 41  42 ● A GND
         NC   ● 8     7 ● NC                            NC   ● 43  44 ● NC
      A GND   ● 6     5 ● NC                          A GND  ● 45  46 ● NC
         NC   ● 4     3 ● A GND                         NC   ● 47  48 ● A GND
         NC   ● 2     1 ● NC                            NC   ● 49  50 ● NC
```

W1
POWER CABLE
CONNECTIONS

*NOTE: Sweep Input for the Controller or Interface boards only.

```
                    A                                              B

         NC   ● 50   49 ● NC                            NC   ● 1    2 ● NC
         NC   ● 48   47 ● A GND                         NC   ● 3    4 ● A GND
         NC   ● 46   45 ● NC                            NC   ● 5    6 ● NC
      A GND   ● 44   43 ● +10V REF                    A GND  ● 7    8 ● +10V REF
         NC   ● 42   41 ● A GND                         NC   ● 9   10 ● A GND
         NC   ● 40   39 ● NC                            NC   ● 11  12 ● NC
      A GND   ● 38   37 ● LO 3 ERR                    A GND  ● 13  14 ● LO 3 ERR
    RF GAIN   ● 36   35 ● A GND                     RF GAIN  ● 15  16 ● A GND
         NC   ● 34   33 ● OFL ERR                       NC   ● 17  18 ● OFL ERR
         NC   ● 32   31 ● D GND                         NC   ● 19  20 ● D GND
         NC   ● 30   29 ● NC                            NC   ● 21  22 ● NC
      D GND   ● 28   27 ● NC                          D GND  ● 23  24 ● NC
         NC   ● 26   25 ● NC                            NC   ● 25  26 ● NC
         NC   ● 24   23 ● NC                            NC   ● 27  28 ● NC
         NC   ● 22   21 ● D GND                         NC   ● 29  30 ● D GND
        A7C   ● 20   19 ● NC                           A7C   ● 31  32 ● NC
        A5    ● 18   17 ● D GND                        A5    ● 33  34 ● D GND
        A4    ● 16   15 ● A3                           A4    ● 35  36 ● A3
        A2    ● 14   13 ● A1                           A2    ● 37  38 ● A1
      D GND   ● 12   11 ● A0                          D GND  ● 39  40 ● A0
        D7    ● 10    9 ● D6                           D7    ● 41  42 ● D6
        D5    ● 8     7 ● D GND                        D5    ● 43  44 ● D GND
        D4    ● 6     5 ● D3                           D4    ● 45  46 ● D3
        D2    ● 4     3 ● D1                           D2    ● 47  48 ● D1
      D GND   ● 2     1 ● D0                          D GND  ● 49  50 ● D0
```

W2
CONTROL CABLE
CONNECTIONS

sp149e

Figure 7-3   Ribbon Cable Connections (2 of 3)
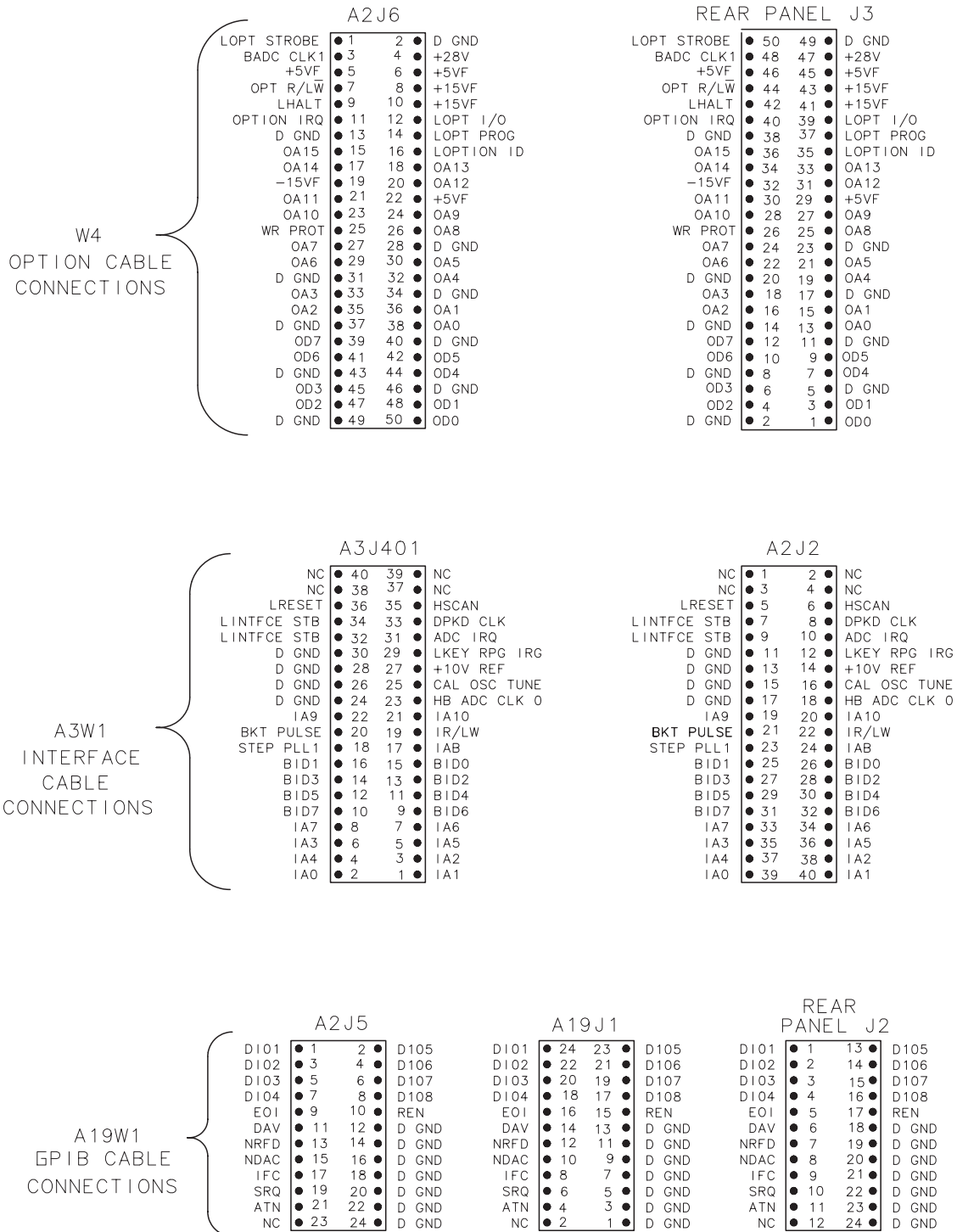
Figure 7-4   Ribbon Cable Connections (3 of 3) - EC-Series Only

GND SX	● 80			● 79	addrmsx2
addrmsx 3	● 78			● 77	GND SX
addrmsx 6	● 76			● 75	addrmsx 7
GND SX	● 74			● 73	addrmsx 10
addrmsx 11	● 72			● 71	GND SX
NC	● 70			● 69	NC
6ND SX	● 68			● 67	NC
NC	● 66			● 65	GND SX
NC	● 64			● 53	NC
GNDSX	● 62			● 61	DATAMSX 2
DATAMSX 3	● 60			● 59	GND SX
DATAMSX 6	● 58			● 57	DATAMSX 7
GND SX	● 56			● 55	DATAMSX 10
DATAMSX11	● 54			● 53	GNSD SX
DATAMSX 14	● 52			● 51	DATAMSX 15
GND SX	● 50			● 49	NC
_RESETMSX	● 48			● 47	GND SX
NC	● 46			● 45	+5V BKLTSX
+5VBKLTSX	● 44			● 43	+5VBKLTSX
+5VBLKTSX	● 42			● 41	+5VSX
addrmsx 1	● 40			● 39	GND SX
addrmsx 4	● 38			● 37	addrmsx 5
gnd sx	● 36			● 35	addrmsx 8
addrmsx 9	● 34			● 33	GND SX
ddrmsx 12	● 32			● 31	addrmsx 13
GND SX	● 30			● 29	NC
NC	● 28			● 27	GNDSX
NC	● 26			● 25	NC
GND SX	● 24			● 23	DATAMSX
DATAMSX 1	● 22			● 21	GND SX
DATAMSX 4	● 20			● 19	DATAMSX 5
GND SX	● 18			● 17	DATAMSX 8
DATAMSX 9	● 16			● 15	GND SX
DATAMSX 12	● 14			● 13	DATAMSX 13
GND SX	● 12			● 11	LMUX-INSX
EN1SX	● 10			● 9	GND SX
NC	● 8			● 7	NC
GND SX	● 6			● 5	+5VBKLTSX
+5V BKLTSX	● 4			● 3	+5VBKLTSX
+5V BKLTSX	● 2			● 1	+5VSX

sj114c

Figure 7-4 shows A2J8 connections on 8560 EC-Series Instruments. Lines 2 – 5 and 42 – 44 supply +5V to the two LCD backlights. Lines 1 and 41 supply +5V to the A17A1 Inverter board. Lines 1 – 6 and 41 – 44 are identical on A17J1.

Service Cal Data Softkey Menus

The jumper on A2J12 is shipped from the factory in the WR PROT (write protect) position (jumper on pins 2 and 3). When the jumper is set to the WR ENA (write enable) position (jumper on pins 1 and 2), an additional service cal data menu is displayed under **CAL**. illustrates those areas of the service cal data menu that are available.

Figure 7-5   **Service Cal Data Menu**


```
*   PRESEL ADJ key and the associated menu
    apply to the 8561E/8563E only.

†   BAND 1 MXR BIAS key applies to
    8561E only.
```
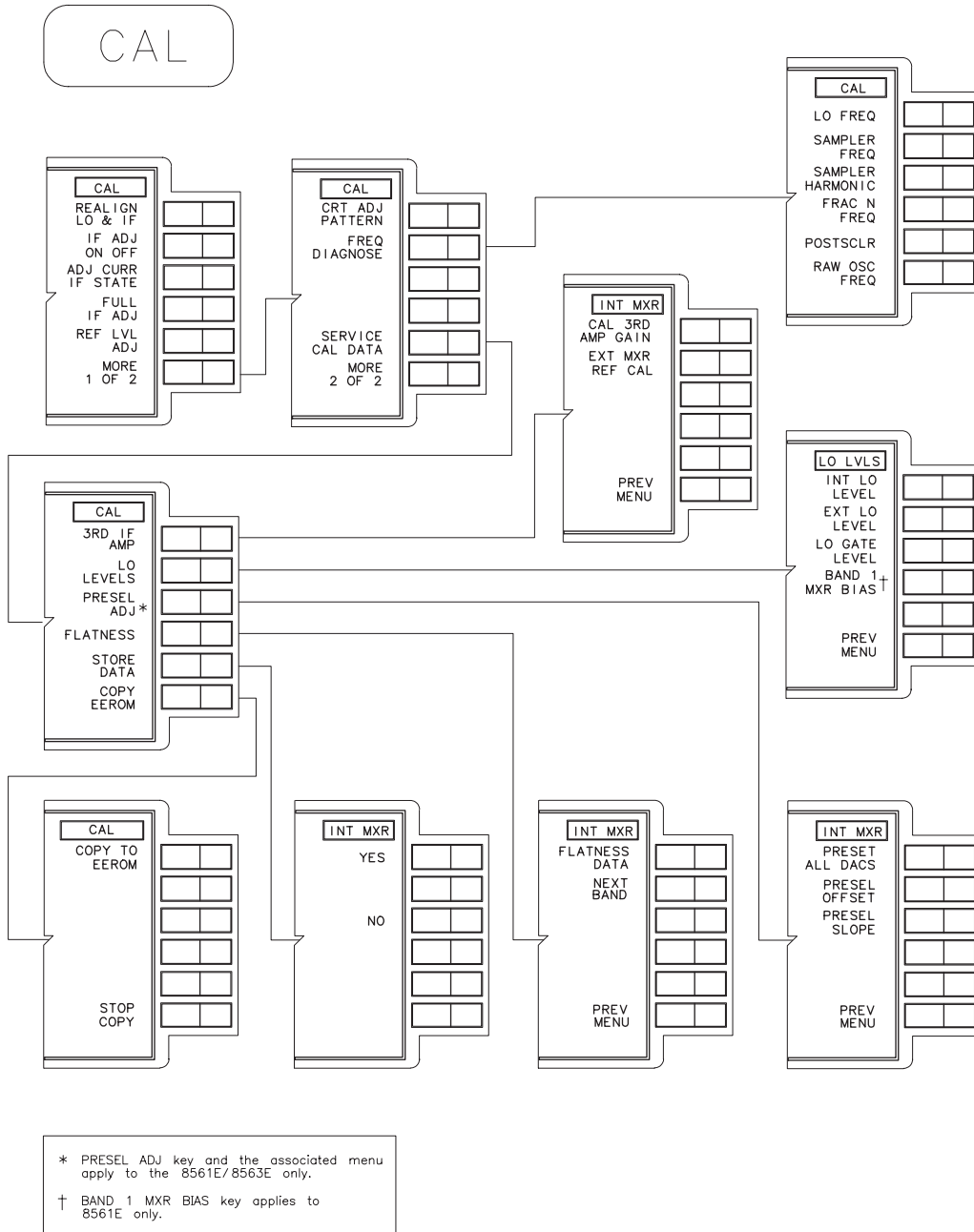
s j 143 e

Troubleshooting to a Functional Section

1. Refer to Table 7-1 on page 310 for the location of troubleshooting information.

2. If the 85629B test and adjustment module (TAM) is available, refer to "TAM (Test and Adjustment Module)" on page 311.

3. If error messages are displayed, refer to "Error Messages" on page 319. You will find both error descriptions and troubleshooting information.

4. If a signal cannot be seen, and no errors messages are displayed, the fault is probably in the RF Section. Refer to Chapter12 , "RF Section."

5. Blank displays result from problems caused by either the controller or display/power-supply sections. Because error messages 700 to 759 caused by the controller section cannot be seen on a blank display, use the following BASIC program to read these errors over GPIB. If the program returns an error code of 0, there are no errors.

```
10 DIM Err$[128]

20 OUTPUT 718;"ERR?;"

30 ENTER 718; Err$

40 PRINT Err$

50 END
```

   a. If there is no response over GPIB, set an oscilloscope to the following settings:

      Sweep time .... 2 ms/div
      Amplitude scale ....1 V/div

   b. The signals at A2J202 pin 3 and pin 14 should measure about 4 V p-p. If the levels are incorrect, refer to Chapter 10 , "Controller Section," and troubleshoot the A2 controller assembly.

   c. Set the oscilloscope to the following settings:

      Sweep time .... 1 ms/div
      Amplitude scale ....2 V/div

   d. The signal at A2J202 pin 15 should consist of TTL pulses. If the signal is at a constant level (high or low), troubleshoot the A2 controller assembly.

6. Display problems such as intensity or distortion are caused by either the controller or display/power-supply sections. Refer to Chapter 10 , "Controller Section," or Chapter13 , "Display/Power Supply Section."

Table 7-1 **Location of Assembly Troubleshooting Text**

Instrument Assembly	Location of Troubleshooting Text
A1A1 keyboard	Chapter 8. ADC/Interface Section
A1A2 RPG	Chapter 8. ADC/Interface Section
A2 controller	Chapter 10. Controller Section
A3 interface	Chapter 8. ADC/Interface Section Chapter 9. IF Section
A4 log amplifier/cal oscillator	Chapter 9. IF Section
A5 IF	Chapter 9. IF Section
A6 power supply	Chapter 13. Display/Power Supply Section
A6A1 HV module	Chapter 13. Display/Power Supply Section
A7 SLODA	Chapter 12. RF Section
A8 low band mixer	Chapter 12. RF Section
A9 input attenuator	Chapter 12. RF Section
A10 RYTHM	Chapter 12. RF Section
A11 YTO	Chapter 11. Synthesizer Section
A13 2nd converter	Chapter 12. RF Section
A14 frequency control	Chapter 11. Synthesizer Section Chapter 12. RF Section
A15 RF assembly	Chapter 11. Synthesizer Section Chapter 12. RF Section
A17 CRT driver	Chapter 13. Display/Power Supply Section
A18 CRT	Chapter 13. Display/Power Supply Section
A19 GPIB	Chapter 10. Controller Section
A21 OCXO	Chapter 11. Synthesizer Section
A22 Display Driver	Chapter 13. Display/Power Supply Section
A23 LCD Display	Chapter 13. Display/Power Supply Section
FL1, FL2	Chapter 12. RF Section

TAM (Test and Adjustment Module)

When attached to the spectrum analyzer rear panel, the 85629B test and adjustment module (TAM), in conjunction with the 8562E/TAM Interface Software, provides diagnostic functions for supporting the 8562E/EC spectrum analyzer. Because the TAM is connected directly to the spectrum analyzer internal data and address bus, it controls the spectrum analyzer hardware directly through firmware control. It would be impossible to control the hardware to the same extent either from the spectrum analyzer front panel or over the GPIB.

The TAM by itself will not support the 8562E/EC; it will not recognize model number "8562E" which is stored in the analyzer EEROM. Fortunately, 95% of the hardware in the 8562E/EC is common to other 8560 E-Series and EC-Series analyzers which are recognized by the TAM. The 8562E/TAM Interface Software enables use of the TAM with the 8562E/EC by modifying the spectrum analyzer "ID String" (the model number and option information stored in EEROM) to include a recognized model number (8560E, 8561E, or 8563E). The model number chosen depends upon which TAM function is desired.

Once the model number is changed to one of the recognized model numbers, the selected TAM function can be run as it normally would on the recognized model number spectrum analyzer. Some TAM functions have limitations when used on an 8562E/EC. These limitations are noted on the computer display.

The TAM measures voltages at key points in the circuitry and flags a failure whenever the voltage falls outside the limits. The TAM locates the failure to a small functional area which can be examined manually. Remember the following when using the TAM:

- Be sure the spectrum analyzer power is turned off when installing or removing the TAM.

- Use the **HELP** softkey (found in all menus) for useful information.

- Press **MODULE** to return to the TAM main menu.

- The TAM acts as the active controller on the GPIB bus. Press the **PASS CONTROL** softkey on the computer keyboard to remove the computer as the active controller.

Loading and Running the 8562E/TAM Interface Software (TAM I/F SW)

The TAM I/F SW requires an HP 9000, Series 200 or Series 300 controller and an HP BASIC operating system as described in the instructions for using the Frequency Response Adjustment Software in Chapter 3 , "Frequency Response Adjustment Software." The TAM I/F SW requires 500 kilobytes of free memory after the operating system is loaded.

Loading the software

1. Connect a GPIB cable from the controller GPIB port to the GPIB port on the 8562E/EC. Turn the 8562E/EC power on.

The WR PROT/WR ENA jumper on the A2 Controller board should be set to the WR ENA position. Moving this jumper requires removal of the instrument cover.

2. Download the 8562E/EC TAM Interface software to a drive accessible by the test computer.

3. Use the MSI (Mass Storage Is) command to make the drive where the software is stored the mass storage device. For example, you would type MSI ":,700,1" if using a flexible disk located at 700,1.

4. Type LOAD "TAM_IFSW",1 and press **RETURN** or **EXECUTE**. The program will run immediately after it is loaded.

GPIB addresses

The program queries the spectrum analyzer for its ID string and serial number. The program assumes the spectrum analyzer GPIB address is 718. If it is something other than 718, use the up/down arrow keys on the computer to place the pointer next to Spectrum Analyzer polling address and press **CHANGE ENTRY**. When entering a GPIB address, also include the select code. For example, if the analyzer were at address 23 on a GPIB interface at select code 14, you would enter 1423 as the polling address.

Data files and system mass storage files

The TAM I/F SW program creates a data file for each 8562E/EC it is used with. This data file contains the original ID string and serial number of the spectrum analyzer. The filename is in the form: "HP62Exxxxx", where xxxxx is the last five digits of the spectrum analyzer serial number. These data files are stored in the location listed as the system mass storage file location. The default location is the location from where the program was loaded.

If the system mass storage file location is more than 37 characters, the first 17 characters will be displayed, followed by three periods (…), and

- If you wish to change the system mass storage file location, use the up/down arrow keys to point to "System mass storage file location" and press **CHANGE ENTRY**. You will then be prompted to enter a new mass storage file location.

- If the polling address or the mass storage file location were changed, press **QUERY DUT**.

Executing a test

1. To execute a particular test, adjustment, or diagnostic function, press the appropriate menu softkey; for example, press **TEST MENU** to access a TAM test function.

   The Test Menu, Adjustments Menu, and Diagnostics Menu all function similarly. A listing of all available TAM functions are given, followed by the model number to which the ID string will be changed to execute that function, and any limitations which apply to using that function. For example, selection 3 in the Diagnostics Menu reads:

   ```
   3) RF Path Fault Isolation 8561E Checks up to 5 GHz
   ```

   If RF Path Fault Isolation is selected, the ID string will be changed to 8561E. When the diagnostic is run, it will only check the RF path up to 5 GHz (a frequency approximately in the middle of the highest band of the 8561E).

2. Move the pointer to the desired function and press **SELECT**. The display will indicate the spectrum analyzer serial number, the function selected, and the new ID string to be sent to the analyzer.

3. Press **WRITE NEW ID$** to change the analyzer ID string. When prompted, cycle the spectrum analyzer power; the new ID string is only read from EEROM at power-up.

4. After the power-on self-realignments are complete, press **PASS CONTROL**. This removes the computer as being the active controller on GPIB, permitting the TAM to be the active controller.

5. The TAM functions are now available and are listed, along with any limitations. For example, if `Automatic Fault Isolation` were selected from the Diagnostics Menu, the ID string would be changed to 8561E. For an 8561E, all TAM diagnostics can be used on an 8562E/EC, except for Manual Probe Troubleshooting.

   You can now execute any of the TAM functions listed without further computer interaction.

6. Press **RESUME CONTROL** to execute an unlisted TAM function. This changes the ID string in EEROM back to 8562E, and shows the complete menu of available TAM functions.

NOTE   The analyzer will always behave like the model number emulated from
        the last TAM function, even though the ID string in the EEROM was
        changed back to 8562E. The analyzer will not revert back to an 8562E
        until power is cycled, but that is not yet necessary.

7. Before exiting the TAM I/F SW program, press **RESTORE DUT ID$**.

NOTE   The amount of free disk space for the system mass storage file location
        will decrease over time, since a data file is created for each 8562E/EC
        used with this program. Once a repair is completed for a given
        8562E/EC, its associated data file can be purged. A good rule of thumb
        is to purge any data file which is more than 1 month old.

TAM Requirements

For the TAM to function properly, certain parts of the spectrum
analyzer must be operating properly. These include the CPU, parts of
the program ROM and program RAM, the keyboard and keyboard
interface, and the display.

Even though the TAM communicates to the operator via the display,
some display problems can be troubleshot using the TAM. This is
possible by using the **Print Page** softkey. Even if the display is dead,
Print Page is still active. Refer to Chapter 13 , "Display/Power Supply
Section," for instructions on using the TAM when the display is not
functioning.

Test Connectors

The TAM uses a built-in dc voltmeter and DAC to measure voltages on
any one of the "test connectors" (or test jacks) located throughout the
spectrum analyzer.

Revision Connectors

One test connector on each assembly is reserved as a "revision
connector." The TAM uses the revision connector to identify the
assembly design revision. A "revision voltage" placed onto one
measured signal line (MSL) pin, indicates design changes.

The TAM must be plugged into the revision connector first to determine
which tests to use for the assembly. If the revision connector has not
been probed, a message will appear instructing you to connect the probe
to the revision connector and press **TEST**. You can then probe the rest of
the assembly connectors.

NOTE   If the revision of the PC board is newer than the TAM, a message will be displayed stating that the revision code for this board is not known by this module. The choices presented are to use the test for the latest known revision board, measure only voltages, or exit. In general, most points will not change from one board revision to another, so using the most current tests is still very useful. However, any failure should be verified using the manual troubleshooting procedures before doing a repair.

Inconsistent Results

Many of the signals measured by the TAM are digitally controlled. If inconsistent results are obtained, or if failures appear in unrelated areas, the digital control may be at fault. Refer to the manual troubleshooting procedures for those assemblies to isolate those failures.

Erroneous Results

If the TAM manual probe troubleshooting seems to be giving erroneous results, its performance can be checked by placing the probe on the TAM test connector (A2J11) located on the A2 controller assembly and executing the manual probe diagnostics. If either of the tests fail, the TAM is malfunctioning and should be serviced.

Blank Display (8562E only)

It is possible to use the TAM manual probe troubleshooting without a display if a GPIB printer is available. Refer to Chapter 13 , "Display/Power Supply Section," for more information.

Automatic Fault Isolation

Automatic fault isolation (AFI) is designed to isolate most faults to one or two assemblies. AFI can be run with the spectrum analyzer cover in place and requires only the CAL OUTPUT signal as a stimulus. The entire procedure takes less than 2 minutes to complete if no failures are found.

AFI performs checks of five functional areas in a pre-defined sequence. The sequence minimizes the chance of making false assumptions. The TAM checks the spectrum analyzer "from the inside out." For example, the ADC is checked before the IF is checked. This ensures that if no signal is detected through the IF, the fault is in the IF section and not a faulty ADC. The ADC measures the video signal from the IF section.

The sequence of checks is as follows:

1. Controller check

2. ADC/interface check

3. IF/log check

4. LO control check

5. RF low band check

NOTE

Only the low band of the spectrum analyzer is checked by AFI. This is because the only stimulus to the RF section is from the 300 MHz CAL OUTPUT signal. A signal greater than 2.9 GHz would be required to check the high band path.

Display/Power Supply

AFI cannot check the display/power-supply section because this section powers the TAM and provides the display of AFI results.

Controller Check (8562E only)

The TAM performs a check-sum of all ROMs, RAMs, and the EEROM. The CPU is also checked, since parts of the CPU could be nonfunctional while the TAM still operates. These checks are very similar to those done by the spectrum analyzer at power-on.

ADC/Interface Check

The keyboard interface and strobe-select circuitry must be functioning correctly, since these are required to operate the TAM. The TAM checks the ADC by attempting to measure three signals from three different locations. This ensures that an open or short in one cable will not hide the fact that the ADC is operating satisfactorily. The analog bus (W2 control cable) is checked by sending data out on the data lines and reading the data back. If this check fails, disconnect one board at a time and rerun AFI to determine if an assembly causes the problem. If the fault remains with all assemblies disconnected from W2, troubleshoot W2 or the A3 interface assembly.

IF/LOG Check

The TAM uses the cal oscillator on the A4 assembly as the stimulus for checking the IF section. If the signal is undetected, the TAM repeats the test with a signal originating from the RF section. Presence of this signal through the IF indicates a faulty cal oscillator.

LO Control Check

The LO control check verifies that all phase-lock loops (PLLs) in the synthesizer section lock. Some oscillators are checked to ensure that they will lock outside their normal operating frequency range. The TAM also performs an operational check on several DACs in the synthesizer section.

RF Low Band Check   The TAM tests the operation of the A8 low band mixer, the A9 input attenuator, the A10 YIG-tuned filter/mixer (RYTHM), the second IF distribution, the third converter (A15), and most of the A13 second converter.

AFI also checks the flatness compensation amplifiers (part of the A15 RF assembly), ensuring that their gain can be adjusted over a certain range.

If no signal is detected through the RF section, AFI will substitute the 298 MHz SIG ID oscillator, if present, for the third LO while simultaneously decreasing the first LO frequency by 2 MHz. If a signal can now be detected, troubleshoot the third LO driver amplifier on the A15 RF assembly.

Manual Probe Troubleshooting

Manual probe troubleshooting probes the instrument test connectors to perform the following types of measurements:

- Amplifier and oscillator dc current draw by monitoring the voltage across a resistor of known value.

- Oscillator tune voltages ensuring proper operation of phase/frequency detectors and loop integrators.

- Static bias voltages.

- DAC output voltages.

If probing a connector for a check yields a "FAIL" indication, select the desired check using either the knob or step keys and press **More Info**. A description of the function checked (with measured and expected voltages or currents) is displayed with a list of additional areas to check. These areas can sometimes be checked by looking at another TAM connector, but usually require manual troubleshooting techniques to isolate the problem further. If a GPIB printer is connected, press **Print Page** to provide a hard copy of the currently displayed screen (the softkey labels will not be printed).

Each test connector has fifteen pins (one pin is missing to act as a key). The pins contain eight measured signal lines (measured signal lines denoted as MS1 through MS8), one input signal line (OS1), one ground, and five pins encoding a five-bit connector address.

The TAM needs to probe each assembly revision connector once; subsequent readings are not necessary. It is possible, for example, to probe the A5 IF assembly, then the A4 log amplifier assembly, and then return to A5 without having to re-probe A5 revision connector. However, the revision connector must be re-probed if the spectrum analyzer is returned to normal operation and then back to TAM control. (This is also true if the spectrum analyzer is turned off.)

RF Path Fault Isolation

RF path fault isolation checks high-band RF paths. (Automatic fault isolation checks the low-band RF path.) An external microwave source with a frequency range of 5 GHz to 13.2 GHz is required. The source is not controlled over GPIB. The user is prompted by the TAM to set the source to 5 GHz at –10 dBm. (The TAM expects –10 dBm at the input of the spectrum analyzer; the amplitude at the source output may have to be higher to account for cable loss.)

The source also provides a signal for high band. The TAM checks the operation of the A9 input attenuator. The TAM checks the A10 YIG-tuned filter/mixer at 5 GHz. If no signal is present, the TAM will use the 298 MHz SIG ID oscillator, if present, as is done in AFI.

Calibration Oscillator Troubleshooting Mode

The cal osc troubleshooting mode enables front-panel control of the cal oscillator on the A4 assembly. The cal oscillator can be fixed-tuned to three different frequencies. The cal oscillator may also be set to one of four sweep widths, centered at 10.7 MHz. Fixed-tuned settings:

11.5 MHz

10.7 MHz

9.9 MHz

Sweep-width settings:

20 kHz

10 kHz

4 kHz

2 kHz

The cal osc troubleshooting mode sends the cal oscillator output (–35 dBm) to the A5 IF assembly. On the A5 IF assembly all crystal filter poles are shorted, all LC poles are enabled, and the 15 dB attenuator is disabled. Signals from the RF section are attenuated as much as possible.

Error Messages

The spectrum analyzer displays error messages in the lower right-hand corner of the display. A number, or error code, is associated with each error message. These error messages alert the user to errors in spectrum analyzer function or use.

Multiple error messages may exist simultaneously. Refer to "Viewing Multiple Messages" on page 320.

The following information can be found in this section:

Viewing Multiple Messages
Error Message Elimination
System Analyzer Programming Errors (100 to 150)
ADC Errors (200 to 299)
LO and RF Hardware/Firmware Failures (300 to 399)
   YTO Loop Errors (300 to 301)
   Roller PLL Errors (302 to 316)
   YTO Loop Errors (317 to 320)
   Roller Oscillator Errors (321 to 329)
   YTO Loop Error (331)
   600 MHz Reference Loop (333)
   YTO Leveling Loop (334)
   Sampling Oscillator (335)
   10 MHz Reference (336)
   Fractional N PLL (337)
   YTO Loop Settling Errors (351 to 354)
   Sampling Oscillator (355)
   Span Accuracy Calibration Errors (356 to 361)
Automatic IF Errors (400 to 599)
System Errors (600 to 651)
Digital and Checksum Errors (700 to 799)
   EEROM Checksum Errors (700 to 704)
   Program ROM Checksum Errors (705 to 710)
   RAM Check Errors (711 to 716)
   Microprocessor Error (717)
   Battery Problem (718)
   Model Number Error (719)
   System Errors (750 to 759)
   Fast ADC Error (760)
Option Module Errors (800 to 899)
User Generated Errors (900 to 999)

Viewing Multiple Messages

Although multiple errors may exist, the spectrum analyzer displays only one error message at a time. To view any additional messages, do the following:

1. Press **RECALL** and **MORE 1 OF 2**.

2. Press **RECALL ERRORS**. An error message is displayed in the active function block.

3. Use the up and down step keys to scroll through any other error messages which might exist, making note of each error code.

Error Message Elimination

When an error message is displayed, always perform the following procedure:

1. Press **SAVE** and **SAVE STATE**.

2. Store the current state in a convenient STATE register. (It may be necessary to set **SAVELOCK** to OFF.)

3. Press **CAL** and **REALIGN LO &IF**. Wait for the sequence to finish.

4. Press **RECALL** and **RECALL STATE**.

5. Recall the previously stored STATE.

6. If an error message is still displayed, refer to the list of error messages below for an explanation of the error messages.

System Analyzer Programming Errors (100 to 150)

Refer to the *8560 E-series and EC-series Spectrum Analyzer User's Guide* for information on programming the spectrum analyzer.

100 NO PWRON Power-on state is invalid; default state is loaded. Press **SAVE**, **PWR ON STATE** to clear error message.

101 NO STATE State to be RECALLed not valid or not SAVEd.

106 ABORTED! Current operation is aborted; GPIB parser reset.

107 HELLO ?? No GPIB listener is present.

108 TIME OUT Analyzer timed out when acting as controller.

109 CtrlFail Analyzer unable to take control of the bus.

110 NOT CTRL Analyzer is not system controller.

111 # ARGMTS Command does not have enough arguments.

112 ??CMD?? Unrecognized command.

113 FREQ NO! Command cannot have frequency units.

114 TIME NO! Command cannot have time units.

115 AMPL NO! Command cannot have amplitude units.

116 ?UNITS?? Unrecognizable units.

117 NOP NUM Command cannot have numeric units.

118 NOP EP Enable parameter cannot be used.

119 NOP UPDN UP/DN are not valid arguments for this command.

120 NOP ONOF ON/OFF are not valid arguments for this command.

121 NOP ARG AUTO/MAN are not valid arguments for this command.

122 NOP TRC Trace registers are not valid for this command.

123 NOP ABLK A-block format not valid here.

124 NOP IBLK I-block format not valid here.

125 NOP STRNG Strings are not valid for this command.

126 NO ? This command cannot be queried.

127 BAD DTMD Not a valid peak detector mode.

128 PK WHAT? Not a valid peak search parameter.

129 PRE TERM Premature A-block termination.

130 `BAD TDF` Arguments are only for TDF command.

131 `?? AM/FM` AM/FM are not valid arguments for this command.

132 `!FAV/RMP` FAV/RAMP are not valid arguments for this command.

133 `!INT/EXT` INT/EXT are not valid arguments for this command.

134 `??? ZERO` ZERO is not a valid argument for this command.

135 `??? CURR` CURR is not a valid argument for this command.

136 `??? FULL` FULL is not a valid argument for this command.

137 `??? LAST` LAST is not a valid argument for this command.

138 `!GRT/DSP` GRT/DSP are not valid arguments for this command.

139 `PLOTONLY` Argument can only be used with PLOT command.

140 `?? PWRON` PWRON is not a valid argument for this command.

141 `BAD ARG` Argument can only be used with FDIAG command.

142 `BAD ARG` Query expected for FDIAG command.

143 `NO PRESL` No preselector hardware to use command with.

144 `COUPL??` Invalid COUPLING argument, expected AC or DC.

ADC Errors (200 to 299)

These errors are directly related to the ADC/interface section. Suspect a faulty A2 controller, A3 interface assembly or, in 8560 E-series analyzers, the A16 fast ADC (FADC) assembly (Option 007).

Errors 202 through 207 apply only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

200 `SYSTEM` ADC driver/ADC hardware/firmware interaction; check for other errors.

201 `SYSTEM` ADC controller/ADC hardware/firmware interaction; check for other errors.

202 `FADC CAL` Binary search failed during FADC linear offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

203 `FADC CAL` Binary search failed during FADC log offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

`204 FADC CAL` Binary search failed during FADC log expand offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

`205 FADC CAL` Slope derivation failed during FADC linear offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

`206 FADC CAL` Slope derivation failed during FADC log offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

`207 FADC CAL` Slope derivation failed during FADC log expand offset calibration.

This error applies only to EC-series analyzers and E-series analyzers with fast ADC (Option 007).

`250 OUTOF RG` ADC input is outside of ADC range.

`251 NO IRQ` Microprocessor not receiving interrupt from ADC.

LO and RF Hardware/Firmware Failures (300 to 399)

YTO Loop Errors (300 to 301)

These errors often require troubleshooting the A14 frequency control assembly (synthesizer section) or the ADC circuits.

`300 YTO UNLK` YTO (first LO) phase locked loop is unlocked. The ADC measures YTO_ERR voltage under phase-lock condition.

`301 YTO UNLK` YTO (first LO) phase locked loop is unlocked. Same as ERR 300 except ERR 301 is set if the voltage is outside certain limits.

Roller PLL Errors (302 to 316)

These errors indicate a faulty roller oscillator on the A14 frequency control assembly. Refer to Chapter11 , "Synthesizer Section." The A3 interface ADC circuits may also be faulty. If error codes 333 and 499 are present, suspect the 10 MHz reference, the A21 OCXO, or on the A15 assembly (Option 103). These errors do not apply to the hardware in an 8560 E-series or EC-series spectrum analyzer. If they occur in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`302 OFF UNLK` Offset roller oscillator PLL is unlocked. May indicate loss of 10 MHz reference. The 10 MHz reference should measure greater than –7 dBm at A15J303. The ADC measures OFFSENSE at the beginning of each sweep and, if the voltage is outside certain limits, the offset oscillator pretune DAC is adjusted to bring OFFSENSE within the proper range. ERR 302 is set if this cannot be accomplished. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`303 XFR UNLK` Transfer roller oscillator PLL is unlocked. May indicate loss of 10 MHz reference. The 10 MHz reference should measure greater than –7 dBm at A15J303. The ADC measures XFRSENSE at the beginning of each sweep and, if the voltage is outside certain limits, the transfer oscillator pretune DAC is adjusted to bring XFRSENSE within the proper range. ERR 303 is set if this cannot be accomplished. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

304 ROL UNLK Main roller oscillator PLL is unlocked. May indicate loss of 10 MHz reference. The 10 MHz reference should measure greater than –7 dBm at A15J303. The ADC measures MAINSENSE at the beginning of each sweep and, if the voltage is outside certain limits, the main roller pretune DAC is adjusted to bring OFFSENSE within the proper range. ERR 304 is set if this cannot be accomplished. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

305 FREQ ACC Unable to adjust MAINSENSE close to 0 volts using the coarse adjust DAC. The coarse adjust and fine adjust DAC are used together to set MAINSENSE to 0 volts with the loop opened. ERR 305 is set if the coarse adjust DAC cannot bring MAINSENSE close enough to 0 volts for the fine adjust DAC to bring MAINSENSE to exactly 0 volts. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

306 FREQ ACC Unable to adjust MAINSENSE to 0 volts using the fine adjust DAC. The coarse adjust and fine adjust DAC are used together to set MAINSENSE to 0 volts with the loop opened. ERR 306 is set if the fine adjust DAC cannot bring MAINSENSE to 0 volts. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

307 FREQ ACC Transfer oscillator pretune DAC out of range. The transfer oscillator pretune procedure attempts to find pretune DAC values by programming the PLL to 25 different frequencies and incrementing the transfer oscillator pretune DAC until XFRSENSE changes polarity. ERR 307 is set if the DAC is set to 255 (maximum) before XFRSENSE changes polarity. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`308 FREQ ACC` Offset oscillator pretune DAC not within prescribed limits at low frequency. The offset oscillator pretune DAC is set to provide a frequency less than 189 MHz while the PLL is programmed for 189 MHz. ERR 308 is set if XFRSENSE is greater than +5 V (it should be at the negative rail). This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`309 FREQ ACC` Offset oscillator pretune DAC not within prescribed limits at high frequency. The offset oscillator pretune DAC is set to provide a frequency less than 204 MHz while the PLL is programmed for 204 MHz. ERR 309 is set if XFRSENSE is greater than +5 V (it should be at the negative rail). This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`310 FREQ ACC` Main roller pretune DAC set to 255. The main roller pretune DAC is set to 5, causing MAINSENSE to go to the positive rail. The DAC is incremented until MAINSENSE changes polarity. ERR 310 is set if the DAC is set to 255 before MAINSENSE changes to a negative polarity. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`311 FREQ ACC` Main roller pretune DAC set to 255. The main roller pretune DAC is set to 5, causing MAINSENSE to go to the positive rail. The DAC is incremented until MAINSENSE changes polarity. ERR 311 is set if the DAC is set to 255 before MAINSENSE changes to a negative polarity. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

312 FREQ ACC Unable to adjust MAINSENSE to 0 volts using the fine adjust DAC. The coarse adjust and fine adjust DAC are used together to set MAINSENSE to 0 volts with the loop opened. ERR 312 is set if the fine adjust DAC cannot bring MAINSENSE to 0 volts. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

313 FREQ ACC Error in LO synthesis algorithm. ERR 313 is set if a combination of sampler oscillator and roller oscillator frequencies could not be found to correspond to the required YTO start frequency. Contact the factory. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

314 FREQ ACC Indicates problems in the span calibration. Troubleshoot any unlocks before attempting to troubleshoot span calibration problems, because the loops must all lock in order to perform the calibration. If LO spans greater than 1 MHz are correct, check A14U114B, A14U115A, A14U116, or A14Q101. This error message appears when the main roller oscillator sweep sensitivity is 0. A sweep ramp is injected into the locked main roller loop which should generate a negative-going ramp on MAINSENSE. ERR 314 is set if the slope of this ramp is 0. This is an indication of an unlocked main roller loop or lack of a sweep ramp. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`315 FREQ ACC` Indicates problems in the span calibration. Troubleshoot any unlocks before attempting to troubleshoot span calibration problems, because the loops must all lock in order to perform the calibration. If LO spans greater than 1 MHz are correct, check A14U114B, A14U115A, A14U116, or A14Q101. This error message appears when the roller span attenuator DAC is out of range. This DAC value is recalculated each time there are changes to the span or start frequency. ERR 315 is set if this value is less than 10 or greater than 245. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

`316 FREQ ACC` Sensitivity of main roller pretune DAC is 0. Once the main roller is locked, the MAINSENSE voltage is measured and the pretune DAC value is incremented by two. ERR 316 is set if the difference between the new MAINSENSE voltage and the previous MAINSENSE voltage is 0. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

YTO Loop Errors (317 to 320)

These messages indicate that the YTO main coil coarse DAC (ERR 317) or fine DAC (ERR 318) is at its limit. If error codes 300 or 301 are not present, a hardware problem exists in the YTO loop but the loop can still acquire lock. Refer to Chapter 11 , "Synthesizer Section," to troubleshoot the YTO PLL. The ADC circuit on the A3 interface assembly may also cause this error.

317 FREQ ACC Main coil coarse DAC at limit. The main coil coarse DAC is set to bring YTO ERR close enough to 0 volts for the main coil fine DAC to bring YTO ERR to exactly 0 volts. ERR 317 is set if the main coil coarse DAC is set to one of its limits before bringing YTO ERR close enough to 0 volts.

318 FREQ ACC Main coil fine DAC at limit. The main coil fine DAC is set to bring YTO ERR to 0 volts after the main coil coarse DAC has brought YTO ERR close to 0 volts. ERR 318 is set if the main coil fine DAC is set to one of its limits before bringing YTO ERR to 0 volts.

319 WARN COA YTO coarse tune DAC near limit.

320 WARN FIN YTO fine tune DAC near limit.

Roller Oscillator Errors (321 to 329)

These errors indicate a faulty roller oscillator on the A14 frequency control assembly. The A3 interface ADC circuits may also be faulty. If error codes 333 and 499 are also present, suspect the 10 MHz reference, the A21 OCXO, or the A15 assembly (Option 103). These errors do not apply to the hardware in an 8560 E-series or EC-series spectrum analyzer. If they occur in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

321 FREQ ACC Main roller tuning sensitivity is not greater than 0. The MAINSENSE voltage is noted in a locked condition and the main roller is programmed to a frequency 400 kHz higher. ERR 321 is set if the new MAINSENSE voltage is not greater than the previous MAINSENSE voltage. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

322 FREQ ACC Main roller pretune DAC value set greater than 255. During the LO adjust sequence, the main roller is locked and then programmed to a frequency 1.6 MHz higher. A new pretune DAC value is calculated based upon the main roller tuning sensitivity. ERR 322 is set if this calculated value is greater than 255. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

324 FREQ ACC Unable to adjust MAINSENSE close to 0 volts using the coarse adjust DAC. The coarse adjust and fine adjust DAC are used together to set MAINSENSE to 0 volts with the loop opened. ERR 324 is set if the coarse adjust DAC cannot bring MAINSENSE close enough to 0 volts for the fine adjust DACs to bring MAINSENSE to exactly 0 volts. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

325 FREQ ACC Unable to adjust MAINSENSE to 0 volts using the fine adjust DAC. The coarse adjust and fine adjust DAC are used together to set MAINSENSE to 0 volts with the loop opened. ERR 325 is set if the fine adjust DAC cannot bring MAINSENSE to 0 volts. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

326 FREQ ACC Fine adjust DAC near end of range. The fine adjust DAC is set to bring MAINSENSE to 0 volts. ERR 326 is set if the fine adjust DAC value is set to less than 5 or greater than 250. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

327 OFF UNLK Offset roller oscillator PLL is unlocked. May indicate loss of 10 MHz reference. The 10 MHz reference should measure greater than –7 dBm at A15J303. The ADC measures OFFSENSE at the beginning of each sweep and, if the voltage is outside certain limits, the offset oscillator pretune DAC is adjusted to bring OFFSENSE within the proper range. ERR 327 is set if this cannot be accomplished. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

328 FREQ ACC Roller fine adjust DAC sensitivity less than or equal to 0. During the LO adjust routine, the fine adjust DAC is set to two different values and the MAINSENSE voltage is measured at each setting. ERR 328 is set if the difference between these voltages is 0 or negative. This is typically the result of the main roller loop being unlocked. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

329 FREQ ACC Roller coarse adjust DAC sensitivity less than or equal to 0. During the LO adjust routine, the coarse adjust DAC is set to two different values and the MAINSENSE voltage is measured at each setting. ERR 329 is set if the difference between these voltages is 0 or negative. This is typically the result of the main roller loop being unlocked. This error is not applicable to 8560 E-series or EC-series spectrum analyzers. If it occurs in an 8560 E-series or EC-series spectrum analyzer, suspect a problem with the model number identification in the spectrum analyzer firmware.

YTO Loop Error (331)

This error rarely occurs but is usually indicative of a digital hardware failure.

331 FREQ ACC Invalid YTO frequency. Firmware attempted to set the YTO to a frequency outside the range of the YTO (2.95 to 6.8107 GHz). Suspect a digital hardware problem, such as a bad RAM on the A2 controller assembly. Contact the factory.

600 MHz Reference Loop (333)

This error requires troubleshooting the A15 RF board assembly (synthesizer section) or the ADC circuits.

`333 600 UNLK` The 600 MHz reference oscillator PLL is unlocked. If error codes 302, 303, 304, 327 or 499 are also present, suspect the 10 MHz reference, the A21 OCXO, or the TCXO (Option 103), or the A15 RF assembly. ERR 333 is set if LO3ERR is outside of its prescribed limits.

YTO Leveling Loop (334)

This error often requires troubleshooting the A14 frequency control assembly (synthesizer section), the A7 LO distribution amplifier, or the ADC circuits.

`334 LO AMPL` First LO distribution amplifier is unleveled. Error 334 may be displayed if the front-panel LO OUTPUT is not terminated in 50 Ω. This error is usually accompanied by error codes 300 or 301. ERR 301 YTO UNLK is cleared once ERR 334 has been cleared. Check the output of the A11 YTO with the jumper on A14J23 in the TEST position. The YTO power output should be between +9 and +13 dBm. If the YTO is working properly, refer to "LODA Drive" on page 611. The LODA AGC voltage is monitored by the ADC. ERR 334 is set if LODA AGC is outside of its prescribed limits. Refer to "LODA Drive" on page 611.

Sampling Oscillator (335)

This error indicates an unlocked sampling oscillator (also known as the offset Lock Loop).

`335 SMP UNLK` Sampling oscillator PLL is unlocked. ERR 335 is set if OFL_ERR is outside its prescribed limits.

10 MHz Reference (336)

> This message occurs during the internal IF calibration routines. The routine locks the cal oscillator to the internal 10 MHz reference, regardless of the setting of INT/EXT REF.

336 10 MHz Ref Calibration oscillator failed to lock within 5 seconds after going to internal 10 MHz reference. ERR 336 will not be cleared until a successful full cal "LO Re-Align" is executed.

Fractional N PLL (337)

> This error indicates an unlocked fractional N phase locked loop. This error only applies to the hardware in an 8560 E-series or EC-series spectrum analyzer.

337 FN UNLK Fractional N circuitry is unable to lock.

YTO Loop Settling Errors (351 to 354)

> These errors are generated when the YTO loop error voltage will not stabilize at an acceptable value during the YTO loop locking routines. These errors only apply to the hardware in an 8560 E-series or EC-series spectrum analyzer.

351 SETL FLD YTO error voltage is not settling.

352 TWID FLD Unable to bring YTO error voltage DAC's to quiescent point.

353 SRCH FLD No acceptable YTO DAC value found.

354 LK ITERS Cannot lock. Lock iteration routine terminated.

Sampling Oscillator (355)

> This error indicates an unlocked sampling oscillator during the local oscillator (LO) alignment routine. This error only applies to the hardware in an 8560 E-series or EC-series spectrum analyzer.

355 SMP CAL Sampler unlock condition during calibration routine. This error remains until a successful recalibration is performed.

Span Accuracy Calibration Errors (356 to 361)

These errors are generated when the span accuracy calibration fails. The span accuracy calibration is done during "power up", IF calibration (every 5 minutes), and LO IF realignment routines. Span accuracy calibration sweeps occur during the retrace (dead time) of the main sweep ramp. The firmware then detects any span accuracy calibration errors. These errors only apply to firmware revisions 931216 and later.

356 SPAC CAL Sweep data problem finding "bucket 1" of the span accuracy calibration sweep. This error indicates a possible failure of the sweep generator, span attenuator, or main/FM coil sweep switches on the A14 frequency control assembly. Refer to Chapter11 , "Synthesizer Section."

357 SPAC CAL Cannot find the "x" intersection for "bucket 1" of the span accuracy calibration sweep. This error indicates a possible failure of the sweep generator, span attenuator, or main/FM coil sweep switches on the A14 frequency control assembly. Refer to Chapter11 , "Synthesizer Section."

358 SPAC CAL Sweep data problem finding "bucket 2" of the span accuracy calibration sweep. This error indicates a possible failure of the sweep generator, span attenuator, or main/FM coil sweep switches on the A14 frequency control assembly. Refer to Chapter11 , "Synthesizer Section."

359 SPAC CAL Cannot find "x" intersection for "bucket 2" of the span accuracy calibration sweep. This error indicates a possible failure of the sweep generator, span attenuator, or main/FM coil sweep switches on the A14 frequency control assembly. Refer to Chapter11 , "Synthesizer Section."

360 SPAC CAL The start bucket correction is out of range. This error indicates a possible failure of the sweep generator on the A14 frequency control assembly. Refer to "Sweep Generator Circuit" on page 585.

361 SPAC CAL The percent of span correction is out of range. This error indicates a possible failure of the sweep generator on the A14 frequency control assembly. Refer to "Sweep Generator Circuit" on page 585.

Automatic IF Errors (400 to 599)

These error codes are generated when the automatic IF adjustment routine detects a fault. This routine first adjusts amplitude parameters, then resolution bandwidths in this sequence: 300 kHz, 1 MHz, 100 kHz, 30 kHz, 10 kHz, 3 kHz, 1 kHz, 300 Hz, 100 Hz, 30 Hz, 10 Hz, 3 Hz, 1 Hz, and 2 MHz. The routine restarts from the beginning if a fault is detected. Parameters adjusted after the routine begins but before the fault is detected are correct; parameters adjusted later in the sequence are suspect. Refer to "Automatic IF Adjustment" on page 439.

The IF Section relies on the ADC and video circuitry to perform its continuous IF adjustments. IF-related errors occur if the ADC, video circuitry, or A4 assembly linear path is faulty.

400 AMPL <300 Unable to adjust amplitude of resolution bandwidths less than 300 Hz.

401 AMPL 300 Unable to adjust amplitude of 300 Hz resolution bandwidth.

402 AMPL 1K Unable to adjust amplitude of 1 kHz resolution bandwidth.

403 AMPL 3K Unable to adjust amplitude of 3 kHz resolution bandwidth.

404 AMPL 10K Unable to adjust amplitude of 10 kHz resolution bandwidth.

Errors 405 to 416: When these 10K resolution bandwidth (RBW) error messages appear, use the following steps to check for errors 581 or 582.

1. Press **LINE** to turn spectrum analyzer off.

2. Press **LINE** to turn spectrum analyzer on and observe the lower right-hand corner of the display for 10 seconds.

3. If ERR 581 or ERR 582 appears, the fault is most likely caused by the cal oscillator. Refer to errors 581 and 582.

4. If ERR 581 or ERR 582 does not appear, troubleshoot the A5 IF assembly.

Multiple IF errors during IF adjust: If a FULL IF ADJ sequence (pressing **CAL** and **FULL IF ADJ**) results in IF errors while displaying `IF ADJUST STATUS: AMPLITUDE`, the cal oscillator on the A4 assembly might not be providing the correct output signal. Perform the following steps:

1. Disconnect W30 (white) from A5J4.

2. Connect W30 to the input of a second spectrum analyzer and set its controls as follows:

   Center frequency.......................... 10.7 MHz
   Reference level .... −30 dBm

3. Observe the spectrum analyzer display while pressing **FULL IF ADJ** on the spectrum analyzer. If a −35 dBm signal does not appear, troubleshoot the cal oscillator on the A4 assembly.

4. If a −35 dBm signal does appear, troubleshoot the A5 IF assembly.

`405 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in first crystal pole.

`406 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in second crystal pole.

`407 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in third crystal pole.

`408 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in fourth crystal pole.

`409 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in first crystal pole.

`410 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in second crystal pole.

`411 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in third crystal pole.

`412 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in fourth crystal pole.

`413 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in first crystal pole.

`414 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in second crystal pole.

`415 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in third crystal pole.

`416 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in fourth crystal pole.

`417 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in first crystal pole.

`418 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in second crystal pole.

`419 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in third crystal pole.

`420 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in fourth crystal pole.

`421 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in first crystal pole.

`422 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in second crystal pole.

`423 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in third crystal pole.

`424 RBW 10K` Unable to adjust 10 kHz resolution bandwidth in fourth crystal pole.

`425 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in first crystal pole.

`426 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in second crystal pole.

`427 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in third crystal pole.

`428 RBW 3K` Unable to adjust 3 kHz resolution bandwidth in fourth crystal pole.

`429 RBW <300` Unable to adjust resolution bandwidths less than 300 Hz. ADC handshake.

`430 RBW 300` Unable to adjust 300 Hz resolution bandwidth. ADC handshake.

`431 RBW 1K` Unable to adjust 1 kHz resolution bandwidth. ADC handshake.

`432 RBW 3K` Unable to adjust 3 kHz resolution bandwidth. ADC handshake.

`433 RBW 10K` Unable to adjust 10 kHz resolution bandwidth. ADC handshake.

`434 RBW 300`	300 Hz resolution bandwidth amplitude low in first crystal pole.
`435 RBW 300`	300 Hz resolution bandwidth amplitude low in second crystal pole.
`436 RBW 300`	300 Hz resolution bandwidth amplitude low in third crystal pole.
`437 RBW 300`	300 Hz resolution bandwidth amplitude low in fourth crystal pole.
`438 RBW 1K`	1 kHz resolution bandwidth amplitude low in first crystal pole.
`439 RBW 1K`	1 kHz resolution bandwidth amplitude low in second crystal pole.
`440 RBW 1K`	1 kHz resolution bandwidth amplitude low in third crystal pole.
`441 RBW 1K`	1 kHz resolution bandwidth amplitude low in fourth crystal pole.
`442 RBW 3K`	3 kHz resolution bandwidth amplitude low in first crystal pole.
`443 RBW 3K`	3 kHz resolution bandwidth amplitude low in second crystal pole.
`444 RBW 3K`	3 kHz resolution bandwidth amplitude low in third crystal pole.
`445 RBW 3K`	3 kHz resolution bandwidth amplitude low in fourth crystal pole.
`446 RBW 10K`	10 kHz resolution bandwidth amplitude low in first crystal pole.
`447 RBW 10K`	10 kHz resolution bandwidth amplitude low in second crystal pole.
`448 RBW 10K`	10 kHz resolution bandwidth amplitude low in third crystal pole.
`449 RBW 10K`	10 kHz resolution bandwidth amplitude low in fourth crystal pole.
`450 IF SYSTM`	IF hardware failure. Check other error messages.
`451 IF SYSTM`	IF hardware failure. Check other error messages.
`452 IF SYSTM`	IF hardware failure. Check other error messages.
`454 AMPL`	Unable to adjust step gain amplifiers. Check other errors.

455 AMPL   Unable to adjust fine attenuator of the step gain amplifiers.

456 AMPL   Unable to adjust fine attenuator of the step gain amplifiers.

457 AMPL   Unable to adjust fine attenuator of the step gain amplifiers.

458 AMPL   Unable to adjust first step gain stage.

459 AMPL   Unable to adjust first step gain stage.

460 AMPL   Unable to adjust first step gain stage.

461 AMPL   Unable to adjust second step gain stage.

462 AMPL   Unable to adjust second step gain stage.

463 AMPL   Unable to adjust third step gain stage.

464 AMPL   Unable to adjust third step gain stage.

465 AMPL   Unable to adjust third step gain stage.

466 LIN AMPL Unable to adjust linear amplifier scale.

467 LOG AMPL Unable to adjust step gain amplifiers.

468 LOG AMPL Unable to adjust third step gain stage.

469 LOG AMPL Unable to adjust step gain amplifiers.

470 LOG AMPL Unable to adjust third step gain stage.

471 RBW 30K Unable to adjust 30 kHz resolution bandwidth in first LC pole.

472 RBW 100K Unable to adjust 100 kHz resolution bandwidth in first LC pole.

473 RBW 300K Unable to adjust 300 kHz resolution bandwidth in first LC pole.

474 RBW 1M Unable to adjust 1 MHz resolution bandwidth in first LC pole.

475 RBW 30K Unable to adjust 30 kHz resolution bandwidth in second LC pole.

476 RBW 100K Unable to adjust 100 kHz resolution bandwidth in second LC pole.

477 RBW 300K Unable to adjust 300 kHz resolution bandwidth in second LC pole.

478 RBW 1M Unable to adjust 1 MHz resolution bandwidth in second LC pole.

483 RBW 10K Unable to adjust 10 kHz resolution bandwidth.

`484 RBW 3K`   Unable to adjust 3 kHz resolution bandwidth.

`485 RBW 1K`   Unable to adjust 1 kHz resolution bandwidth.

`486 RBW 300` Unable to adjust 300 Hz resolution bandwidth.

`487 RBW 100` Unable to adjust 100 Hz resolution bandwidth.

`488 RBW 100` Unable to adjust 100 Hz resolution bandwidth.

`489 RBW 100` Unable to adjust 100 Hz resolution bandwidth.

`490 RBW 100` Unable to adjust 100 Hz resolution bandwidth.

`491 RBW <300` Unable to adjust the resolution bandwidths less than 300 Hz. Crystal sweep gain problem.

`492 RBW 300` Unable to adjust 300 Hz resolution bandwidth. Crystal sweep gain problem.

`493 RBW 1K`   Unable to adjust 1 kHz resolution bandwidth. Crystal sweep gain problem.

`494 RBW 3K`   Unable to adjust 3 kHz resolution bandwidth. Crystal sweep gain problem.

`495 RBW 10K` Unable to adjust 10 kHz resolution bandwidth. Crystal sweep gain problem.

`496 RBW 100` Unable to adjust 100 Hz resolution bandwidth. Inadequate Q.

`497 RBW 100` Unable to adjust 100 Hz resolution bandwidth. Alignment problem.

`498 RBW 100` Unable to adjust 100 Hz resolution bandwidth. Gain problem.

`499 CAL UNLK` Cal oscillator is unlocked. Verify the unlocked conditions as follows:

     1. Place A4 in its service position and disconnect W51 (gray-yellow) from A4J7.

     2. Connect W51 to the input of another spectrum analyzer. This is the 10 MHz reference for the cal oscillator.

     3. If a 10 MHz signal (approximately 0 dBm) is not present, suspect the A15 RF assembly, the A21 OCXO, or the A15 assembly TCXO (Option 103). If the 10 MHz reference is present, continue with step 4.

     4. Reconnect W17 to A4J7 and monitor the tune voltage at A4J9 pin 3 with an oscilloscope.

     5. Press **PRESET** on the spectrum analyzer under test.

6. If the voltage is either +15 Vdc or −15 Vdc, the Cal Oscillator is probably at fault. Normally, the voltage should be near +15 V during a sweep, and between −9 V and +9 V during retrace.

An **intermittent** error 499 indicates the cal osc phase-locked-loop probably can lock at 10.7 MHz, but cannot lock at the 9.9 and 11.5 MHz extremes. This may prevent the cal oscillator from adjusting the 1 MHz or 30 kHz through 300 kHz bandwidths. This symptom implies a failure in the oscillator, function block X. (See the A4 log amp/cal oscillator schematic sheet 4 of 4.) The oscillator is unable to tune the required frequency range with the −9 V to +9 V control voltage. Troubleshoot A4CR802 (most probable cause), L801, C808, C809, and U807.

`500 AMPL 30K` Unable to adjust amplitude of 30 kHz resolution bandwidth.

`501 AMPL .1M` Unable to adjust amplitude of 100 kHz resolution bandwidth.

`502 AMPL .3M` Unable to adjust amplitude of 300 kHz resolution bandwidth.

`503 AMPL 1M` Unable to adjust amplitude of 1 MHz resolution bandwidth.

`504 AMPL 30K` Unable to adjust amplitude of 30 kHz resolution bandwidth.

`505 AMPL .1M` Unable to adjust amplitude of 100 kHz resolution bandwidth.

`506 AMPL .3M` Unable to adjust amplitude of 300 kHz resolution bandwidth.

`507 AMPL 1M` Unable to adjust amplitude of 1 MHz resolution bandwidth.

`508 AMPL 30K` Unable to adjust amplitude of 30 kHz resolution bandwidth. Insufficient gain during LC bandwidth calibration.

`509 AMPL .1M` Unable to adjust amplitude of 100 kHz resolution bandwidth. Insufficient gain during LC bandwidth calibration.

`510 AMPL .3M` Unable to adjust amplitude of 300 kHz resolution bandwidth. Insufficient gain during LC bandwidth calibration.

`511 AMPL 1M` Unable to adjust amplitude of 1 MHz resolution bandwidth. Insufficient gain during LC bandwidth calibration.

`512 RBW <300` Unable to adjust resolution bandwidths less than 300 Hz. Insufficient gain during crystal bandwidth calibration.

`513 RBW 300` Unable to adjust 300 Hz resolution bandwidth. Insufficient gain during crystal bandwidth calibration.

`514 RBW 1K` Unable to adjust 1 kHz resolution bandwidth. Insufficient gain during crystal bandwidth calibration.

`515 RBW 3K` Unable to adjust 3 kHz resolution bandwidth. Insufficient gain during crystal bandwidth calibration.

`516 RBW 10K` Unable to adjust 10 kHz resolution bandwidth. Insufficient gain during crystal bandwidth calibration.

`517 RBW 100` Unable to adjust 100 Hz resolution bandwidth. Crystal sweep problem.

`518 RBW 300` Unable to adjust 300 Hz resolution bandwidth. Crystal sweep problem.

`519 RBW 1K` Unable to adjust 1 kHz resolution bandwidth. Crystal sweep problem.

`520 RBW 3K` Unable to adjust 3 kHz resolution bandwidth. Crystal sweep problem.

`521 RBW 10K` Unable to adjust 10 kHz resolution bandwidth. Crystal sweep problem.

`522 RBW 10K` Unable to adjust symmetry of 10 kHz resolution bandwidth in first crystal pole.

`523 RBW 10K` Unable to adjust symmetry of 10 kHz resolution bandwidth in second crystal pole.

`524 RBW 10K` Unable to adjust symmetry of 10 kHz resolution bandwidth in third crystal pole.

`525 RBW 10K` Unable to adjust symmetry of 10 kHz resolution bandwidth in fourth crystal pole.

`526 RBW <300` ADC timeout during IF ADJUST of <300 Hz resolution bandwidth.

`527 RBW <300` Step gain correction failed for <300 Hz resolution bandwidth. Check narrow bandwidth SGO attenuator.

`528 RBW <300` Calibration of dc level at ADC failed for <300 Hz resolution bandwidth.

529 `RBW <300` Invalid demodulated data for <300 Hz resolution bandwidth flatness and IF down-converter. Demod data for calibration may be bad.

530 `RBW <300` Adjustment of VCXO down-converter failed with resolution bandwidths less than 300 Hz. Narrow bandwidth VCXO calibration failed.

531 `RBW <300` Flatness correction data for resolution bandwidths <300 Hz not acceptable.

532 `RBW <300` Absolute gain data for resolution bandwidths <300 Hz not acceptable.

533 `RBW <300` ADC timeout adjusting resolution bandwidths less than 300 Hz. Timeout during data sampling narrow bandwidth chunk.

534 `RBW <300` Unable to do frequency count of CAL OSC using IF down-converter when adjusting resolution bandwidths less than 300 Hz.

535 `RBW <300` Unable to obtain adequate FM demod range to measure 500 Hz IF filter with resolution bandwidths less than 300 Hz.

536 `RBW <300` Unable to auto-range chirp signal while setting VCXO or doing flatness calibration with resolution bandwidths less than 300 Hz.

537 `RBW <300` Unable to auto-range CW CAL OSC signal to count VCXO signal with resolution bandwidths less than 300 Hz.

538 `RBW <300` Shape of 500 Hz IF filter appears too noisy to adjust VCXO down-converter for resolution bandwidths less than 300 Hz.

539 `RBW <300` Unable to auto-range the CW CAL OSC signal to pretune the VCXO for resolution bandwidths less than 300 Hz.

540 `RBW <300` Unable to find CW CAL OSC signal during VCXO pretune at power-up with resolution bandwidths less than 300 Hz.

550 `ID CALOSC` CAL Oscillator ID. Indicates incompatible hardware. Cal Osc not expected

551 `ID LOGBD` LOG Board ID. Indicates incompatible hardware. Log board not expected.

552 `LOG AMPL` Unable to adjust amplitude of log scale.

553 `LOG AMPL` Unable to adjust amplitude of log scale.

`554 LOG AMPL` Unable to adjust amplitude of log scale.

`555 LOG AMPL` Unable to adjust amplitude of log scale.

`556 LOG AMPL` Unable to adjust amplitude of log scale.

`557 LOG AMPL` Unable to adjust amplitude of log scale.

`558 LOG AMPL` Unable to adjust amplitude of log scale.

`559 LOG AMPL` Unable to adjust amplitude of log scale.

`560 LOG AMPL` Unable to adjust amplitude of log scale.

`561 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in second step gain.

`562 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in second step gain.

`563 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in third step gain range.

`564 LOG AMPL` Unable to adjust amplitude of log scale.

`565 LOG AMPL` Unable to adjust amplitude of log scale.

`566 LOG AMPL` Unable to adjust amplitude of log scale.

`567 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in Log offset/Log Expand stage.

`568 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in Log offset/Log Expand stage.

`569 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in Log offset/Log Expand stage.

`570 LOG AMPL` Unable to adjust amplitude of log scale. Possible problem in Log offset/Log Expand stage.

`571 AMPL` Unable to adjust step gain amplifiers.

`572 AMPL 1M` Unable to adjust amplitude of 1 MHz resolution bandwidth.

`573 LOG AMPL` Unable to adjust amplitude of log scale. Check video offset circuitry.

`574 LOG AMPL` Unable to adjust amplitude of log scale. Check video offset circuitry.

`575 LOG AMPL` Unable to adjust amplitude of log scale. Check video offset circuitry.

`576 LOG AMPL` Unable to adjust amplitude of log scale. Check video offset circuitry.

`577 LOG AMPL` Unable to adjust amplitude of log scale. Check video offset circuitry.

`578 LOG AMPL` Limiter calibration error from DC logger calibration.

`579 LOG AMPL` Attenuator CAL level error from DC logger calibration.

`580 LOG AMPL` Calibration level error from DC logger fidelity calibration.

`581 AMPL` Unable to adjust 100 kHz resolution bandwidth and resolution bandwidths less than or equal to 10 kHz. ADC/CALOSC handshake calibration problem in crystal sweep. Refer to Error 582.

`582 AMPL` Unable to adjust 100 kHz resolution bandwidth and resolution bandwidths less than or equal to 10 kHz. Bad CALOSC Calibration in Sweep Rate. Test the 100 kHz resolution bandwidth filter 3 dB bandwidth as follows:

1. Connect the CAL OUTPUT signal (A4J8) to the INPUT 50Ω .

2. Press **PRESET** and set the controls as follows:

Center frequency .... 300 MHz
Span .... 500 kHz
Resolution bandwidth .... 100 kHz
Log dB/div ....1 dB
Reference level adjust to place signal peak at top of the screen

3. Press **PEAK SEARCH** and **MARKER DELTA** and turn the knob clockwise to position the marker until the delta MKR reads –3 dB ±0.1 dB.

4. Press **MARKER DELTA** and move the marker to the other side of the peak until the delta MKR reads 0 dB ±0.1 dB.

5. If the delta MKR frequency is between 90 kHz and 110 kHz, the 100 kHz resolution bandwidth is working properly. If the frequency is outside these limits, read the following information on the A4 Cal Oscillator sweep generator.

If the 100 kHz resolution bandwidth works properly, the cal oscillator sweep generator is failing to sweep its oscillator frequency at the correct rate. The error is detected in sweeping on the skirts of the 100 kHz resolution bandwidth.

A properly operating sweep generator generates a series of negative-going parabolas. These parabolas generate the sweeps used to adjust resolution bandwidths of 10 kHz and below. Check the sweep generator with the following steps. Refer also to "300 Hz to 3 kHz Resolution Bandwidth Out of Specification" on page 478.

1. Remove the shields.

2. Connect an oscilloscope probe to A4U804C pin 8.

3. On the spectrum analyzer, press **CAL**, **FULL IF ADJ**.

4. Approximately 8 seconds after starting the **FULL IF ADJ**, check for negative-going parabolas (similar to half-sine waves) 5 ms wide and approximately –4 V at their peak. Refer to Chapter 9 , "IF Section," for more information on the A4 Log Amp/Cal Oscillator Assembly.

583 `RBW 30K` Unable to adjust 30 kHz resolution bandwidth.

584 `RBW 100K` Unable to adjust 100 kHz resolution bandwidth.

585 `RBW 300K` Unable to adjust 300 kHz resolution bandwidth.

586 `RBW 1M` Unable to adjust 1 MHz resolution bandwidth.

587 `RBW 30K` Unable to adjust 30 kHz resolution bandwidth.

588 `RBW 100K` Unable to adjust 100 kHz resolution bandwidth.

589 `RBW 300K` Unable to adjust 300 kHz resolution bandwidth.

590 `RBW 1M` Unable to adjust 1 MHz resolution bandwidth.

591 `LOG AMPL` Unable to adjust amplitude of log scale.

592 `LOG AMPL` Unable to adjust amplitude of log scale.

593 `LOG TUNE` Limiter calibration tune error from DC logger calibration.

594 `LOG OFST` Attenuator calibration offset error from DC logger calibration.

595 `LOG ATTN` Attenuator calibration absolute error from DC logger calibration.

596 `LOG FID` Fidelity error from DC logger calibration.

597 `LOG OFST` Fidelity offset error from DC logger calibration.

598 `LOG OFST` Fidelity offset unstable from DC logger calibration.

599 `LOG GAIN` Fidelity gain error from DC logger calibration.

System Errors (600 to 651)

ADC timeout errors occur if the A2 controller assembly frequency counter is faulty. Refer to Chapter8 , "ADC/Interface Section."

600 SYSTEM   Hardware/firmware interaction; check other errors.

601 SYSTEM   Hardware/firmware interaction; check other errors.

650 OUTOF RG   ADC input is outside of the ADC range.

651 NO IRQ   Microprocessor is not receiving interrupt from ADC.

Digital and Checksum Errors (700 to 799)

EEROM Checksum Errors (700 to 704)

Faults on the A2 controller assembly can cause these errors. Refer to Chapter10 , "Controller Section." Although some of these errors might result in a blanked display, it is possible to read these errors over GPIB. Refer to "Troubleshooting to a Functional Section" on page 309.

The EEROM on A2 is used to store data for frequency response correction, elapsed time, focus, and intensity levels. Error codes from 700 to 703 indicate that some part of the data in EEROM is invalid. An EEROM error could result from either a defective EEROM or an improper sequence of storing data in EEROM. Check the EEROM with the following steps:

1. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR ENA position.

2. On the spectrum analyzer, press **CAL MORE 1 OF 2**, **SERVICE CAL DATA**, **FLATNESS**, and **FLATNESS DATA**. Enter a value of 130. Press **PREV MENU**, **STORE DATA**, **YES**, and **DISPLAY**.

3. Press **INTEN**, enter an intensity value of 90, and press **STORE INTEN**.

4. Press **MORE 1 OF 2 FOCUS**, enter a focus value of 128, and press **STORE FOCUS**. Turn the **LINE** switch off, then on, cycling the power.

5. If errors are still present, the EEROM A2U501 is defective. Refer to the EEROM replacement procedure in Chapter5 , "Replaceable Parts."

`700 EEROM`   Checksum error of EEROM A2U501.

`701 AMPL CAL` Checksum error of frequency response correction data.

`702 ELAP TIM` Checksum error of elapsed time data.

`703 AMPL CAL` Checksum error of frequency response correction data. Default values being used.

`704 PRESELCT` Checksum error of customer preselector peak data. External preselector data recalled in internal mode, or internal preselector data recalled in external mode. To clear the error, press **RECALL**, **MORE 1 OF 2**, **FACTORY PRSEL PK**, **SAVE**, and **SAVE PRSEL PK**.

Program ROM Checksum Errors (705 to 710)

The instrument power-on diagnostics perform a checksum on each programmed ROM (A2 controller assembly). If an invalid checksum is found for a particular ROM, an error code is generated. If a defective programmed ROM is found, replace it with another ROM with the same part number. Refer to Chapter5 , "Replaceable Parts."

Although some of these errors might result in a blanked display, it is possible to read these errors over GPIB. Refer to "Troubleshooting to a Functional Section" on page 309.

`705 ROM U306` Checksum error of program ROM A2U306.

`706 ROM U307` Checksum error of program ROM A2U307.

`707 ROM U308` Checksum error of program ROM A2U308.

`708 ROM U309` Checksum error of program ROM A2U309.

`709 ROM U310` Checksum error of program ROM A2U310.

`710 ROM U311` Checksum error of program ROM A2U311.

RAM Check Errors (711 to 716)

The instrument power-on diagnostics check the program RAM. This includes the two RAMs used for STATE storage. If any STATE information is found to be invalid, all data in that RAM is destroyed. A separate error code is generated for each defective program RAM. All RAM is battery-backed. See "State- and Trace-Storage Problems" on page 522.

`711 RAM U303` Checksum error of system RAM A2U303.

`712 RAM U302` Checksum error of system RAM A2U302.

`713 RAM U301` Checksum error of system RAM A2U301.

`714 RAM U300` Checksum error of system RAM A2U300.

`715 RAM U305` Checksum error of system RAM A2U305.

`716 RAM U304` Checksum error of system RAM A2U304.

Microprocessor Error (717)

`717 BAD uP` Microprocessor not fully operational. Refer to Chapter10 , "Controller Section."

Battery Problem (718)

If STATE or TRACE data is found to be corrupt, the processor tests the display RAMs and the program RAMs containing the STATE information. If the RAMs are working properly, this error message is generated. To check the BT1 Battery and the battery backup circuitry, refer to "State- and Trace-Storage Problems" on page 522.

`718 BATTERY?` Nonvolatile RAM not working; check battery BT1. This error can also be generated if the battery has been disconnected then reconnected. If this is the cause, cycling power clears the error.

Model Number Error (719)

If this error occurs, return the instrument to a service center for repair.

`719 MODEL #?` Could not read ID string from EEROM A2U501.

System Errors (750 to 759)

These errors often require troubleshooting the A2 controller and A3 interface assemblies.

`750 SYSTEM` Hardware/firmware interaction, zero divide. Check for other errors.

`751 SYSTEM` Hardware/firmware interaction, floating point overflow. Check for other errors.

`752 SYSTEM` Hardware/firmware interaction, floating point underflow. Check for other errors.

`753 SYSTEM` Hardware/firmware interaction, log error. Check for other errors.

`754 SYSTEM` Hardware/firmware interaction, integer overflow. Check for other errors.

`755 SYSTEM` Hardware/firmware interaction, square root error. Check for other errors.

`756 SYSTEM` Hardware/firmware interaction, triple overflow. Check for other errors.

`757 SYSTEM` Hardware/firmware interaction, BCD overflow. Check for other errors.

`758 SYSTEM` Unknown system error.

`759 SYSTEM` Hardware/firmware interaction. Code invoked for wrong instrument.

Fast ADC Error (760)

This error applies to EC-series instruments, and E-series instruments with fast ADC (Option 007).

`760 NO FADC` The FADC board did not respond properly to initialization commands.

Option Module Errors (800 to 899)

These error codes are reserved for option modules, such as the 85629 test and adjustment module and the 85620A mass memory module. Refer to the option module manual for a listing of error messages.

User-Generated Errors (900 to 999)

These error codes indicate user-generated errors.

900 `TG UNLVL` Tracking generator output is unleveled.

901 `TGFrqLmt` Tracking generator output unleveled because START FREQ is set below tracking generator frequency limit (300 kHz).

902 `BAD NORM` The state of the stored trace does not match the current state of the spectrum analyzer.

903 `A > DLMT` Unnormalized trace A is off-screen with trace math or normalization on.

904 `B > DLMT` Calibration trace (trace B) is off-screen with trace math or normalization on.

905 `EXT REF` Unable to lock cal oscillator when set to external frequency reference. Check that the external 10 MHz reference is within tolerance.

906 `OVENCOLD` The oven-controlled crystal oscillator (OCXO) oven is cold.

907 `DO IF CAL` Unit is still performing IF calibrations, or is in need of IF calibrations which were not yet done due to an OVENCOLD condition, since an OVENCOLD error is indicative of a bandwidth ≤ 1 kHz not getting calibrated.

908 `BW>>SPCG` Channel bandwidth is too wide, compared to the channel spacing, for a meaningful adjacent channel power computation.

909 `SPANACP` The frequency span is too small to obtain a valid adjacent channel power (ACP) measurement.

910 `SPAN>ACP` The frequency span is too wide, compared to the channel bandwidth, to obtain a valid adjacent channel power (ACP) measurement.

Block Diagram Description

The spectrum analyzer is comprised of the six main sections listed below. See Figure 7-6 on page 353. The following descriptions apply to the simplified block diagram and overall block diagram located at the end of this chapter. Assembly level block diagrams are located in Chapters 8 through 13.

Figure 7-6   **Functional Sections**
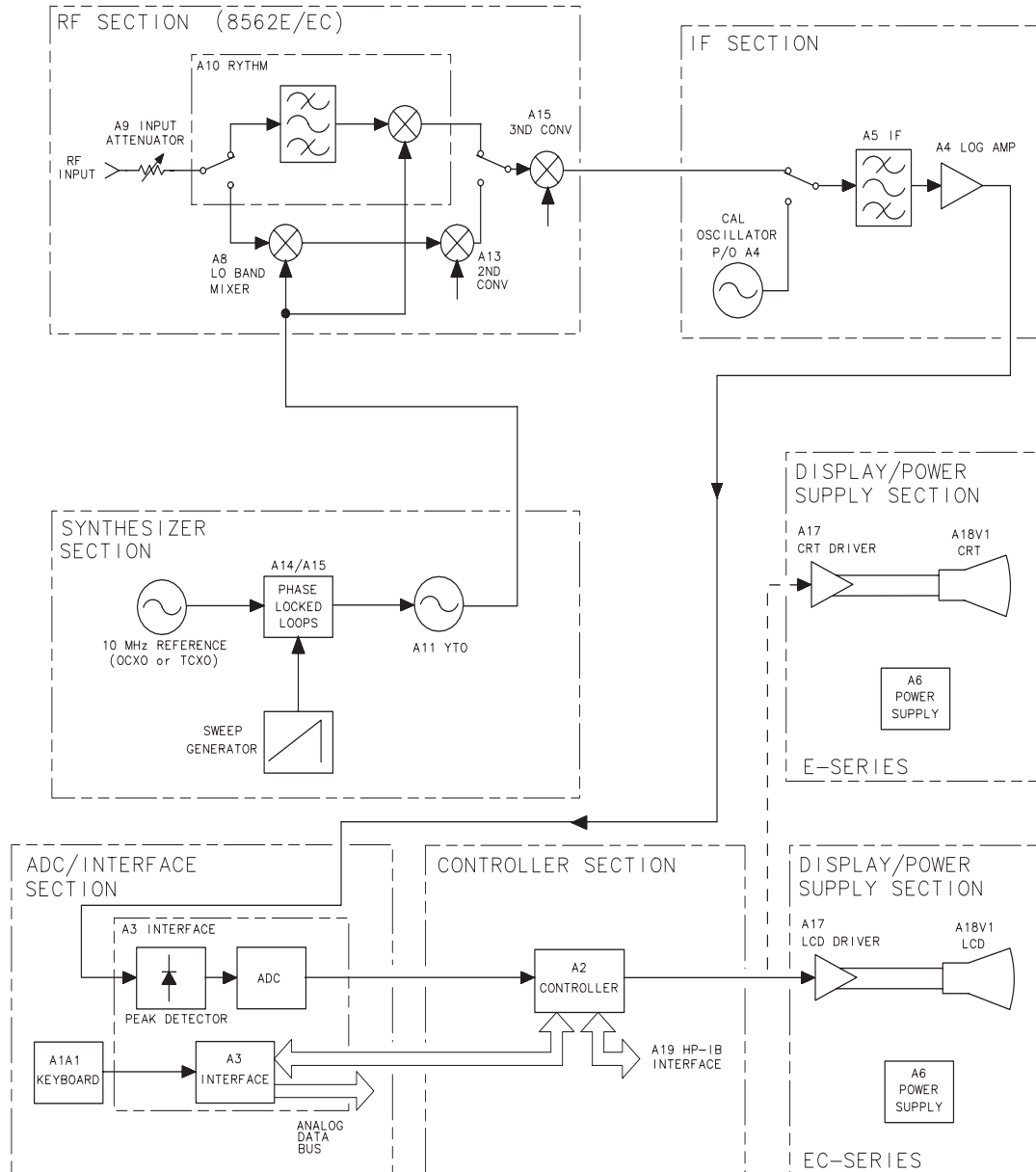
sl116c

RF Section

The RF section includes the following assemblies:

A7 SLODA (switched LO distribution amplifier)
A8 low band mixer
A9 input attenuator
A10 YIG-tuned filter/mixer (RYTHM)
A11 YTO (YIG-tuned oscillator)
A13 second converter
A14 frequency control assembly (also in synthesizer section)
A15 RF assembly (also in synthesizer section)
FL1, FL2 low-pass filters

The RF section converts all input signals to a fixed IF of 10.7 MHz. The RF section microcircuits are controlled by signals from the A14 frequency control and A15 RF assemblies.

Band 0 ....9 kHz to 2.9 GHz
Bands 1 through 2 ....2.75 to 13.2 GHz

Band 0 uses triple conversion to produce the 10.7 MHz IF and a fourth conversion used only in the digital resolution bandwidths (≤100 Hz). A8 low band mixer up-converts the RF input to a first IF of 3.9107 GHz. A13 second converter down-converts the 3.9107 GHz IF to an IF of 310.7 MHz. A third conversion on the A15 RF assembly down-converts the second IF to the 10.7 MHz third IF. A fourth conversion on the A4 log amplifier assembly down-converts the third IF to the 4.8 kHz fourth IF used only in the digital resolution bandwidths (≤100 Hz).

Bands 1 and 2 use double conversion. A third conversion is used for the digital resolution bandwidths (≤100 Hz). A10 YIG-tuned filter/mixer (RYTHM) down-converts the RF input to a first IF of 310.7 MHz. Although this IF passes through the A13 second converter, it bypasses the second mixer. The second conversion on the A15 RF assembly down-converts the 310.7 MHz IF to 10.7 MHz. A third conversion on the A4 log amplifier assembly down-converts the second IF to the 4.8 kHz third IF used only in the digital resolution bandwidths (≤100 Hz).

A7 SLODA

The A7 SLODA (switched LO distribution amplifier) levels the output of the A11 YTO and distributes the power to the front-panel First LO OUTPUT, A8 low band mixer, A10 YIG-tuned filter/mixer, and A15U100 sampler. The leveling circuitry is on the A14 frequency control assembly.

A8 Low Band Mixer

A8 low band mixer is ac-coupled and contains a limiter. The high band mixing is done in the A10 YIG-tuned filter/mixer. A PIN diode switch in A10 directs the RF input to the appropriate mixer. A PIN diode switch in A7 SLODA directs the first LO to the appropriate mixer. Low band mixer power is provided by the A14 frequency control assembly.

A9 Input Attenuator

The attenuator is a 50Ω precision, coaxial step attenuator. Attenuation in 10 dB steps from 0 dB to 70 dB is accomplished by switching the signal path through one or more of the three resistive pads. The attenuator automatically sets to 70 dB when the spectrum analyzer turns off, providing ESD protection. (Note that the input attenuator is not field-repairable.) A fourth attenuator section switches a blocking capacitor in and out.

A10 YIG-Tuned Filter/Mixer

The YIG-tuned filter/mixer (RYTHM) is a combination of an RF switch, a high band mixer, and a tracking preselector. The PIN diode switch directs the RF input to the appropriate mixer in the A10 RYTHM assembly or A8 low band mixer.

The tracking preselector is a YIG-tuned filter. It functions as a tunable bandpass filter for high band signals. Coarse frequency control originates from slope and offset DACs located on the A14 frequency control assembly. (Slope and offset DAC values are loaded into EEROM.)

Fine frequency control originates from a preselector peak DAC located on the A3 interface assembly. Values for the preselector peak DAC are interpolated approximately every 17 MHz based upon data taken during the frequency response (flatness) adjustment. The preselector bandwidth varies from greater than 30 MHz, at 2.75 GHz, to greater than 40 MHz, at 13.2 GHz.

The high band mixer is ac coupled. It uses the first and second harmonics of the first local oscillator to cover the frequency range. A PIN diode switch in A7 SLODA directs the first LO to the appropriate mixer. The A14 frequency control assembly provides PIN diode bias.

A11 YTO

A11 is a YTO (YIG-tuned oscillator). YIG (yttrium-iron-garnet) is a ferro-magnetic material which is polished into a small sphere and precisely oriented in a magnetic field. Changes in this magnetic field alter the frequency generated by the YTO. Current control of the magnetic field surrounding the YIG sphere tunes the oscillator to the desired frequency.

A13 Second Converter

The A13 second converter down-converts the 3.9107 GHz first IF to a 310.7 MHz 2nd IF. In high band, it passes the 310.7 MHz first IF from the A10 YIG-tuned filter/mixer to the A15 RF assembly. The converter generates a 3.6 GHz second LO by multiplying a 600 MHz reference. Bandpass filters remove unwanted harmonics of the 600 MHz driving signal. First IF and 2nd LO signals are filtered by cavity filters.

Second IF Amplifier (part of A15)

The second IF amplifier (SIFA) amplifies and filters the second IF. Access to this pre-filtered signal is available at the rear-panel 2ND IF OUTPUT (Option 001 only).

The external mixing input from the front-panel IF INPUT connector is also directed through the SIFA. A dc bias is placed onto the IF INPUT line for biasing external mixers.

Third Converter (part of A15)

The third converter down-converts the 310.7 MHz IF to 10.7 MHz. A PIN-diode switch selects the LO signal used. For normal operation, a 300 MHz LO signal is used. The signal is derived from the 600 MHz reference PLL. During signal identification (SIG ID ON), the 298 MHz SIG ID oscillator is fed to the double balanced mixer on alternate sweeps. Signal identification is available as Option 008.

Flatness Compensation Amplifiers (part of A15)

The flatness compensation amplifiers amplify the output of the double-balanced mixer. The amplifier variable gain (0 to 45 dB) compensates for flatness variations within a band. Band conversion loss is compensated by step gain amplifiers in the IF section.

Control for the amplifiers originates from two DACs on the A3 Interface assembly. (DAC values are interpolated approximately every 17 MHz based on data obtained during the frequency response adjustment.) The A15 flatness-compensation control circuitry converts the RF GAIN voltage, from A3, into two currents: RF GAIN1 and RF GAIN2. These currents drive PIN diodes in the flatness compensation amplifiers.

Synthesizer Section

The first LO uses four PLLs to phase-lock to the internal 10 MHz standard in the instrument. See Figure 7-7 on page 359.

The reference PLL supplies reference frequencies for the instrument. The three remaining PLLs tune and phase-lock the LO through its frequency range. To tune the LO to a particular frequency, the instrument microprocessor must set the programmable feedback dividers (N) and reference dividers (R) contained in each PLL.

Sweeping the First LO

The spectrum analyzer uses a method called lock and roll to sweep the first LO (A11 YTO) for LO spans >2 MHz. This involves phase-locking the spectrum analyzer at the start frequency during the retrace of the sweep, then sweeping through the desired frequency range in an unlocked condition. The sweep ramp, which sweeps the LO during the roll part of the lock and roll process, is generated on the A14 frequency control assembly. It is applied to either the A11 YTO main coil or the A11 YTO FM coil. For LO spans≤2.0 MHz, the YTO PLL remains locked and the fractional N PLL sweeps while remaining phase locked. The frequency/span relationships are as follows:

Table 7-2   **Location of Assembly Troubleshooting Text**

A11 YTO Span Width	Sweep Applied to
20.1 MHz to 3.8107 GHz	A11 YTO main coil
2.01 MHz to 20.0 MHz	A11 YTO FM coil
100 Hz to 2 MHz	Fractional N phase locked loop

When the sweep ramp is applied to the YTO, the spectrum analyzer must prevent this loop from trying to compensate for changes in the output frequency. To accomplish this, the spectrum analyzer opens the PLL by disconnecting the phase detector output of the YTO PLL.

Reference PLL (part of A15)

The 600 MHz reference PLL provides 600 MHz for the second LO, 300 MHz for the third LO, and the sampling oscillator reference, and 10 MHz to the fractional N PLL. The reference PLL is locked to a 10 MHz OCXO (oven-compensated crystal oscillator) or a TCXO (Option 103). The PLL can also be locked to an external frequency reference.

The 10 MHz reference also supplies the reference for the frequency counter on the A2 controller assembly, and the cal oscillator on the A4 assembly.

YTO PLL (A7, A11, part of A14, part of A15)

The YTO PLL produces the instrument first LO (3.0 to 6.81 GHz). The YTO output is mixed with a harmonic of the sampling oscillator in the sampler (A15A2), and the resulting frequency is phase-locked to the output of the fractional N PLL.

The A15U100 sampler mixes the LO signal from the A7 SLODA with a harmonic of the sampling oscillator. The mixing product, the sampler IF, is between 60 and 96 MHz (same frequency range as the fractional N PLL).

Offset Lock Loop (part of A15)

The 285 MHz to 297.2 MHz sampling oscillator is used to sample the YTO. The frequency can be changed by changing the programmable dividers of the offset lock loop.

Figure 7-7 **Phase Lock Loops**
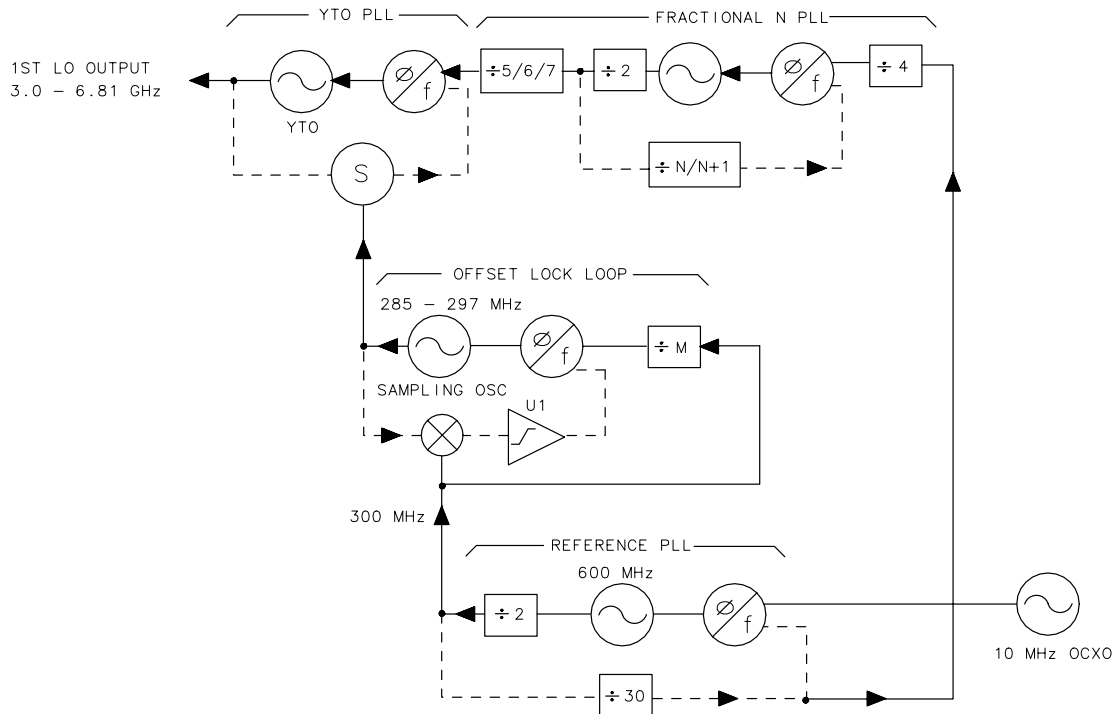
sp113e

Fractional N PLL (part of A14)

The fractional N PLL produces an output of 60 MHz to 96 MHz. This PLL output serves as the reference frequency for the YTO PLL. A one-to-one relationship in frequency tracking exists between the fractional N PLL and the YTO. A change of 1 MHz in the fractional N PLL will produce a 1 MHz change in the YTO frequency.

IF Section

The IF section processes the 10.7 MHz output of the RF section and sends the detected video to the ADC/interface section. The following major assemblies are included in this section:

A3 interface assembly

A4 log amplifier/calibration oscillator assembly

A5 IF assembly

The spectrum analyzer uses trace-data manipulation to generate the 5 dB/DIV scale from the 10 dB/DIV scale. The A3 interface assembly amplifies and offsets the 10 dB/DIV video to generate the 2 dB/DIV scale. The 1 dB/DIV scale is generated from the 2 dB/DIV scale through trace data manipulation. The first 50 dB of IF gain (log and linear mode) is achieved using the A5 assembly linear step-gain amplifiers. The A4 assembly video-offset circuit provides the remaining 60 dB of log mode IF gain. The A4 assembly linear amplifiers provide 40 dB of linear mode gain. IF gain steps of less than 10 dB (regardless of the reference level) are accomplished on the A5 assembly.

A4 Log Amplifier/Cal Oscillator Assembly

The A4 log amplifier has separate log and linear amplifier paths. After amplification, the signal path consists of a linear detector, video log amp, buffer amplifier, video offset, and video buffer amplifier. Other auxiliary functions include the frequency counter prescaler/conditioner, the AM/FM demodulator, and down-conversion to 4.8 kHz for digital resolution bandwidths of 1 Hz through 100 Hz.

The cal oscillator, which is part of A4, supplies the stimulus signal for automatic IF adjustments. Normally, the oscillator operates only during retrace (for a few milliseconds) to adjust part of the IF. (All IF parameters will be re-adjusted approximately every five minutes.) With continuous IF adjust on, a group of IF parameters are adjusted during each retrace period (non-disruptive). If continuous IF adjust is off, the most recent IF calibration data will be used.

The IF parameters adjusted include step gains, log amplifier gain and offset, bandwidth centering, 3 dB bandwidth, bandwidth amplitude, crystal-filter symmetry, and oscillator frequency used in 1 Hz through 100 Hz resolution bandwidths.

The cal oscillator output has three forms (all –35 dBm):

• 10.7 MHz

• 9.9 to 11.5 MHz in 100 kHz steps

• Frequency sweeps from 20 kHz to 2 kHz centered at 10.7 MHz (lasting 5 to 60 ms respectively)

The purpose of these signals is to:

- Adjust gains, log amps, and video slopes and offsets.

- Adjust 3 dB bandwidth and center frequencies of LC resolution BW filters (30 kHz through 1 MHz).

- Adjust 3 dB bandwidth, symmetry, and gain of the crystal resolution BW filters (300 Hz through 10 kHz).

- Adjust gain and gain-vs-frequency for digital resolution bandwidths (1 Hz through 100 Hz).

A5 IF Assembly

The A5 IF assembly has four crystal filter poles, four LC filter poles, and step gain amplifiers. The crystal filters provide resolution bandwidths of 300 Hz to 10 kHz. The LC filters provide resolution bandwidths of 30 kHz to 2 MHz. All filter stages are in series. PIN diode switches bypass unwanted stages.

An automatic IF adjustment, in spectrum analyzer firmware, sets center frequency and 3 dB bandwidth of all filter poles through varactor and PIN diodes. The firmware also controls crystal-pole symmetry and the step gain amplification.

ADC/Interface Section

The ADC/interface section is the link between the controller section and the rest of the spectrum analyzer. It controls the RF, synthesizer, and IF sections through address and data lines on the W2 control cable (analog bus). Analog signals from these sections are monitored by the ADC/interface section ADC (analog to digital converter) circuit.

The ADC/interface section includes the A3 interface assembly, A1A1 keyboard, and A1A2 RPG (front-panel knob). The A3 assembly includes log expand, video filter, peak detector, track-and-hold, real-time DACs, RF gain DACs, +10 V reference, and ADC circuitry. The digital section of the assembly includes ADC ASM, sweep trigger, keyboard interface, RPG interface, and analog bus interface circuitry.

ADC

The spectrum analyzer can digitize signals with either the main ADC on the A3 interface assembly, or the optional A16 fast ADC (Option 007). The main ADC is used for digitizing video signals (when the sweep time is $\geq$30 ms) and various other signals such as PLL error voltages. The fast ADC is used only to digitize video signals for sweep times $\leq$30 ms.

Main ADC (part of A3 interface assembly)   For slower sweep times (≤30 ms), the spectrum analyzer uses a successive-approximation type of ADC. The main ADC has a 10-bit resolution but it is realized with 12-bit hardware. The ADC algorithmic state machine (ADC ASM) controls the interface between the start/stop control and the ADC itself, switching between positive and negative peak detectors when the NORMAL detector mode is selected, and switching the ramp counter into the ADC for comparison to the analog sweep ramp.

Fast ADC   In EC-series instruments, and when Option 007 is installed in E-series instruments, and sweep times ≤30 ms are selected, the spectrum analyzer digitizes video signals with the A16 fast ADC. The fast ADC uses an 8-bit flash ADC, sampled at a 12 MHz rate. Only POS PEAK, NEG PEAK, and SAMPLE detector modes are available with fast ADC; NORMAL detector mode is not available. Pre-triggering is possible with fast ADC.

Log Expand/Video Functions

The A3 interface assembly performs log expand and offset functions. The log expand/log offset amplifier provides a 2 dB/Div log scale. When the main ADC is used, the 5 dB/Div scale is derived by multiplying the digitized 10 dB/Div trace data by two in the CPU. When the fast ADC is used, the 5 dB/Div scale is derived by amplifying the video signal by two. The 1 dB/Div scale is similarly derived by either multiplying the 2 dB/Div trace data by two (main ADC) or amplifying the video signal by two (fast ADC).

The spectrum analyzer uses two types of video filters. An RC low-pass circuit provides 300 Hz to 3 MHz video bandwidths. Video bandwidths ≤100 Hz are generated using digital filtering. Digitally filtered video bandwidths use a sample detector. When sample detection is selected, the effective video bandwidth is limited to approximately 450 kHz. When a digital filter is selected, a D appears along the left edge of the CRT, indicating that something other than the normal detector mode is being used.

After filtering, the video is sent to the positive and negative peak detectors. These detectors are designed for optimum pulse response. The positive peak detector resets at the end of each horizontal "bucket" (there are 601 such buckets across the screen). The negative peak detector resets at the end of every other bucket. When reset, the output of the peak detector equals its input.

Triggering

The spectrum analyzer has five trigger modes: free run, single, external, video, and line. The free run and single trigger signal comes from the 1 MHz ADC clock. The line trigger signal comes from the A6 power supply. Video triggering originates from the A3 video filter buffer circuit. External triggering requires either a high or low TTL logic level as determined by the setting of the trigger polarity function. The external trigger signal is received from a rear-panel BNC connector. A DAC in the trigger circuit sets the video trigger level. The trigger circuit is responsible for setting HSCAN high.

Controller Section

The controller section includes the A2 controller assembly and A19 GPIB assembly. The battery on the rear panel provides battery backup for state and trace storage.

In 8562EC instruments the A2 contains the CPU, RAM, ROM, the display ASM, Fast ADC circuitry, GPIB interface, control, frequency counter, display RAM, option module interface, and EEROM.

In 8562E instruments the A2 contains the CPU, RAM, ROM, the display ASM and line generators, CRT blanking, focus, intensity, GPIB interface, control, frequency counter, display RAM, option module interface, and EEROM. In 8562E instruments the A2 assembly controls the A17 CRT driver through W7.

The A19 GPIB is a mechanical interface between the standard GPIB connector and the ribbon cable connector on the A2 controller assembly.

All six RAM ICs (four RAM ICs on 16 MHz controller assemblies) are battery-backed. The battery-backed RAM stores trace information (two display memory RAMs) and spectrum analyzer state information (two program RAMs). A total of eight traces and ten states may be stored. Typical battery life is five years with the lithium battery. Trace and state information may be retained for up to 30 minutes with a dead battery and power turned off. This is due to the very low data retention current of the RAM.

EEROM

The EEROM stores important amplitude-related correction data. This includes data for LO distribution amplifier DACs, preselector slope and offset DACs, RF gain DACs (flatness correction), and preselector peak DAC. The spectrum analyzer serial number, model number, and installed options are also stored in EEROM.

Firmware

The spectrum analyzer firmware reads the model number and installed options from the EEROM to determine how to respond to certain keystrokes.

Display ASM

Much of the miscellaneous digital control is performed by A2U100. U100 functions as the display ASM (algorithmic state machine) and character ROM. It also converts the 16-bit CPU data bus to an 8-bit data bus for the rest of the spectrum analyzer.

Display/Power Supply Section

A6 Power Supply

The A6 power supply is a switching supply operating at 40 kHz for low voltages in both EC-series and E-series instruments.

In E-series instruments, the power supply also provides the 30 kHz signal for the CRT supplies (cathode, filament, +110 Vdc, and post accelerator). The A6A1 high voltage module contains the high-voltage transformer and post-accelerator multiplier. Power is distributed through W8 to A17 and through W1 to the rest of the assemblies. A6A1W2 supplies CRT cathode and filament voltages to the A17 assembly.

The speed of the spectrum analyzer fan is variable. A thermistor on A6 senses the temperature and adjusts the fan speed accordingly. This allows the spectrum analyzer to run quietly in most room-temperature environments and faster (louder) only when necessary.

A17 LCD Display Driver (EC-series)

The display is an LCD color flat panel screen with 640 X 480 VGA resolution. A connector for an external VGA is available at the rear panel. The A17A1 backlight supply provides the high voltage to supply the two backlights in the LCD display. The LCD display is not adjustable.

The display driver board consists of the Hitatchi 7707 processor, an Actel FPGA, DRAM, SRAM, a filter circuit, and a video DAC. This board monitors the 8560 EC-series controller board, copies display instructions to local memory, creates a bitmap from the data, and generates the signals needed to drive the LCD and a VGA monitor. The video DAC converts the digital color information from the LCD to analog; these analog signals drive the RGB color lines on the VGA port on the rear panel.

A17 CRT Display Driver (E-series)

The line generators on the A2 assembly drive the A17 CRT driver. The A17 assembly contains X and Y deflection amplifiers, focus and intensity grid amplifiers, and miscellaneous CRT bias circuitry. The high voltage is supplied by A6A1 high voltage module.

In fast-analog zero-span mode (sweep times ≤30 ms without Option 007), the 0-SPAN VIDEO signal from A3 and the sweep ramp from A14 connects to the A17 CRT driver. The graticule and annotation are still digitally drawn.

HP 8562E AND 8562EC SIMPLIFIED BLOCK DIAGRAM

FIGURE 7-8. SIMPLIFIED BLOCK DIAGRAM

8562E OVERALL BLOCK DIAGRAM
(SHEET 1 OF 4)

s1129c
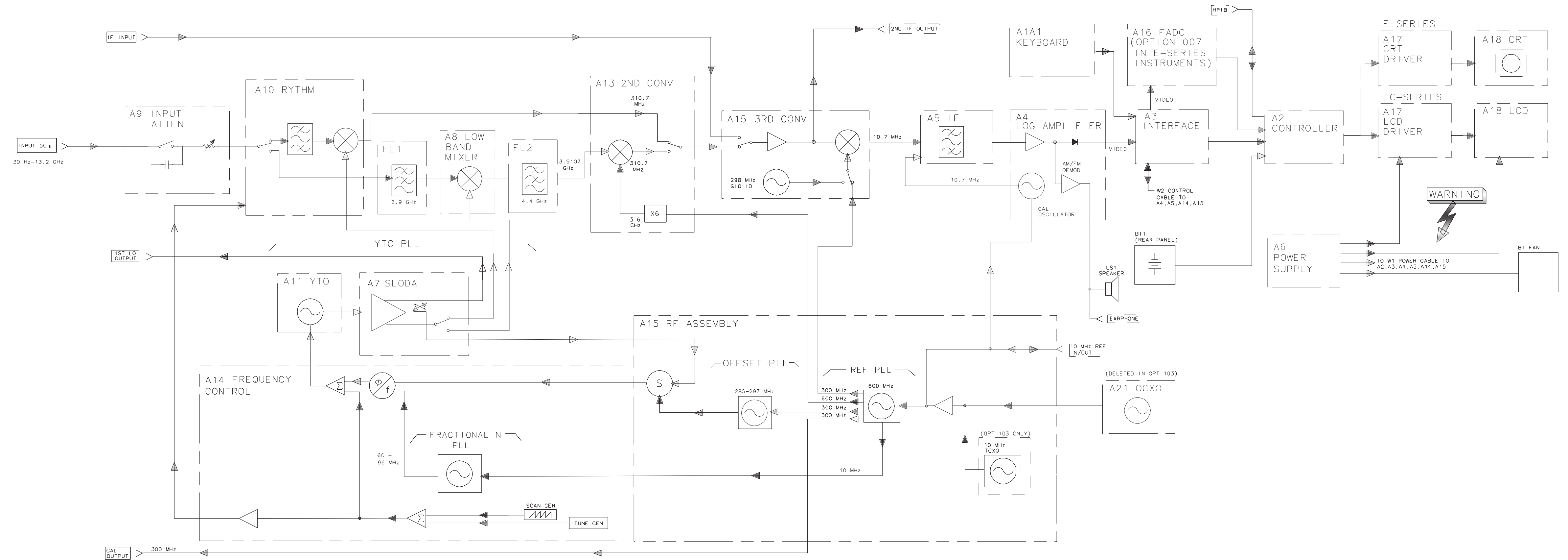
FIGURE 7-9. 8562E AND 8562EC OVERALL BLOCK DIAGRAM
(SHEET 1 OF 4)
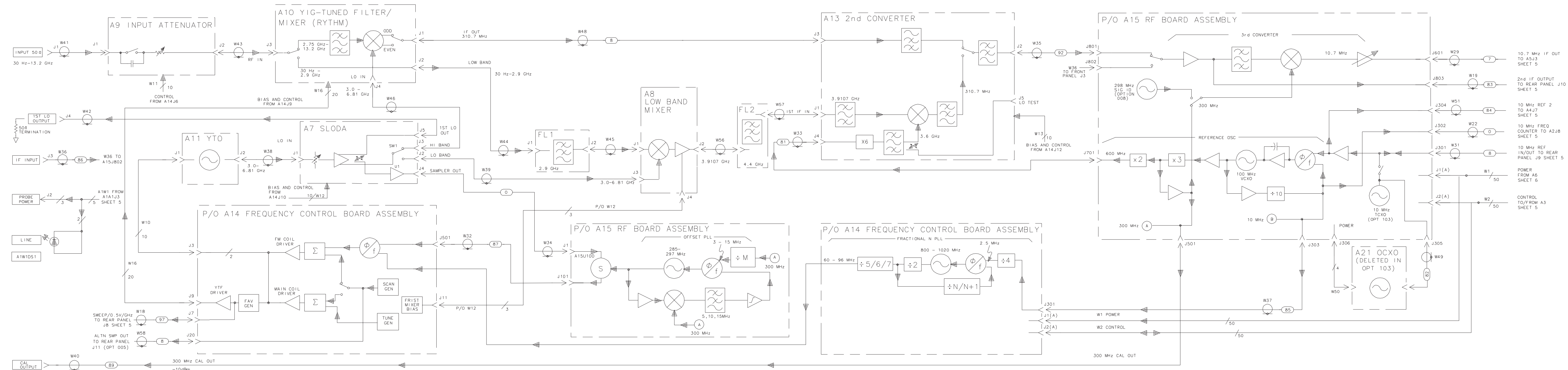
8562EC OVERALL BLOCK DIAGRAM
(SHEET 2 OF 4)
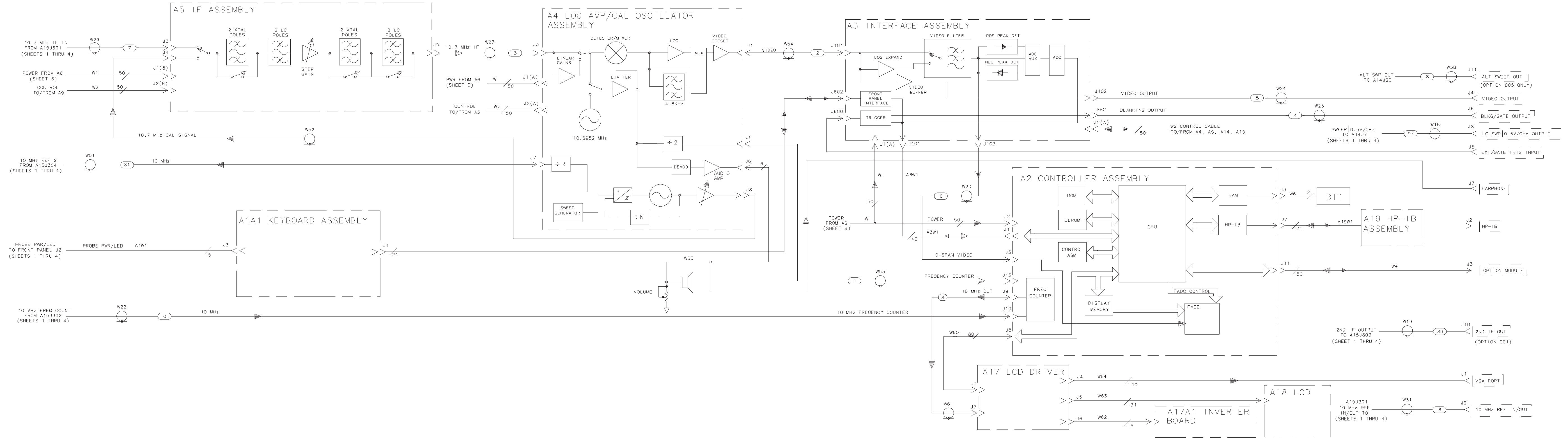
8562 OVERALL BLOCK DIAGRAM
(SHEET 3 OF 4)

s1131c

FIGURE 7-9 8563E OVERALL BLOCK DIAGRAM (SHEET 3 OF 4)
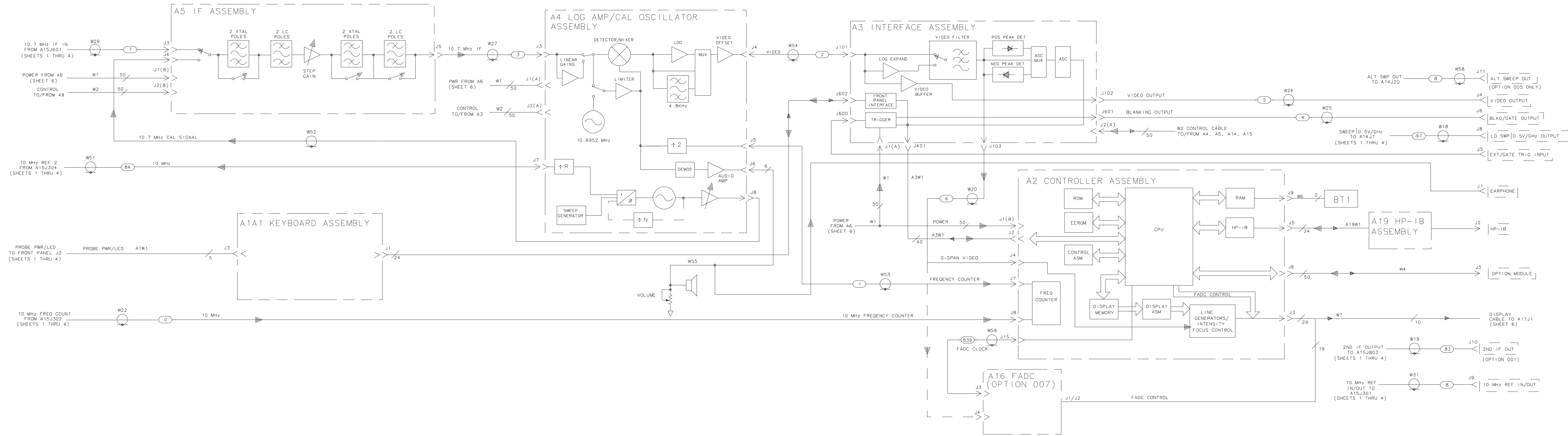
HP 8560E-Series OVERALL BLOCK DIAGRAM
(SHEET 4 OF 4)

8   ADC/Interface Section

Introduction

The ADC/Interface section includes the A1A1 keyboard, A1A2 RPG (rotary pulse generator), A3 interface, and A16 fast ADC (Option 007) assemblies. Table 8-1 on page 379 lists signal versus pin numbers for control cable W2.

Table 8-1   **W2 Control Cable Connections**

Signal	A3J2 (pins)	A4J2 (pins)	A5J2 (pins)	A14J2 (pins)	A15J2 (pins)
D0	1*	1	50	1	1
D GND	2*	2	49	2	2
D1	3*	3	48	3	3
D2	4*	4	47	4	4
D3	5*	5	46	5	5
D4	6*	6	45	6	6
D GND	7*	7	44	7	7
D5	8*	8	43	8	8
D6	9*	9	42	9	9
D7	10*	10	41	10	10
A0	11*	11	40	11	11
D GND	12*	12	39	12	12
A1	13*	—	38	13	13
A2	14*	—	37	14	14
A3	15*	15	36	15	15
A4	16*	—	35	16	16
D GND	17*	17	34	17	17
A5	18*	—	33	18	—
A6	19*	—	32	—	—
A7	20*	—	31	20	—
D GND	21*	21	30	21	21
LRF_STB	22*	—	—	—	22
LFC_STB	23*	—	—	23	—
LIF_STB	24*	—	27	—	—
CAL OSC TUNE	25	25*	—	—	—
LLOG_STB	26*	26	—	—	—
* Indicates signal source					

Table 8-1   **W2 Control Cable Connections**

Signal	A3J2 (pins)	A4J2 (pins)	A5J2 (pins)	A14J2 (pins)	A15J2 (pins)
VCMON	—	—	—	27	—
D GND	28*	28	23	28	28
RT PULSE	29*	—	—	—	—
HSCAN	30*	—	—	30	—
D GND	31*	31	20	31	31
RESERVED	—	—	—	—	—
OFL ERR	33	—	—	—	33*
R/T DAC3	34*	—	—	—	—
A GND	35*	35	16	35	35
RF GAIN	36*	—	—	—	36
LO3 ERR	—	—	—	37	37*
A GND	38*	38	13	38	38
LVFC_ENABLE	39*	—	—	39	—
FC ERR	40	—	—	40*	—
A GND	41*	41	10	41	41
YTO ERR	42	—	—	42*	—
+10V REF	43*	43	—	—	43
A GND	44*	44	7	44	44
SCAN RAMP	45	—	—	45*	—
VIDEO TRIGGER	46*	—	—	—	—
A GND	47*	47	4	47	47
NC	—	—	—	—	—
R/T DAC2	49*	—	—	—	—
R/T DAC1	50*	—	—	50	—
* Indicates signal source.					

Troubleshooting Using the TAM

Refer to Chapter 7 , "General Troubleshooting," for information on enabling the TAM for use with the 8562E/EC Spectrum Analyzer.

When using Automatic Fault Isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 8-2 on page 382 to locate the manual procedure.

Table 8-3 on page 383 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 8-1 on page 381 illustrates the location of the A3 test connectors.

Figure 8-1   **A3 Test Connectors**
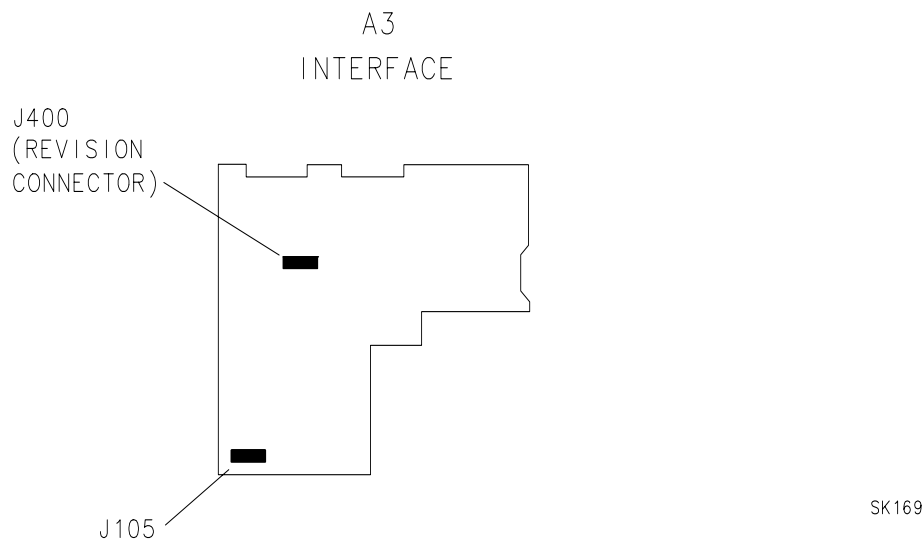
Automatic Fault Isolation

Analog data bus errors that occur during Automatic Fault Isolation result from either a shorted W2 control cable or faulty A3 assembly. Perform the following steps to determine the cause of the error.

1. Disconnect W2 from A3J2 and repeat the Automatic Fault Isolation procedure.

2. If the analog data bus error is still present, troubleshoot the A3 Interface assembly. If the error disappears, look for a short on W2 or another assembly connecting to it.

3. To isolate a short on W2, reconnect W2 to A3J2 and disconnect W2 from all other assemblies.

4. Repeat the Automatic Fault Isolation routine.

5. If the analog data bus error is still present, W2 is shorted. If the error disappears, reconnect the other assemblies one at a time and repeat the procedure. Once the faulty assembly is reconnected to W2, the error should reappear.

Table 8-2   **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check ADC ASM	ADC ASM
Check ADC MUX	ADC MUX
Check ADC Start/Stop Control	ADC Start/Stop Control
Check Analog Bus Drivers	Automatic Fault Isolation *(in this chapter)* Analog Bus Drivers
Check Analog Bus Timing	Automatic Fault Isolation *(in this chapter)* Analog Bus Timing
Check Interface Strobe Select	Interface Strobe Select
Check Keyboard Interface	Keyboard/RPG Problems
Check Negative Peak Detector	Positive/Negative Peak Detectors *(steps 3 through 10)*
Check Peak Detector Reset	Peak Detector Reset
Check Positive Peak Detector	Positive/Negative Peak Detectors *(steps 3 through 10)*
Check Real Time DAC	Preselector Peaking Control (Real Time DAC)
Check Ramp Counter	Ramp Counter
Check RF Gain DACs	Band Flatness Control (RF Gain DACs)
Check Rosenfell Detector	Rosenfell Detector
Check RPG Interface	Keyboard/RPG Problems
Check Track and Hold	Track and Hold
Check Trigger	Triggering Problems
Check Variable Gain Amplifier (VGA)	Variable Gain Amplifier (VGA)
Check Video Filter	Video Filter
Check Video Filter Buffer Amplifier	Video Filter Buffer Amplifier
Check Video MUX	Video MUX

Table 8-3   TAM Tests versus A3 Test Connectors

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A3J105	Video Input to Interface	MS1
	Video to Rear Panel	MS1, MS2
	Video MUX	MS1, MS3
	LOG Offset/LOG Expand	MS1, MS3
	Video Filter Buffer Amp.	MS3, MS5, OS1
	Video Peak Detectors	MS5, MS6
	ADC MUX	MS6
	Variable Gain Amplifier	MS6, MS7
	Track and Hold	MS7, MS8
A3J400	Revision	MS2
	Trigger	MS8
	ADC Start/Stop Control	MS7
	Video Trigger DAC	MS1
	Real Time DAC #1	MS3
	RF Gain DACs	MS6

Keyboard/RPG Problems

Keyboard Interface

Refer to function block G of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

A pressed key results in a low on a keyboard sense line (LKSNS0 through LKSNS7). This sets the output of NAND gate U607 high, generating KBD/RPG_IRQ. The CPU determines the key pressed by setting only one keyboard scan line (LKSCN0 through LKSCN5) low through U602 and reading the keyboard sense lines.

1. If none of the keys or RPG responds, check ribbon cable, A1A1W1. (This cable connects the A1A1 keyboard to the A3 interface assembly.) The keys are arranged in a row/column matrix, as shown in Table 8-4 on page 384.

2. If an entire row or column of keys does not respond, and the RPG does respond, there might be an open or shorted wire in A1A1W1.

Table 8-4   **Keyboard Matrix**

	LKSNS0	LKSNS1	LKSNS2	LKSNS3	LKSNS4	LKSNS5	LKSNS6	LKSNS7
LKSCN0	CONFIG	SAVE	RECALL	GHz	MHz	kHz	Hz	PRESET
LKSCN1	MODULE	TRIG	DISP	9	6	3	BK SP	↑
LKSCN2	PEAK SEARCH	BW	TRACE	8	5	2	•	↓
LKSCN3	FREQ COUNT	AUTO COUPLE	MKR →	7	4	1	0	HOLD
LKSCN4	SWEEP	SK1	SK2	SK3	SK4	SK5	SK6	MKR
LKSCN5	AUX CTRL	MEAS/ USER	CAL	SGL SWP	COPY	FRE- QUENCY	SPAN	AMPLI- TUDE

3. Check that all inputs to NAND gate A3U607 (LKSNS lines) are high when no key is pressed. If any input is low, continue with the following:

   a. Disconnect A1A1W1 from A3J602 and again check all inputs to U607.

   b. If any input is low with A1A1W1 disconnected, suspect A3U604, A3U607, or A3U602.

   c. Reconnect A1A1W1 to A3J602.

4. Monitor A3U607 pin 8 with a logic probe. A TTL high should be present when any key is held down. Monitor this point while pressing each key in succession.

5. Check that the LKSCN lines (outputs of A3J602 pins 1 through 6) read a TTL low with no key pressed. (Any TTL high indicates a faulty A3 Interface assembly.)

6. Check that a pulse is present at each LKSCN output of U602 when a key is pressed.

7. Check that only one input to U607 (LKSNS lines) goes low when a key is pressed.

8. Check that U602 pin 9 (LKBD_RESET) pulses low when a key is pressed.

9. If LKBD_RESET is incorrect and a pulse is not present at each of the LKSCN outputs of U602 when a key is pressed, check for LWRCLK and LSCAN_KBD.

RPG Interface

Refer to function block J of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

U608B latches the RPG direction from the two RPG outputs, RPG_COUNT and RPG_COUNT1. Counterclockwise RPG rotation produces low-going pulses which result in a high output on U608B. Clockwise RPG rotation results in a low output from U608B. U612A provides the edge to trigger one-shot U423B, which generates a 90 ms pulse. This pulse gates U610A for counting of RPG pulses by U606. Gates U610D and U614D prevent retriggering of U423B until its 90 ms pulse has timed out.

NOTE   Elsewhere, RPG_COUNT1 is referred to as RPG_01 and RPG_COUNT is referred to as RPG_02.

1. Monitor A3U401 pin 2 with a logic probe or oscilloscope. Pulses should be present as the RPG is rotated.

2. Monitor A3U608 pin 12 as the RPG is rotated. Pulses should be present.

3. If pulses are missing at both points, check for power and ground signals to A1A1W1 and A1A2W1. If both power and ground are there, the A1A2 RPG is probably defective.

4. If pulses are missing at only one point, check for an open or short on A1A1W1 and A1A2W1. If these cables are working properly, A1A2 RPG is probably defective.

5. Press **LINE** to turn spectrum analyzer off and disconnect A1A1W1 from A3J602. Jumper A3U608 pin 12 (RPG_COUNT1) to U608 pin 14 (+5 Vdc). Jumper U401 pin 2 (RPG_COUNT1) to U511 pin 11 (HDPKD_CLK). This provides a 7.8 kHz square wave to the RPG_COUNT input of the RPG Interface.

6. Press **LINE** to turn spectrum analyzer on.

7. Check A3U608 pin 9 for narrow, low-going pulses approximately every 90 ms.

8. Check A3U608 pin 13 (LRPG_RESET) for narrow, low-going pulses approximately every 90 ms.

9. Check A3U612 pin 5 for narrow, low-going pulses approximately every 90 ms.

10. Check U608 pin 5 (HRPG_IRQ) for narrow, high-going pulses approximately every 90 ms.

11. If HRPG_IRQ is correct but LRPG_RESET is incorrect, check U505 pin 13 (LKBD/RPG_IRQ) for narrow, low-going pulses approximately every 90 ms.

12. If HRPG_IRQ and LKBD/RPG_IRQ are correct but LRPG_RESET is incorrect, suspect a failure on the A2 controller assembly.

13. Check U610 pin 3 for a 7.8 kHz square wave. Check U606 pin 2 (HRPG_RESET) for narrow, high-going pulses approximately every 90 ms. Refer to Table 8-5 on page 386 and check the frequencies at divide-by-16 counter A3U606.

14. If all the checks above are correct but the spectrum analyzer does not respond to the RPG, suspect a problem in either the A1A2 RPG or the A1A1 Keyboard.

15. Press **LINE** to turn spectrum analyzer off.

16. Reconnect A1A1W1 to A3J602 and remove all jumpers.

Table 8-5   **Counter Frequencies**

A3U606 pin #	Nominal Frequency (Hz)
3	3900
4	1950
5	975
6	488
11	244
10	122
9	61

Triggering or Video Gating Problems

Refer to function block H of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The 1 MHz ADC clock provides synchronization in FREE RUN and SINGLE triggering. LINE triggering synchronization originates on the A6 power supply. Trigger MUX A3U613 selects between FREE RUN, VIDEO, LINE, and EXTERNAL trigger sources. The trigger signal sets the output of the HSCAN latch high. HBADC_CLK0 provides the trigger signal for FREE RUN. The VIDEO TRIG signal must be at least 25 mV (0.25 divisions) peak-to-peak to trigger in video trigger mode.

The trigger for Gated Video has two modes of operation, level mode and edge mode. In the edge mode, positive-edge or negative-edge triggering can be selected. Output 0 from pin 10 of A3U617 generates the gate delay and output 1 from pin 13 of A3U617 generates the gate length. The duration of these two time intervals is set using front-panel softkeys under the **SWEEP** key. The trigger input for Gated Video is the rear-panel EXT/GATE TRIG INPUT (TTL > 10 kΩ).

1. Check that the trigger MUX is receiving the proper trigger source information by selecting each of the following trigger modes and checking the TRIG_SOURCE0 and TRIG_SOURCE1 lines as indicated in Table 8-6 on page 387.

2. If a trigger mode does not work, check that a trigger signal is present at the appropriate trigger MUX input, as indicated in the table.

Table 8-6   **Trigger MUX Truth Table**

Trigger Mode	TRIG_SOURCE0 U613 pin 14	TRIG_SOURCE1 U613 pin 2	MUX Input Pin Number U613
FREE RUN	L	L	6
VIDEO	H	L	5
LINE	H	H	3
EXTERNAL	L	H	4

3. Check that the appropriate trigger MUX input signal is present at the trigger MUX output (A3U613 pin 7).

4. To check the video trigger level DAC, connect the positive lead of a DVM to A3J400 pin 1 and the negative DVM lead to A3TP4.

5. Press **TRIG** and **VIDEO**.

6. Press the STEP ▼ key several times while noting the DVM reading and position of the video trigger level on the screen.

7. Check that the voltage displayed on the DVM changes by 1 V for each step of the VIDEO TRIG LEVEL.

8. If the voltage changes incorrectly, proceed as follows:

   a. Check the −10 Vdc reference (A3U409 pin 4).

   b. While using the front-panel knob to adjust the video trigger level, check for the presence of pulses on A3U409 pin 15 (LDAC2).

   c. While using the front-panel knob to adjust the video trigger level, check for the presence of pulses on A3U409 pin 16 (LWRCLK).

   d. Check that pulses are present on U409 pin 6 (IA0).

9. If the LWRCLK and LDAC2 signals are not correct, refer to "Interface Strobe Select" on page 412.

10. If correct trigger pulses are present at the trigger MUX output (A3U613 pin 7), but the instrument does not appear to be sweeping, proceed as follows:

    a. Press **PRESET**, **SWEEP**, and **DLY SWP ON OFF** until ON is underlined, then **DLY SWP [ ]** 30 milliseconds.

    b. Using an oscilloscope, check for activity at pins 1 and 3 of A3U615A.

    c. If there is activity at pin 1 but not at pin 3 of A3U615A, suspect A3U616 or A3U617.

    d. If there is activity at pin 1 and pin 3 of A3U615A, suspect A3U615. (Check pin 5 for activity.)

11. If there is a problem with Video Gating, proceed as follows:

    a. Press **PRESET** and set the spectrum analyzer as follows:

        Center frequency .... 300 MHz
        Span .... 0 Hz
        Sweep time .... 150 ms

    b. Press **TRIG**, **EXTERNAL**, then **SWEEP** and **GATE ON OFF** until ON is underlined.

    c. Press **GATE DLY [ ]** 10 milliseconds, then press **GATE LEN [ ]** 30 milliseconds.

    d. Connect a pulse/function generator (such as an 8116A) to provide a 5 V peak-to-peak square wave (TTL level) to the spectrum analyzer rear-panel EXT/GATE TRIG INPUT and also (using a BNC tee) to the channel 4 input of the oscilloscope (54501A).

    e. Set the pulse/function generator to NORMAL mode with a duty cycle of 50% and a frequency of 10 Hz.

f. Press the following keys on the oscilloscope:

CLEAR DISPLAY

off frame axes grid .... highlight **grid**

connect dots off on .... highlight **on**

TRIG

source 1 2 3 4 .... highlight **4**

level .... 2 V

TIMEBASE

TIMEBASE .... 50 ms/div

CHAN

CHANNEL 1 2 3 4 off on

highlight **CHANNEL 1 on**

set V/div to 0.2 V and offset to 0.6 V (10:1 probe used)

highlight **CHANNEL 4 on**

set V/div to 2 V and offset to 0 V

DISPLAY

DISPLAY norm avg env .... highlight **norm**

g. Using a 10:1 probe connected to channel 1 of the oscilloscope, check for activity at pins 10 and 13 of A3U617.

h. If either pin (or both) show no activity, check for activity at pin 21 (LTIMER) of A3U617.

i. If LTIMER is not active, troubleshoot the Interface Strobe Select circuitry (block K).

j. If there was activity at pins 10 and 13 of A3U617, suspect A3U616.

Preselector Peaking Control (Real Time DAC)

Refer to function block H of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*. The spectrum analyzer uses a real-time DAC (R/T DAC1) to peak the preselector.

1. Press **PRESET** on the spectrum analyzer and set the span to 0 Hz.

2. Connect a positive DVM lead to A3J400 pin 3 and the negative DVM lead to A3TP4.

3. Press **MKR**, **AUX CTRL**, **INTERNAL MIXER**, and **PRESEL MAN ADJ**.

4. Monitor the DVM reading while changing the PRESELECTOR TUNE value from 0 to 255. The PRESELECTOR TUNE value is the R/T DAC1 setting.

5. Check that the DVM reading increases from 0 to approximately +10 Vdc as R/T DAC1 is set from 0 to 255.

6. If the voltage does not change as described, set the spectrum analyzer to single trigger mode and check the following:

   a. Check that A3U409B pin 18 is at −10 Vdc.

   b. Check for the presence of pulses at U409 pin 6 (IA0).

   c. Check that pulses are present at U409 pin 15 (LDAC2).

   d. Check that pulses are present at U409 pin 16 (LWRCLK).

7. If the LDAC2 or LWRCLK signals are incorrect, refer to "Interface Strobe Select" on page 412.

Flatness Control (RF Gain DACs)

Refer to function block M of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

RF Gain DACs control the A15 assembly flatness compensation amplifiers. The RF Gain DACs are arranged so that the output of one DAC is the voltage reference for the other DAC. This results in an RF GAIN voltage which is exponentially proportional to the DAC settings. Each DAC is set to the same value. The A15 RF assembly converts the RF GAIN signal to a current for driving the PIN diode attenuators in the Flatness Compensation Amplifiers. The exponentially-varying voltage compensates for the nonlinear resistance-versus-current characteristic of the PIN diodes.

1. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR ENA position.

2. Press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **FLATNESS**, and **FLATNESS DATA**. Press **NEXT BAND** until "FLATNESS BAND # 0" is displayed.

3. Press the ▲ key until "DATA @ 300 MHz" is displayed. Note the number directly below "DATA @ 300 MHz"; this is the RF Gain DAC value.

4. Connect a positive DVM lead to A3J400 pin 13 and the negative DVM lead to A3TP4.

5. Check that the DVM reading increases from near 0 Vdc to between −1.3 and −1.9 Vdc as the RF Gain DAC setting is increased from 0 to 4095.

6. If the DVM readings are incorrect, press **PRESET**, **SGL SWP**, **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **FLATNESS**, and **FLATNESS DATA**. Press **NEXT BAND** until "FLATNESS BAND # 0" is displayed. Press the ▲ key until "DATA @ 300 MHz" is displayed. Proceed as follows:

   a. Check the +10 V reference.

   b. Check for narrow, low-going pulses at A3U417 pin 13 (LWRCLK).

   c. While rotating the front-panel knob, check for narrow, low-going pulses at A3U417 pin 1 (LDAC1) and pin 14 (LDACU1).

   d. While rotating the front-panel knob, check for narrow, low-going pulses at U417 pin 16 (L_IA0) and pin 15 (IA4).

7. If the LWRCLK, LDAC1, or LDACU1 is incorrect, refer to the Interface Strobe Select block in this chapter.

8. Place the WR PROT/ WR ENA jumper on the A2 controller assembly in the WR PROT position. Press **PRESET**.

A3 Assembly Video Circuits

Voltages from A3J101 to the A3 Variable Gain Amplifier correspond (approximately) to on-screen signal levels. (One volt corresponds to the top of the screen and zero volts corresponds to the bottom of the screen.) This is true for both log and linear settings except when the spectrum analyzer is in 1 dB/div or 2 dB/div. In these cases the log expand amplifier is selected, and 1 V corresponds to top-screen and 0.8 or 0.9 V corresponds to bottom-screen. The spectrum analyzer can be set to zero span at the peak of a signal to generate a constant dc voltage in the video circuits during sweeps.

1. Disconnect W26 from A3J101 and W20 from A2J4.

2. Connect W26 to A2J4.

3. Set the spectrum analyzer to the following settings:

   Span .... 0 Hz
   Sweep time .... 20 ms
   Resolution bandwidth .... 1 MHz
   Log/division .... 10 dB/DIV

4. If a trace is displayed, troubleshoot the A3 assembly. If a trace is absent, connect an oscilloscope to the rear-panel BLKG/GATE OUTPUT.

5. The presence of a TTL signal (TTL low during 20 ms sweep) indicates a good A3 Interface Assembly. Troubleshoot the IF section.

6. If the BLKG/GATE OUTPUT is always at a TTL high or low, troubleshoot the A3 trigger/video gating circuits.

7. Reconnect W26 to A3J101 and W20 to A2J4.

8. Remove the A3 assembly shield.

9. If the video filters appear faulty, see "Video Filter" on page 396.

10. If there appears to be a peak detector problem, refer to "Positive/Negative Peak Detectors" on page 398.

11. Connect the spectrum analyzer CAL OUTPUT to the INPUT 50Ω and set the controls as follows:

    Center frequency .... 300 MHz
    Span .... 0 Hz
    Reference level .... −10 dBm

12. If the spectrum analyzer works correctly in 5 dB/div and 10 dB/div but not in 1 dB/div or 2 dB/div, refer to "Log Offset/Log Expand" on page 394. Continue with step 13 if the problem involves on-screen amplitude errors which appear to originate in the video chain.

13. Press **CAL** and **IF ADJ ON OFF** until OFF is underlined. Monitor A3TP9 with an oscilloscope. If the voltage is not approximately +1 Vdc, troubleshoot the Log Amplifier on A4. (Refer to the IF troubleshooting procedure in Chapter 9 , "IF Section.")

14. To confirm proper video input to the video circuit, set the spectrum analyzer to Log 10 dB per division and change the reference level in 10 dB steps from −10 dBm to +30 dBm. At each 10 dB step, the input voltage should change 100 mV. The input level should be +0.6 Vdc for a +30 dBm reference level.

NOTE	The on-screen amplitude level will probably not change as expected, since the video circuitry is assumed to be faulty.

15. Monitor A3TP14 while stepping the reference level from −10 dBm to +30 dBm. If the voltage does not step approximately 100 mV per 10 dB step, refer to "Video MUX" on page 395.

16. If the Video MUX is working properly, monitor A3TP15 with the oscilloscope and step the reference level from −10 dBm to +30 dBm. If the voltage does not change 100 mV per 10 dB step, refer to "Video Filter" on page 396.

17. If the voltage at A3TP15 is correct, move the oscilloscope probe to A3TP17 and step the reference level between −10 dBm and +30 dBm. If the voltage does not change 100 mV per 10 dB step, refer to "Video Filter Buffer Amplifier" on page 397.

18. If the voltage at A3TP17 is correct, move the oscilloscope probe to A3TP6. Set the following controls to keep the ADC MUX set to the MOD_VIDEO input during the sweep:

    Sweep time .... 50 s
    Detector mode .... Sample

19. Step the reference level from −10 dBm to +30 dBm while monitoring the voltage change on the oscilloscope. If the voltage does not change 100 mV per 10 dB step, refer to "ADC MUX" on page 401.

20. If the voltage at A3TP6 is correct, move the oscilloscope probe to A3TP8 and step the reference level between −10 dBm and +30 dBm. If the voltage at A3TP8 is not the same as that at A3TP6, replace A3U110.

21. If the voltage at A3TP8 and A3TP6 are equal, move the oscilloscope probe to A3TP7.

22. Change the reference level from −10 dBm to 0 dBm. The voltage change on A3TP7 should be between 630 mV and 770 mV. If the voltage change is outside of these limits, refer to "Variable Gain Amplifier (VGA)" on page 404. The gain of the VGA should be 7 ±10%.

Log Offset/Log Expand

Refer to function block X of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The log scales are modified using a combination of amplification and digital trace manipulation. The video input to the A3 assembly is either 10 dB/div or linear. To obtain the 5 dB/div scale, the CPU manipulates the trace data from the 10 dB/div scale. To obtain the 2 dB/div scale, the video signal is amplified and offset so that top-screen in 10 dB/div corresponds to top-screen in 2 dB/div. To obtain the 1 dB/div scale, the CPU manipulates trace data from the 2 dB/div scale.

In 2 dB/div, Log Offset/Log Expand amplifies the top 20 dB of the display. This is done by offsetting the video signal by –0.8 V and providing a gain of 5 to the top 0.2 V of the video signal. The –0.8 V offset is accomplished by sinking 2 mA through R114 by current source U105/Q101.

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, and **IF ADJ OFF**.

2. Disconnect W26 (coax 2) from A3J101 and connect the output of a function generator to A3J101.

3. Set the function generator to the following settings:

   Output .... Sine wave
   Amplitude .... 1 V pk-to-pk
   DC Offset .... +500 mV
   Frequency .... 50 Hz

4. Set the spectrum analyzer sweep time to 50 ms.

5. Adjust the function generator amplitude and offset until the sine wave fills the entire graticule area.

6. Measure and note the function generator peak-to-peak voltage using an oscilloscope.

   $V_{(10 \text{ dB/div})}$ = _____V

7. Set the spectrum analyzer to 2 dB/div.

8. Readjust the function generator amplitude and offset until the sine wave again fills the entire graticule area.

9. Measure the function generator peak-to-peak voltage and dc offset.

   $V_{(2 \text{ dB/div})}$ = _____V

10. The ratio of voltage recorded in step 6 to the voltage recorded in step 9 should be 5 ±3%. If the ratio is not 5, troubleshoot the A3 Interface assembly.

11.Reconnect W26 to A3J101.

Video MUX

Refer to function block U of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** and set the spectrum analyzer controls as follows:

   Center frequency .... 300 MHz
   Span .... 0 Hz

2. Press **SGL SWP**, **CAL**, and **IF ADJ OFF**. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Check for a TTL high on A3U104 pin 2 and a TTL low on U104 pin 10. Set the spectrum analyzer to 2 dB/div and check for a TTL high on A3U104 pin 10 and a TTL low on A3U104 pin 2.

4. If the logic levels on A3U104 are incorrect, check the LLOG_STB signal as follows:

   a. Monitor A3U104 pin 9 with an oscilloscope or logic probe. Check that a 1 microsecond, low-going pulse is present when switching between 10 dB/div and 2 dB/div.

   b. Check the inputs to A3U104 (pins 3 and 11) while switching between 10 dB/div and 2 dB/div.

   c. If the logic signals are incorrect, refer to "Analog Bus Timing" on page 411 and "Analog Bus Drivers" on page 410.

5. Check comparators A3U109A/C for proper outputs. The outputs should be high when the non-inverting input is greater than the threshold voltage of +1.3 Vdc.

6. If A3U104 and A3U109 are working properly, set the **AMPLITUDE** and **REF LVL** to 0 dBm.

7. Monitor the voltage at A3TP14 while switching the spectrum analyzer between 10 dB/div and 2 dB/div. The voltage should switch between 0.8 and 0.4 Vdc.

8. If the voltage at A3TP14 is incorrect, suspect either A3Q220 or A3Q221.

9. The Video MUX will appear faulty if A3CR109 is shorted or leaky. Diode A3CR109 clamps the voltage at A3TP14 to –0.4 V when in log expand with less than 0.8 V at J101. To confirm this failure, lift the cathode of diode A3CR109 and perform steps 1 through 7 again.

10.To return the spectrum analyzer to automatic sweep, press **SWEEP**, **SWEEP CONT SGL** or press **PRESET**.

Video Filter

Refer to function block V of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The spectrum analyzer uses digital filtering for 1 Hz to 100 Hz video bandwidths. An RC low-pass filter is used for 300 Hz to 3 MHz video bandwidths. Various series resistances and shunt capacitances switch into the video filter to change its cutoff frequency.

When sample detection is selected, the effective video bandwidth is limited to approximately 450 kHz by the track and hold circuitry.

When Gated Video is selected, the video signal is "gated" (turned on periodically for a set duration of time). This function is shown in block V of the block diagram as a series switch that allows the video signal to pass only when it is closed. The actual switch, U109B/CR118, shunts the video to ground (video signal is passed only when the switch is open). The control circuitry for this switch is described under "Triggering or Video Gating Problems" in this chapter. The rear-panel EXT/GATE TRIG INPUT provides the connection for triggering in the Gated Video mode. The gate output signal is available at the rear-panel BLKG/GATE OUTPUT connector. Positive or negative edge mode, or level mode can be selected from the front panel.

1. Press **PRESET** and set the spectrum analyzer controls to the following settings:

   Center frequency .... 225 MHz
   Span .... 550 MHz
   Sweep time .... Uncoupled (MAN)

2. Press **CAL** and **IF ADJ OFF**.

3. Step the Video BW from 3 MHz to 10 kHz. At each step, the peak-to-peak deviation of the noise should decrease.

4. Step the Video BW down to 1 Hz. At each step, the amplitude of the LO feedthrough should decrease.

5. Refer to Table 8-7 on page 397 and check for correct latched levels for the selected video bandwidth setting.

6. If the output of latch A3U102 is not correct, trigger an oscilloscope on LLOG_STB (U102 pin 9) and monitor U102 pin 1 and other latch inputs while changing the video bandwidth.

7. If the inputs are incorrect, troubleshoot the analog bus. Correct inputs with bad outputs indicate a faulty U102.

8. Check that the outputs of A3U111A, A3U111B, and A3U107A/B/C/D are correct for their inputs. The outputs should be high with non-inverting inputs higher than the +1.4 V threshold voltage. If a voltage drop is noticed across these components, suspect A3CR109 or A3Q317B. Since no dc current flows through any of the series resistances or FETS (drain to source), no voltage drops should occur.

9. To return the spectrum analyzer to automatic sweep, press **SWEEP**, **SWEEP CONT SGL** or **PRESET**.

Table 8-7   **A3U102 Latch Outputs**

Video BW	Pin 2	Pin 5	Pin 7	Pin 10	Pin 12	Pin 15
300 Hz	H	L	L	L	L	L
1 kHz	L	L	L	L	L	H
3 kHz	L	H	L	L	L	L
10 kHz	L	L	L	L	H	L
30 kHz	H	L	H	L	L	L
100 kHz	L	L	H	L	L	H
300 kHz	L	H	H	L	L	L
1 MHz	L	L	H	L	H	L
3 MHz	L	L	L	H	L	L

Video Filter Buffer Amplifier

Refer to function block W of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The video filter buffer amplifier provides outputs for video trigger, positive and negative peak detectors, and the analog zero-span (sweeps <30 ms). The zero-span video output is terminated in 500 ohms on the A2 Controller assembly. The amplifier is a high-input-impedance buffer amplifier with a gain of one when properly terminated.

Current source U307C provides twice the current of Q316. Resistor R145 and current source U307D shift the dc level. Resistor R260 terminates the peak detector inputs in 500 ohms. The unterminated gain is 1.1. Diode CR114 prevents latch-up during positive overdrive conditions while CR113 protects Q318 during overdrive. Diode CR117 is a 12.7 V zener that limits the peak detector output to +1.5 V. Typically, limiting occurs at +1.1 V.

Positive/Negative Peak Detectors

Refer to function blocks Y and Z of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The following information pertains to the positive peak detector and is applicable to troubleshooting the negative peak detector.

The positive peak detector consists of an input amplifier (A3U204 and A3Q210) followed by detector diodes (A3CR203 and A3CR204) and hold capacitor A3C217. Output amplifier A3Q206, Q211, and Q212 buffers the hold capacitor. Both the input and output amplifiers have a gain of one. Each amplifier has local feedback. On the output amplifier the emitter of Q212 connects to the gate of Q206. On the input amplifier the feedback goes through Q209 and Q208 back to the base of U204D. Global feedback occurs from the output amplifier through R223 back to the input amplifier U204D. The peak detector resets through Q207.

1. Press **PRESET** and set the spectrum analyzer controls as follows:

   Center frequency .... 300 MHz
   Span .... 500 MHz
   Resolution bandwidth .... AUTO
   Video bandwidth .... AUTO
   Log dB/division .... 10 dB/DIV

2. If the spectrum analyzer does not meet the conditions in steps a through e below, the positive and negative peak detectors are probably faulty. Continue with step 3 to check the detectors.

   a. The peak-to-peak deviation of the noise in NORMAL detector mode should be approximately two divisions. Press **TRACE**, **TRACE B**, **CLEAR WRITE B**, **VIEW B**, **TRACE A**, **MORE 1 of 3**, and **DETECTOR MODES**.

   b. Select **DETECTOR POS PEAK** mode.

   c. Confirm that the noise is about one-third division peak-to-peak. The noise should also be no higher than the top of the noise level in NORMAL detector mode.

   d. Select **DETECTOR NEG PEAK** mode. The noise should be about one-third of a division peak-to-peak. The noise should also be no lower than the bottom of the noise in NORMAL mode.

   e. Select **DETECTOR SAMPLE** mode. Check that the noise appears between the top and bottom of the noise in NORMAL mode.

3. On the spectrum analyzer, connect the front-panel CAL OUTPUT to the INPUT 50Ω and set the controls to the following settings:

> Center frequency .... 300 MHz
> Span .... 0 Hz
> Sweep time .... 5 s
> Detector mode .... POS PEAK

4. Monitor A3TP17 and A3TP16 simultaneously with an oscilloscope.

5. Change the reference level from −10 dBm to +30 dBm and verify a voltage change at both A3TP17 and A3TP16 of 0.9 V to 0.5 V in 100 mV steps.

6. Check the entire range of the detector by substituting a dc source at J101 and varying its output from 0 V to 1 V.

7. If the peak detector appears latched up, check LPOS_RST (U422 pin 4) for a negative TTL level reset pulses. The reset pulses should occur every 130 μs and should be approximately 250 ns wide.

8. If the reset pulses are absent, troubleshoot the Peak Detector Reset circuitry.

9. If the reset pulses are present, check the gate of Q207. The pulses should be positive-going from −12.7 V to −1.35 V.

10. The peak detector can be made into a unity gain amplifier by shorting the, cathode of CR203 to the anode of CR204. If the peak detector functions normally as a unity gain amplifier, suspect Q208 or CR203 or CR204.

Peak Detector Reset

Refer to function block R of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

> Center frequency .... 300 MHz
> Span .... 0 Hz
> Sweep time .... 5 s
> Detector mode .... POS PEAK

2. Check that HHOLD (A3U526 pin 11) has 18 μs wide pulses every 128 μs.

3. Check that HODD (U408 pin 5) is a square wave with a period of 16.7 ms ($2 \times$ sweep time/600).

4. Check LPOS_RST (U422 pin 4) for 200 ns low-going pulses every 128 μs.

5. Check LNEG_RST (A3U422 pin 12) for 200 ns low-going pulses every 128 μs.

6. Set the detector mode to NORMAL and check that LNEG_RST (A3U422 pin 12) has two pulses spaced 40 μs apart and then a single pulse approximately 88 μs from the second pulse.

7. Check HMUX_SEL0 (A3U408 pin 3) and HMUX_SEL1 (A3U408 pin 9) according to .

Table 8-8   **HMUX_SELO/1 versus Detector Mode**

Detector Mode	HMUX_SEL0 (U408 pin 3)	HMUX_SEL1 (U408 pin 9)
NORMAL	15 μs pulse every 128 μs	40 μs pulse every 128 μs
SAMPLE	H	H
POS PEAK	H	L
NEG PEAK	L	H

Rosenfell Detector

Refer to function block S of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

If both HPOS_HLDNG and HNEG_HLDNG are high during the same bucket, HROSENFELL will also be set high. This indicates that the video signal probably consists of noise, since it rose and fell during the same period. The HROSENFELL signal is valid only when the NORMAL (rosenfell) detector mode is selected.

1. Remove anything connected to the 8561E or 8563E front-panel INPUT 50Ω connector. Press **PRESET** on the spectrum analyzer and set the controls as follows:

    Center frequency .... 300 MHz
    Span .... 0 Hz
    Sweep time .... 5 s
    Detector mode .... NORMAL

2. Check LPOS_RST and LNEG_RST as described in .

3. Check A3U423 pin 4 for two low-going 3.3 μs pulses 40 μs apart occurring every 130 μs.

4. Check that HROSENFELL (A3U610 pin 6) has two pulses spaced approximately 40 μs apart and then a third pulse 60 μs from the second pulse. Each pulse should be approximately 10 μs wide and low-going.

5. Monitor HROSENFELL with an oscilloscope while reducing the video bandwidth from 1 MHz to 1 kHz.

6. As the video bandwidth is decreased to 1 kHz, the HROSENFELL line should increasingly show a low logic level. With a video bandwidth of 1 kHz, a nearly flat line should be displayed on the CRT.

7. Set the sweep time to 50 ms. Externally trigger the oscilloscope using the spectrum analyzer rear-panel BLKG/GATE OUTPUT.

8. Check that HPOS_HLDNG (A3U416 pin 4) is mostly high with a 1 MHz video bandwidth and mostly low with a 1 kHz video bandwidth.

9. Check that LNEG_HLDNG (U408A pin 13) is mostly high with a 1 MHz video bandwidth and mostly low with a 1 kHz video bandwidth.

ADC MUX

Refer to function block AA of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC MUX switches various inputs into the video path for conversion by the ADC. The SCAN RAMP input is used during sweeps having a width of equal to or greater than 2.01 MHz times N, to control the timing of the ADC operations. Some combination of MOD_VIDEO, NEG_PEAK, and POS_PEAK is used for the video signal to be converted by the ADC. The YTO ERR, FCMUX, CAL OSC TUNE, and OFL ERR inputs are used only during diagnostic and auto adjust routines and during retrace.

1. Set the spectrum analyzer to the following settings:

        Center frequency .... 300 MHz
        Span .... 0 Hz
        Reference level .... −10 dBm
        Sweep time .... 50 s
        DETECTOR MODE .... SAMPLE

2. Refer to Table 8-9 on page 403 and check for correct logic levels at A3U108 pins 1, 15, and 16. Check for proper output signals at TP6. If the select lines are not changing, suspect the ADC ASM or the VGA/ADC MUX Control. If the select lines are changing, but the proper video inputs are not being switched to the output, replace U108. In SAMPLE mode, the input is MOD_VIDEO (pin 7); in POS PEAK mode, the input is POS_PEAK (pin 5); and in NEG PEAK mode, the input is NEG_PEAK (pin 6).

3. Check for the presence of the YTO ERR signal at A3J2 pin 42 with an oscilloscope probe.

4. If ERR 300 YTO UNLK or 301 YTO UNLK occurs and the voltage is near zero during a sweep and positive during retrace (YTO is being locked), the fault is on the A3 assembly. If a constant dc voltage is present, refer to the synthesizer troubleshooting procedure in Chapter 11 , "Synthesizer Section."

Table 8-9 **Logic Levels at A3U108**

Detector Mode	U108 pin 1	U108 pin 15	U108 pin 16
SAMPLE	H	L	H
POS PEAK	H	L	L
NEG PEAK	L	L	H

5. Set the spectrum analyzer to the following settings:

    Span .... 5 MHz
    Sweep time .... 50 ms

6. Check for the presence of the SCAN RAMP signal by connecting an oscilloscope probe to A3J2 pin 45 (component side of A3J2). Connect the negative-probe lead to A3TP4.

7. A 0 to 10 V ramp should be present in both LINE and FREE RUN trigger modes. If the waveform is present only in LINE trigger, ADC control signal HBADC_CLK0 may be faulty. Refer to "ADC Control Signals" on page 405.

8. If the scan ramp is present, but is not being switched to the output of U108, replace U108. If the scan ramp is absent in either mode, do the following:

    a. Connect the oscilloscope probe to A3J400 pin 15 (HSCAN).

    b. A TTL signal (high during 50 ms sweep time and low during retrace) should be present, indicating A3 is working properly. Refer to the synthesizer troubleshooting procedure in Chapter 11 , "Synthesizer Section." A faulty TTL signal indicates a bad A3 Interface assembly.

9. Set the spectrum analyzer to the following settings:

    Sweep time .... 100 ms
    Span .... 100 MHz

10. Press **CAL** and **IF ADJ ON** and check for the presence of the CAL OSC TUNE signal by monitoring A3J401 pin 25 with an oscilloscope. If ERR 499 CAL UNLK is displayed and a signal within the range of −10 V to +10 V is present during part of the retrace period, the fault is on the A3 assembly.

11. If a constant dc voltage is present during the sweep and all of the retrace period, refer to the IF Section troubleshooting procedure in Chapter 9 , "IF Section."

Variable Gain Amplifier (VGA)

Refer to function block AB of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The VGA provides adjustable gain in the video path. Its nominal gain of 7 can be adjusted ±10%. U112 removes dc offset to keep U113 in its monotonic range. (Both U112 and U113 are set to the same value.) The DAC settings cannot be changed from the front panel.

Track and Hold

Refer to function block AC of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Detector mode .... Sample
   Reference level .... −70 dBm
   Log dB/division .... 2 dB/DIV
   Sweep time .... 50 ms

2. Disconnect any signal from the spectrum analyzer input. A full scale display of sampled noise should be present.

3. Trigger an oscilloscope on the positive going edge of HHOLD (A3U506 pin 16).

4. The waveform at A3TP10 should be random noise with an average level of approximately 4 V. The noise should have a flat spot in its response while HHOLD is high, indicating proper operation of U114.

A3 Assembly ADC Circuits

The ADC consists of a 12-bit DAC, 12-bit successive approximation register (SAR), data multiplexers, and data latches. The ADC ASM (algorithmic state machine) controls the ADC. Eight inputs are controlled by the ADC MUX. These include a positive peak detector, negative peak detector, sampled video, scan ramp, YTO error voltage, FC MUX voltages, Cal Oscillator tune voltage, and offset lock error voltage. A MUX on the A14 frequency control assembly selects which voltage is sent to the ADC MUX on the FC MUX signal line.

During NORMAL detector mode sweeps, when noise is detected by the rosenfell detector, the ADC ASM automatically switches between POS PEAK and NEG PEAK.

ADC Control Signals

Refer to function blocks B and F of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC requires two signals from the A2 controller assembly: HBADC_CLK0 and HBBKT_PULSE. HBBKT_PULSE is used only in zero span. Use the following steps to verify the signals.

1. Disconnect W22 from A2J8.

2. If a 10 MHz TTL signal is absent on W22, refer to the 10 MHz Reference (on the A15 RF assembly) troubleshooting procedure in Chapter 12 , "RF Section."

3. Set the spectrum analyzer **SPAN** to zero.

4. Reconnect W22.

5. With an oscilloscope probe, monitor A3J401 pin 20.

6. If TTL pulses are absent, the A2 controller assembly is faulty. Refer to Chapter 10 , "Controller Section." The presence of TTL pulses indicates a faulty A3 assembly.

7. Monitor A3J401 pin 23 (HBADC_CLK0). If a 1 MHz TTL clock signal is present, HBADC_CLK0 is working properly.

8. If HBKT_PULSE or HBADC_CLK0 is missing, disconnect A3W1 from A2J2.

9. Monitor A2U5 pin 3 for HBKT_PULSE and A2U5 pin 7 for HBADC_CLK0.

10. If HBADC_CLK0 is absent, troubleshoot the A2 controller assembly.

11. HBKT_PULSE is absent, refer to the information on troubleshooting the frequency counter in Chapter 10 , "Controller Section."

12. Reconnect A3W1 to A2J2.

ADC Start/Stop Control

Refer to function block B of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC Start/Stop Control determines the start time of all ADC conversions. Multiplexer A3U509 chooses the source of the start signal. Both HSTART_SRC and HBUCKET tell the ASM to start a conversion.

1. Press **PRESET** on the spectrum analyzer and set the following controls:

   Span .... 0 Hz
   Sweep time .... 60 s
   Detector mode .... SAMPLE

2. Check for a TTL high at A3U509 pin 2 and a TTL low at A3U509 pin 14.

3. Set the detector mode to NORMAL.

4. Check that A3U509 pins 2 and 14 are both TTL low.

5. Set the spectrum analyzer to the following settings:

   Span .... 1 MHz
   Detector mode .... SAMPLE

6. Check for a TTL high at A3U509 pin 2 and a TTL low at A3U509 pin 14.

7. Press **CAL** and **REALIGN LO &IF**. During the realignment, A3U509 pin 2 should be TTL low and pin 14 should be TTL high until the 10 kHz and narrower resolution bandwidths are adjusted. If correct, the Start/Stop Control circuitry is being selected properly by the processor and U508 in the ADC Register block is working properly.

8. Press **PRESET** on the spectrum analyzer and set the controls as follows:

   Span .... 0 Hz
   Detector mode .... SAMPLE
   Sweep time .... 400 ms

9. Check that A3U509 pin 7 has positive 15 μs pulses with a 667 μs period (sweep time/600). Check that A3U509 pin 9 has positive 15 μs pulses with a 667 μs period (sweep time/600). The pulses should be present during the sweep but absent during retrace.

10. Set the detector mode to NORMAL.

11. Check that A3U509 pin 9 has pulses every 130 μs and U509 pin 7 has pulses every 667 μs (although pulse widths may be changing).

ADC ASM

Refer to function block F of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

   Span .... 0 Hz
   Sweep time .... 60 s
   Detector mode .... SAMPLE

2. Check that HSTART_SRC (U504 pin 4) goes TTL high, causing HHOLD (U506 pin 16) to go high 15 μs later.

3. Check that HSTART_ADC (U506 pin 15) goes TTL high 19 μs after HSTART_SRC goes high.

4. HHOLD should stay TTL high for approximately 18 μs, and HSTART_ADC should stay high for approximately 31 μs.

5. Check that LCMPLT (U504 pin 15) goes TTL low 12 μs after HSTART_ADC goes high (12 bits at 1 μs per bit). LCMPLT indicates that the successive approximation state machine (SASM) has completed the ADC conversion.

6. Check that LDONE (U506 pin 19) goes TTL low approximately 2 μs after LCMPLT goes low.

ADC

Refer to function block A of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The successive approximation state machine (SASM) consists of A3U527 and A3U528. Upon the occurrence of HSTART_ADC, the SASM successively toggles bits from high to low starting with the most significant bit. The digital result is then converted to an analog current in DAC U518 and compared with the SAMPLED VIDEO. If the DAC current is too high, the output of U512 will be low, telling the SASM that the "guess" was high and that the bit just toggled should remain low. It then moves on to the next most significant bit until all 12 bits have been "guessed" at. Each "guess" takes 1 µs (one cycle of HBADC_CLK0), or 12 µs to complete a conversion. When the conversion is completed, the SASM sets LCMPLT low. The bits are written to the data bus by buffers U514 and U516.

1. Set the spectrum analyzer controls as follows:

   > Center frequency .... 300 MHz
   > Span .... 0 Hz
   > Sweep time .... 60 s
   > Detector mode .... SAMPLE

2. Trigger an oscilloscope on HSTART_ADC (U506 pin 15) and monitor the outputs of the SASM (U527 pins 18 and 19; U528 pins 14 through 23). Each bit should start high and be switched low. It will either stay low or return to a high state 1 µs later, depending on the comparison at U512.

3. If the outputs do not exhibit this bit pattern, and the ADC ASM checks are working properly, suspect A3U527, U528, or one of the latches (U514/516). If the output of comparator U512 does not toggle back and forth during a conversion, suspect either U512 or one of the clipping diodes (CR500/CR501).

NOTE   Because currents are being summed at U512 pins 2 and 3, voltage levels at these points are difficult to interpret.

Ramp Counter

Refer to function block D of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The ramp counter is used for sweeps with widths greater than 2.0 MHz times N. The analog sweep ramp is compared to the digital ramp counter. When the analog sweep ramp exceeds the DAC output generated for that ramp counter setting, HRAMP_COMP toggles high, indicating the end of a bucket. The ramp counter counts horizontal buckets. There are 601 buckets per sweep, so the ramp (bucket) counter counts from 0 to 600. The ramp counter is incremented by HRST_PK_ENA.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

    Span .... 5 MHz
    Detector mode .... SAMPLE

2. For spans greater than 2.0 MHz times N0, HODD (A3U525 pin 3) is a square wave with a period defined by ($2 \times$ sweep time/600). For example, for a 6 s sweep time, HODD has a period of 20 ms. The ramp (bucket) counter will be odd every other bucket.

A3 Assembly Control Circuits

A digital control problem will cause the following three steps to fail.

1. On the spectrum analyzer, press **AMPLITUDE**, **ATTEN MAN**, 7, 0, and **dB**.

2. A click should be heard after pressing dB in step 1, unless ATTEN was previously set to 70 dB.

3. Press 1, 0, and **dB**. Another click should be heard. If no clicks were heard, but the ATTEN value displayed on the CRT changed, the digital control signals are not operating properly.

Analog Bus Drivers

Refer to function block N of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the spectrum analyzer, and set the controls as follows:

   Span .... 0 Hz
   Trigger .... Single

2. Monitor A3U401 pin 3 (LRF_STB) with an oscilloscope or logic probe. This is the strobe for the A15 RF Assembly.

3. Press **AUX CTRL** and **REAR PANEL** and check that pulses occur when toggling between **10 MHz INT** and **10 MHz EXT**.

4. Monitor U401 pin 5 (LFC_STB) with an oscilloscope or logic probe. This is the strobe for the A14 frequency control assembly.

5. Press **AMPLITUDE** and check that pulses occur when toggling between **ATTEN** settings of 10 and 20 dB.

6. Monitor U401 pin 7 (LIF_STB) with an oscilloscope or logic probe. This is the strobe for the A5 IF assembly.

7. Press **AMPLITUDE** and check that pulses occur when toggling between **REF LVL** settings of −10 dBm and −20 dBm.

8. Monitor U401 pin 9 (LLOG_STB) with an oscilloscope or logic probe. This is the strobe for the log amplifier on the A4 assembly.

9. Press **AMPLITUDE** and check that pulses occur when toggling between **LINEAR** and **LOG dB/DIV**.

10. To check the Address and Data Lines, place a jumper from A3TP1 and A3TP2 to A3U406 pin 20 (+5 V).

11. Check that address lines A0 through A7 and data lines D0 through D7 are all TTL high.

12. If any address or data line is low, press **LINE** to turn spectrum analyzer off and disconnect the W2 control cable from A3J2. Press **LINE** to turn spectrum analyzer on. Ignore any error messages.

13. Check that address lines A0 through A7 and data lines D0 through D7 are all high. If all address and data lines are high, suspect a fault either in W2 or one of the other four assemblies which connect to W2.

14. If any address or data line is low, check the appropriate input of either U405 (data lines) or U406 (address lines).

15. If a data line input is stuck low, check the data bus buffer. If an address line input is stuck low, check A3W1 and the A2 controller assembly.

16. If the appropriate input is high or toggling between high and low, suspect a failure in either U405 (data lines) or U406 (address lines).

17. Remove jumpers.

Analog Bus Timing

Refer to function block P of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Analog bus timing (ABT) generates the strobes for the A4, A5, A14, and A15 assemblies. The A14 frequency control assembly also requires a qualifier for its strobe, LVFC_ENABLE. A3U400 and A3U414 provide a 2 μs delay between the time HANA_BUS goes high and the enable line to demultiplexer A3U407 goes low.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

   Center frequency .... 300 MHz
   Span .... 100 MHz

2. Check that A3U407 pin 1 goes low approximately 2 μs after HANA_BUS (A3U400 pin 3) goes high.

3. If HANA_BUS is absent, check for pulses on ABT A3U505 pin 2 and IA10 (A3U505 pin 5).

4. If A3U407 pin 1 is not delayed 2 μs from HANA_BUS, check for the presence of the 1 MHz HBADC_CLK0.

5. If A3U407 pin 1 is not delayed 2 μs from HANA_BUS and HBADC_CLK0 is correct, suspect a fault in either A3U414 or A3U400.

6. Press **PRESET** and set the controls as follows:

    Span .... 0 Hz

    Trigger .... SINGLE

7. Monitor A3U401 pin 3 (LR_STB) with an oscilloscope or logic probe. This is the strobe for the A15 RF assembly.

8. Press **AUX CTRL** and **REAR PANEL** and check that pulses occur when toggling between **10 MHz INT** and **10 MHz EXT**.

9. Monitor A3U401 pin 5 (LF_STB) with an oscilloscope or logic probe. This is the strobe for the A14 frequency control assembly.

10. Press **AMPLITUDE** and check that pulses occur when toggling between **ATTEN** settings of 10 and 20 dB.

11. Monitor A3U401B pin 7 (LIF_STB) with an oscilloscope or logic probe. This is the strobe for the A5 IF assembly.

12. Press **AMPLITUDE** and check that pulses occur when toggling between **REF LVL** settings of −10 dBm and −20 dBm.

13. Monitor A3U401B pin 9 (LLOG_STB) with an oscilloscope or logic probe. This is the strobe for the A4 log amplifier/cal oscillator assembly.

14. Press **AMPLITUDE** and check that pulses occur when toggling between **LINEAR** and **LOG DB/DIV**.

Interface Strobe Select

Refer to function block K of A3 Interface Assembly Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Interface strobe select generates the various strobes used by circuits on the A3 Interface Assembly. Table 8-10 on page 413 and Table 8-11 on page 413 are the truth tables for demultiplexers A3U410 and A3U500.

Table 8-10   **Demultiplexer A3U410 Truth Table**

Selected Output Line	IA1	IA2	IA3
Pin 15, LSCAN_KBD	L	L	L
Pin 14, LDACU1	H	L	L
Pin 13, LDAC1	L	H	L
Pin 12, LDAC2	H	H	L
Pin 11, LDAC3	L	L	H
Pin 10	H	L	H
Pin 9, LTIMER	L	H	H
Pin 7, LADC_REG1	H	H	H

Table 8-11   **Demultiplexer A3U500 Truth Table**

Selected Output Line	IA0	IA1	IA2
Pin 15, LSENSE_KBD	L	L	L
Pin 14, LINT_PRIOR	H	L	L
Pin 13, LADC_DATA1	L	H	L
Pin 12, LDAC_DATA0	H	H	L
Pin 11, HCNTR_LD0	L	L	H
Pin 10, HCNTR_LD1	H	L	H
Pin 9, LRPG_RD	L	H	H
Pin 7, LADC_REG0	H	H	H

A16 Assembly Fast ADC Circuits (8562E with Option 007)

The fast ADC consists of video signal scaling and limiting amplifiers, an 8-bit flash ADC, peak/pit detection of the digitized video signal, a 32 K-byte RAM, and the fast ADC control circuitry.

Video Input Scaling Amplifiers and Limiter

Refer to function block L of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information.*

The video input scaling amplifiers help provide scaling (10 dB/div, 5 dB/div, 2 dB/div, or 1 dB/div) and buffer the flash video output. When the GAINX2 control line is low, switch U44D is open and switch U44C is closed. Thus, the scaled video at TP26 virtually follows the video input (0 - 1 V). When the GAINX2 control line is high, switch U44C is open and switch U44D is closed. Amplifier U43 then provides a gain of $2(V_{in}) -1$ V. Voltage clamp CR4 prevents the scaled video input to amplifier U45 from going more negative than –0.35 V or more positive than +1.25 V.

NOTE
When measuring voltages or waveforms on the A16 fast ADC assembly, connect the ground (or common) lead to the ground-plane trace on the A16 assembly. This digital ground plane is totally isolated from the chassis.

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1. Press **PRESET** on the Option 007 spectrum analyzer and set the controls as follows:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Reference level .... –10 dBm
   Log/division .... 10 dB/DIV
   Sweep time .... 20 ms

2. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Adjust the Option 007 spectrum analyzer reference level to place the signal at the top graticule line on the CRT display.

4. Measure the dc level at TP25. If the voltage measured is not +1.0 ±0.15 V, troubleshoot the A3 interface assembly.

5. Measure the dc level at TP26. The level should be approximately the same as the level measured at TP25. If not, suspect switch U44.

6. Set the Option 007 spectrum analyzer scale to 5dB per division.

7. Adjust the Option 007 spectrum analyzer reference level to place the signal at the top graticule line on the CRT display.

8. Measure the dc level at TP25 and TP26. The level should be +1.0 ±0.25 V. If the level measured at TP26 differs from the level measured at TP25 by more than 0.25 volts, troubleshoot U43 and associated circuitry.

9. Disconnect the CAL OUTPUT signal from the INPUT 50Ω connector.

10. The level at TP26 should drop to −0.35 Vdc. If the level is less (more negative) than −0.35 Vdc, replace voltage clamp CR4.

11. Measure the dc level of the flash video at TP27. The level should be near 0 Vdc with the signal at the bottom graticule line (no input to the spectrum analyzer).

12. Connect the CAL OUTPUT to the INPUT 50Ω connector.

13. Measure the dc level of the flash video at TP27. The level should be near +1.7 Vdc.

8-Bit Flash ADC

Refer to function block I of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The flash ADC (U35) converts the analog video signal into 8-bit digital values at a fixed rate of 12 megasamples per second.

NOTE   When measuring voltages or waveforms on the A16 fast ADC assembly, connect the ground (or common) lead to the ground-plane trace on the A16 assembly. This digital ground plane is totally isolated from the chassis.

---

1. Press **PRESET** on the Option 007 spectrum analyzer and set the controls as follows:

Center frequency	300 MHz
Span	0 Hz
Reference level	−20 dBm
Log/division	5 dB/DIV
Sweep time	20 ms

2. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Pins 4 through 10 (ADC7-ADC1) and pin 21 (ADC0) of U35 should all be high (logic 1), corresponding to an ADC digital count of 255 for the analog input of +2 volts or greater.

4. Disconnect the CAL OUTPUT signal from the INPUT 50Ω connector.

5. Pins 4 through 10 (ADC7-ADC1) and pin 21 (ADC0) of U35 should all be low (logic 0), corresponding to an ADC digital count of zero for the analog input of 0 volts or less.

Peak/Pit Detection

Refer to function block J of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Peak detection or pit (negative peak) detection can be enabled whenever the sample rate is less than 12 MHz (sweep times greater than 50 μs). Peak detection uses the maximum value of all the samples taken within each bucket (between adjacent display points). Pit detection uses the minimum value of all the samples taken within each bucket. And sample detection uses the last sample of all the samples taken within each bucket.

The different detection modes are implemented by selectively clocking latch U30, depending on the state of LP/Q which is generated in PAL U1 (block A). When LP/Q is low, U30 is clocked by WCLK. When LP/Q is high, U30 is not clocked. LP/Q is a function of the 12M_SEL, SCLK-1, LSAMPLE, LPEAK, P_LO, and P_HI signals. See Table 8-12 on page 417.

If the sample rate is 12 MHz, 12M_SEL is high, which forces LP/Q low so that every sample is clocked into latch U30 and latched into RAM U32 (block K). If the sample rate is less than 12 MHz and the detection mode is peak or pit, the SCLK-1, LPEAK, P_LO, and P_HI signals control the LP/Q signal. In these detection modes, latch U30 stores the peak or pit value of the samples taken for each bucket. The 8-bit digital magnitude comparator, U31, compares the input byte (P) with the output byte (Q) from latch U30. When P is greater than Q, P_LO is low (0) and P_HI is high (1). When P is less than Q, P_LO is high (1) and P_HI is low (0). When P is equal to Q, P_LO and P_HI are both low (0). See Table 8-12 on page 417.

Table 8-12   **LP/Q Truth Table**

Mode	LP/Q	12M_SEL	SCLK-1	LSAMPLE	LPEAK	P_LO	P_HI
12MHz	L	H	X	X	X	X	X
SAMPLE	L	X	X	L	X	X	X
POS PEAK	L H H	L L L	L L L	H H H	L L L	L H L	H L L
NEG PEAK (Pit)	H L H	L L L	L L L	H H H	H H H	L H L	H L L
Clocking Peak/Pit Sample	L	L	H	H	X	X	X

32 K-Byte Static RAM

Refer to function block K of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The static RAM stores the flash ADC samples that are taken when the fast ADC circuitry is in the "write" mode. When not in the "write" mode, the static RAM is read by the CPU on the A2 controller assembly to retrieve the fast ADC data.

The 8-bit Q bus connects the outputs of latch U30 to the data port of static RAM U32.

A16 Assembly Fast ADC Control Circuits (8562E with Option 007)

The fast ADC control circuits consist of the CPU interface and control registers, the reference clock, a clock and sample rate generator, a trigger circuit, a 16-bit post-trigger counter, a 15-bit circular address counter, a video trigger comparator, and the reference and power supply circuits.

CPU Interface and Control Registers

Refer to function block A of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The A16 assembly digital interface to the A2 controller assembly consists of an 8-bit bi-directional data bus, one address line, a most-significant byte strobe, and a least-significant byte strobe.

The A16 fast ADC assembly can be accessed by firmware (on the A2 controller assembly) at two logical addresses. When the address line (ADDR3) is low, the primary address is selected. When the ADDR3 is high, the secondary address is selected. The data transfers between the A16 fast ADC assembly and the A2 controller assembly are clocked by the two strobe lines, MSB_STRB and LSB_STRB. 16-bit word transfers occur as two sequential byte transfers; the most-significant byte first, followed by the least-significant byte. The primary address (ADDR3 low) contains the 16-bit control word written by the firmware on the A2 controller assembly. The secondary address (ADDR3 high) supports both 8-bit byte and 16-bit word reads and writes. There is no read/write line on the A16 fast ADC assembly to control the direction of data transfer. The fast ADC is preconfigured to read or write by setting the appropriate bits in the 16-bit control word. Refer to Table 8-13 on page 419. If the control word is not correct, it may result in a bus conflict.

Table 8-13   Control Word at Primary Address (U3 and U4)

Bit	Mnemonic	State	Description
Bit 0	WRITE		Allows samples to be written to FADC memory.
		1	All on-board clocks running and samples being written to FADC memory. (FADC memory cannot be read by A2 controller in this mode.)
		0	All on-board clocks turned off and no samples being written to FADC memory. (FADC memory can be read by A2 controller.)
Bit 1	ARM		Arms the FADC assembly for a trigger.
		1	FADC assembly armed to accept trigger from HSWP line or video trigger.
		0	FADC assembly cannot be triggered.
Bit 2	GAINX2		Turns on X2 log expand amplifier.
		1	A16U43 turned on. (5 dB/div or 1 dB/div scale)
		0	A16U43 turned off. (10 dB/div, 2 dB/div, or linear scale)
Bit 3	VTRIG_POL		Controls digital video trigger polarity.
		1	Negative-edge video trigger.
		0	Positive-edge video trigger.
Bit 4	LSAMPLE		Enables sample detection mode.
		1	Sample detection mode disabled.
		0	Sample detection mode enabled.
Bit 5	LADCEN		Enables FADC memory for "writes". (Toggled in conjunction with bit 0.)
		1	Disables FADC memory for "writes."
		0	Enables FADC memory for "writes."
Bit 6	LLOADADDR		Enables load address counter.
		1	"Writes" to the address counter disabled.
		0	"Writes" to the address counter enabled.
Bit 7	LLOADPOST		Enables load post-trigger counter.
		1	"Writes" to the post-trigger counter disabled.
		0	"Writes" to the post-trigger counter enabled.
Bit 8	LVTRIG_EN		Enables digital video trigger on A16.
		1	Digital video trigger disabled.
		0	Digital video trigger enabled.

Table 8-13   **Control Word at Primary Address (U3 and U4)**

Bit	Mnemonic	State	Description
Bit 9	LREADCLK		Clocks counters during "read" mode. Used to load post-trigger counter or address counter. Also used to post-increment address counter following memory "reads."
		1	Read clock disabled.
		0	Read clock enabled.
Bit 10	LREADMEM		Enables read FADC memory.
		1	Read FADC memory disabled.
		0	Read FADC memory enabled.
Bit 11	LREADADDR		Enables read trigger address latch.
		1	"Reads" from trigger address latch disabled.
		0	"Reads" from trigger address latch enabled.
Bit 12	LRATELATCH		Enables load sample rate latch.
		1	"Writes" to the sample rate latch are disabled.
		0	"Writes" to the sample rate latch are enabled.
Bit 13	LRLSHSWP		Releases HSWP strobe.
		1	Release HSWP strobe disabled.
		0	Release HSWP strobe enabled.
Bit 14	LLOADTRIG		Enables load video trigger level.
		1	Load digital video trigger level disabled.
		0	Load digital video trigger level enabled.
Bit 15	LPEAK		Peak/pit detection mode control.
		1	Enables pit (negative-peak) detection mode if LSAMPLE (Bit 4) is also high.
		0	Enables peak detection mode if LSAMPLE (Bit 4) is high.

Reference Clock

Refer to function block B of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The reference clock circuitry takes the 8 MHz CMOS square wave clock from the A2 controller assembly (via W59, coax 839) and triples the frequency to 24 MHz. Inverters U5A and U5B provide the proper match for the 8 MHz clock input, and also the desired drive level into the 24 MHz bandpass filter. The 24 MHz bandpass filter consists of R5, C8, L1, C9, C10, L2, C11, L3, C12, L4, C13, C14, and R6. Inverters U6A and U6B provide amplification of the 24 MHz clock to produce CMOS levels, and also buffer the 24 MHz clock output.

Clock and Sample Rate Generator

Refer to function block C of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The clock and sample rate generator takes the 24 MHz reference clock signal and generates all of the various clock signals used on the A16 fast ADC assembly. The sample rate generator consists of CMOS latch U15, CMOS counters U14 and U16, and CMOS flip-flops U7B and U9A. The sample rate generator only controls the rate at which the static RAM address counter (15-bit circular address counter) and the 16-bit post-trigger counter are clocked (ACLK and PCLK respectively). The sample rate generator also controls the number of flash ADC samples taken per bucket. The range of the sample rate is 1 sample per bucket (12 MHz rate) to 256 samples per bucket (less than 12 MHz rate). SCLK-1 is an input to PAL U1 (block A) and affects the LP/Q signal to ensure that the first sample of a bucket is always clocked into latch U30 (block J) and written into static RAM U32 (block K) when the detection mode is peak or pit and the sample rate is less than 12 MHz. Refer to Table 8-12 on page 417, LP/Q Truth Table in this chapter.

Trigger

Refer to function block D of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

When the A16 fast ADC is triggered, the current static RAM address is latched into trigger address latches U27 and U28 (block G), and the post-trigger counter (U19, U20, U21, U22, and U47) begins counting. Samples continue to be written to consecutive addresses in RAM U32 until the post-trigger counter reaches its terminal count. The CPU on the A2 controller assembly monitors the HSWP line and starts a software timer when HSWP goes high after being triggered. The software timer is set to slightly longer than the post-trigger counter will be counting, so at the end of the "time-out," the post-trigger counter has already reached its terminal count. At the end of this "time-out," the CPU on the A2 controller assembly takes the fast ADC out of "write" mode and reads latches U27 and U28 to determine the static RAM address of the sample that was taken when the trigger occurred. The CPU then writes the trigger address (read at U27/U28) to the fast ADC static RAM address counter (15-bit circular address counter). If pre-trigger or post-trigger (delay) is being used, the CPU adds or subtracts appropriately and writes the "adjusted" trigger address to the static RAM counter. The CPU then begins reading the fast ADC data, starting from the trigger (or offset trigger) address.

The trigger circuitry is enabled by the ARM signal (bit 1 of the fast ADC control word). Once a trigger occurs, the fast ADC cannot be triggered again until the ARM line goes low (disarmed), then high again (armed).

The fast ADC is triggered by the HSWP line in **FREE RUN**, **LINE**, and **EXTERNAL** trigger modes. When **VIDEO** trigger is being used, a synchronous digital video trigger signal, VCLK, is generated by PAL U1 (block A) and U17A (block D).

16-Bit Post-Trigger Counter

Refer to function block E of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*. The 16-bit post-trigger counter controls the number of static RAM memory locations that will be written after the trigger occurs. This counter consists of U19, U20, U21, U22, and U47. The counter is loaded from the CPU on the A2 controller assembly when the A16 fast ADC assembly is in "read" mode. The CPU loads the counter by first setting the LLOADPOST (bit 7 of the fast ADC control word) and the LREADCLK (bit 9 of the fast ADC control word) to their low state. The CPU then writes the 16-bit word to the fast ADC secondary address. The rising edge of PCLK then latches the 16-bit data into the post-trigger counter.

The post-trigger counter begins counting upward in "write" mode on the first rising edge of PCLK after the LCOUNT signal from the trigger circuit goes low. The frequency of PCLK is the programmed sample rate. When the post-trigger counter reaches its terminal count, the LSTOP signal goes low and disables the static RAM address counter from further counting. LSTOP also forces LCOUNT high in NAND gate U11D, which disables the post-trigger counter.

15-Bit (32 K) Circular Address Counter

Refer to function block G of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

This 15-bit programmable circular counter provides the address lines of the static RAM (U32). The counter consists of U23, U24, U25, and U26. It counts upward from 0 to 32767 and then back to 0 in a circular fashion. When a trigger occurs, latches U27 and U28 latch the current static RAM address so that the CPU on the A2 controller assembly can later read the latches and determine the static RAM address of the sample that was taken when the trigger occurred.

The CPU loads the address counter during "read" mode by first setting LLOADADDR (bit 6 of the fast ADC control word) and LREADCLK (bit 9 of the fast ADC control word) to their low state. The CPU then writes the 16-bit load value to the CPU secondary address. The rising edge of ACLK then latches the 16-bit data into the address counter.

After the address counter is loaded by the CPU during "read" mode, the static RAM is read by the CPU. The RAM is read by first setting LREADMEM (bit 10 of the fast ADC control word) and LREADCLK (bit 9 of the fast ADC control word) to their low state. Since the LREADCLK control bit is low, a negative-going pulse on the ACLK line will occur on every static RAM "read" by the CPU. This causes the address counter to increment at the end of each static RAM "read" so that the address counter automatically post-increments to the next address of RAM U32. In order for this address post-increment to occur, the LSTOP count enable signal from the post-trigger counter must be high. LSTOP goes low when the post-trigger counter reaches its terminal count in the "write" mode to stop the address counter from counting. When the fast ADC assembly is changed from "write" mode to "read" mode, LSTOP will be low. So the CPU on the A2 controller board must always first program the post-trigger counter to a value other than the terminal count (65535) to force LSTOP high.

Video Trigger Comparator

Refer to function block M of the A16 fast ADC assembly schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

This 8-bit digital magnitude comparator, U34, compares the digitized samples from the flash ADC (latch U29 output) to the programmed video trigger level. The video trigger level value on IOB2 through IOB7 is latched into the P input (top portion of U34) by the firmware on the A2 controller assembly when the fast ADC is in "read" mode. When the sample on the Q input is higher than the video trigger level on the P input, V_HI output is high, and V_LO output is low. When the Q input is lower than the P input, V_HI output is low and V_LO output is high. And when P is equal to Q, both V_HI and V_LO are low. These two signals (V_HI and V_LO) go to PAL U1 (block A) and are used to clock the video trigger generator (block D).

FIGURE 8-2. A3 INTERFACE ASSEMBLY BLOCK DIAGRAM

s1110c

FAST ADC (OPTION 007)
BLOCK DIAGRAM

P/O A3 INTERFACE ASSEMBLY

A16 FAST ADC (OPTION 007)

FROM
A2J15   839   W59
                  D

(T) VIDEO BUFFER
J105 MS1   J105 MS2
    X1
J102 VIDEO OUT
TO REAR PANEL

(V) VIDEO FILTER
TP15
VIDEO GATE
VIDEO ENABLE FROM SHEET 3. (H)

(Y) POSITIVE PEAK DETECTOR
TP16
TP17

J3   8 MHz TTL

(B) REF CLOCK (24 MHz)

J101
VIDEO INPUT
TP9
J105 MS3
(U) VIDEO MUX
TP14
ANALOG BUS

(W) VIDEO FILTER BUFFER AMP
J105 MS5
X1
J103
0-SPAN VIDEO
TP17
VIDEO TRIG

(X) LOG EXPAND
X5
.8V

(Z) NEGATIVE PEAK DETECTOR
TP17
TP18

LNEG_RESET

(A) CPU INTERFACE AND CONTROL REGISTERS
(C) CLOCK AND SAMPLE RATE GENERATOR
(D) TRIGGER
(E) 16-BIT POST-TRIGGER COUNTER
IOB0-IOB15
(G) 15-BIT (32K) CIRCULAR ADDRESS COUNTER AND LATCH

3
HSWP
TIMING AND   CONTROL BUS

W20   J4
6   VIDEO INPUT 0-1V
A

(L) VIDEO INPUT SCALING AMPLIFIERS AND LIMITER
FLASH VIDEO
(I) 8-BIT FLASH ADC
ADC0-ADC7
(J) PEAK/PIT DETECTION
(K) 32K RAM
IOB0-IOB7
A0-A14
MEMORY ADDRESS BUS

P2-P7
Q0-Q7

FROM A2J3   W7   20   10   J1   10
                         10   J2   2   2   4
(F) POWER SUPPLIES
D

4
4
4

(M) VIDEO TRIGGER COMPARATOR
IOB2-IOB7

IO0-IO7
(PLUS 2 DIGITAL GROUNDS)

IOB0-IOB15
IOB2-IOB7
IOB DATA BUS

si137e

FIGURE 8-3. FAST ADC (OPTION 007) BLOCK DIAGRAM

9   IF Section

Introduction

The IF Section contains the A4 log amplifier/cal oscillator and A5 IF assemblies.

NOTE

Because the cal oscillator circuitry on the A4 assembly is such an integral part of the IF adjustment, always check this assembly first, before checking the rest of the IF Section. A faulty cal oscillator can cause many apparent "faults" in the rest of the IF Section.

Troubleshooting Using the TAM

Refer to Chapter 7 , "General Troubleshooting," for information on enabling the TAM for use with the 8562E/EC spectrum analyzer.

When using Automatic Fault Isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 9-1 on page 433 to locate the manual procedure. Table 9-2 on page 434 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 9-1 on page 432 illustrates the location of A4 and A5 test connectors. Figure 9-2 on page 436 illustrates the levels and paths through the IF Section.

Figure 9-1   A4 and A5 Test Connectors
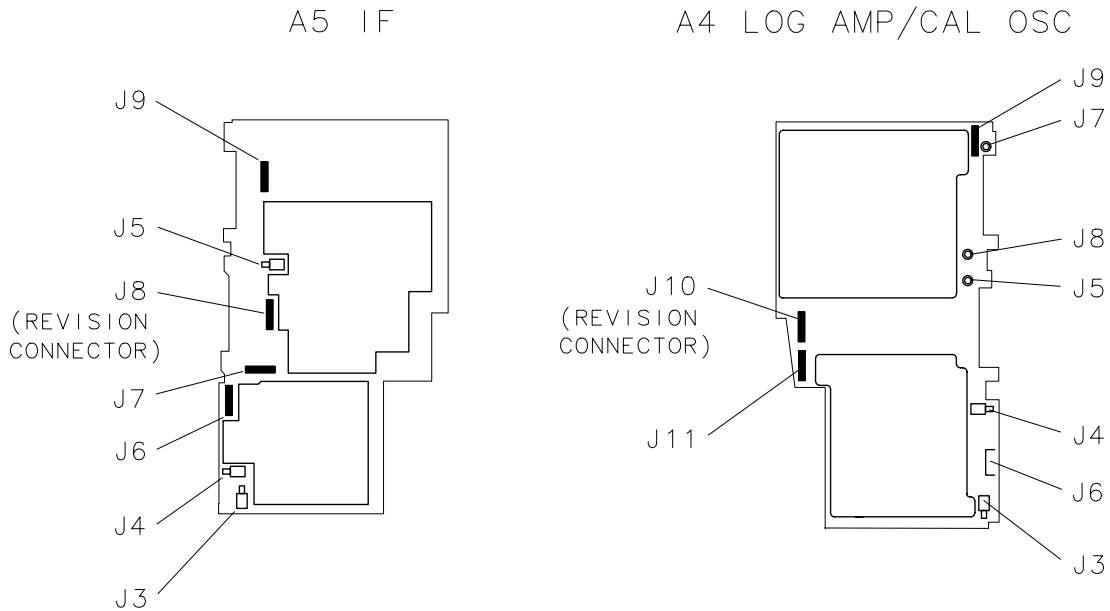
Table 9-1   **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check Cal Oscillator on A4 Assembly	Troubleshooting the Cal Osc with the TAM
Check Input Switch on A5 IF Assembly	Troubleshooting A5 with the TAM
Check Linear Amplifiers on A4 Assembly	Linear Amplifiers
Check Log Expand on A3 Interface Assembly	Refer to "Log Expand" in this chapter
Check Step Gains on A5 IF Assembly	Step Gains
Check Video Offsets on A4 Assembly	Video Offset *(steps 1 through 4)*
Check VIDEO OUT on A4 Assembly	Video Output

Troubleshooting the Log Amplifier with the TAM

Manual probe troubleshooting tests several dc bias points and signal path voltages. A dc bias is measured in the limiter and a fault here indicates a broken limiter stage. Signal path voltages are measured at the input, after the video amplifier in the linear path, after the offset and gain compensation circuits in the log path, and after the video offset.

The cal oscillator on A4 is used as an input to the log amp for the purpose of measuring gains. Faults in the signal path voltages indicate broken circuitry in prior stages. This technique locates dead stages, but might not report slightly degraded ones. Both +15 V and –15 V are measured. The revision code is on J11.

Troubleshooting A5 with the TAM

Manual Probe Troubleshooting calculates stage bias-currents which test the operation of the IF chain. (This technique locates dead stages, but might not report slightly degraded ones.) DACs that are monitored are listed below:

```
IFDAC1 ....................................................................... A5U812
IFDAC2 ....................................................................... A5U813
IFDAC3 ....................................................................... A5U809
IFDAC4 ........................................................................ A5U807
IFDAC5 ....................................................................... A5U810
IFDAC6 ....................................................................... A5U806
```

Table 9-2   **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A3J105	Video Input to Interface	MS1
	Video to Rear Panel	MS2
	Video MUX	MS3
	Log Offset/Log Expand	MS1,MS3
	Video Filter Buffer Amplifier	MS3, MS5, OS1
	Video Peak Detectors	MS5, MS6
	ADC MUX	MS6
	Variable Gain Amplifier	MS6, MS7
	Track and Hold	MS7, MS8
A3J400	Video Trigger DAC	MS1
	Revision	MS2
	Real Time DAC #1	MS3
	RF Gain DACs	MS6
	ADC Start/Stop Control	MS7
	Trigger	MS8
A4J9	Cal Osc Sweep Gen Hardware	MS1, MS2
	Cal Osc Tune Line Test	MS3
	Cal Osc ALC Test	MS4
	Cal Osc Sweep Gen Output	MS6
A4J10	Log Amp Input Switch	MS1
	Log Amp Limiter Bias	MS2
	Positive 15 V Supply	MS5
A4J11	Logamp Linear Output	MS2
	Logamp Linear MUX Path	MS2,MS3,MS8
	Logamp Log Output	MS3
	Logamp Compensation	MS3,MS4
	Logamp Log MUX Path	MS4,MS8
	Logamp Video Offset	MS8

Table 9-2   **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A4J11(Cont.)	−15 V Supply	MS7
	Revision	MS5
A5J6	1st Step Gain Stage 1	MS1, MS2, MS8
	1st Step Gain Stage 2	MS1, MS2, MS3
	1st XTAL Pole Stage	MS2, MS3, MS4
	2nd XTAL Pole Stage	MS3, MS4, MS5
	1st LC Pole Stage 1	MS4, MS5, MS6
	1st LC Pole Stage 2	MS5, MS6, MS7
A5J7	Ref 15 dB Attenuator Stage	MS1, MS2, MS3
	2nd Step Gain Stage	MS2, MS3, MS4
	2nd/3rd Step Gain Stage	MS3, MS4, MS5
	3rd Step Gain Stage	MS4, MS5, MS6
	Fine Atten/3rd XTL Pole	MS5, MS6, MS7
	3rd XTAL Pole Stage	MS6, MS7, MS8
A5J8	Revision	MS8
	4th XTAL Pole Stage	MS1, MS2, MS3
	Post Amplifier Stage 1	MS2, MS3, MS4
	Post Amplifier Stage 3	MS3, MS4, MS5
	3rd LC Pole Stage	MS5, MS6, MS7
	4th LC Pole Stage	MS6, MS7
A5J9	IFDAC Channels `A'	MS1
	IFDAC Channels `B'	MS3
	IFDAC Channels `C'	MS4
	IFDAC Channels `D'	MS2
	Latched IF Control Lines	MS5
	Negative 15 V Supply	MS6
	5 V Supply	MS7
	10 V Reference	MS8

Figure 9-2   **IF Section Troubleshooting with the TAM**
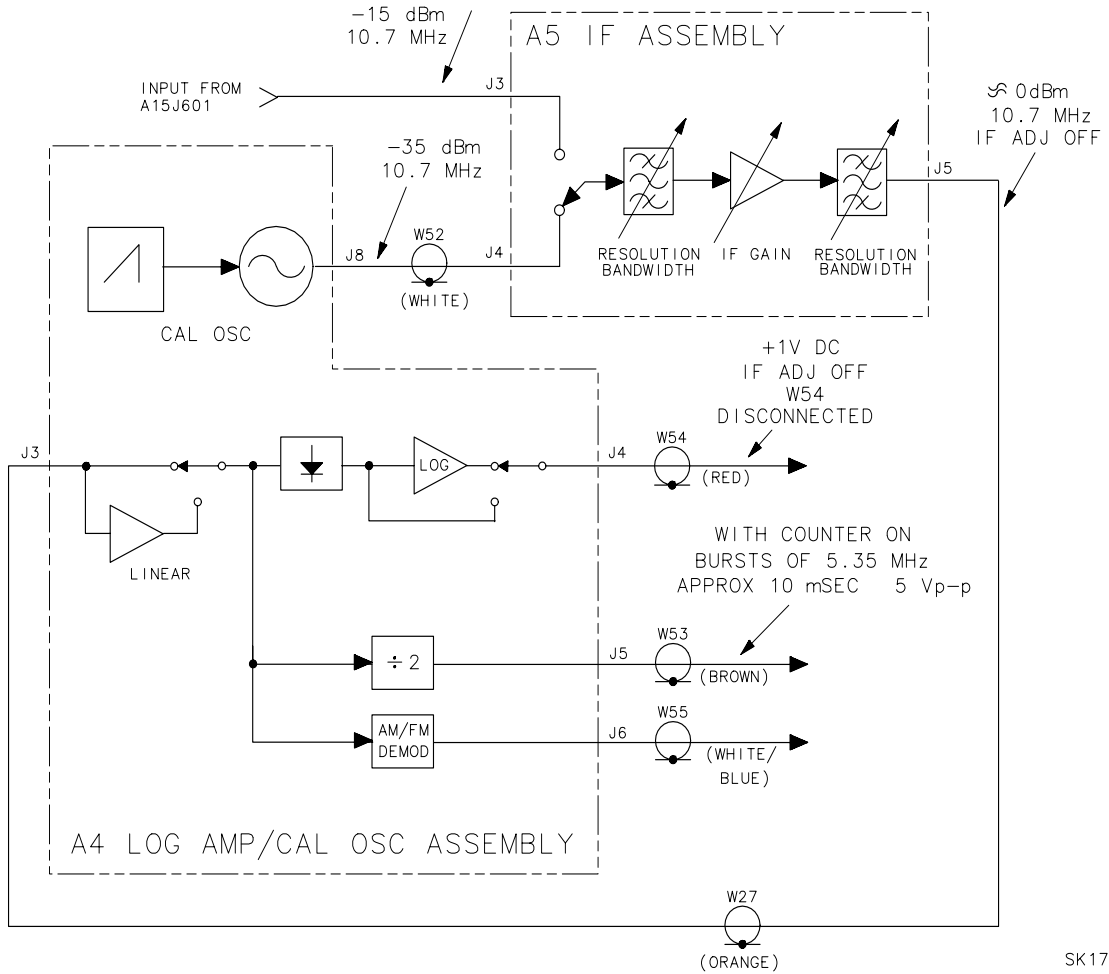
Both the digital control and DACs are multiplexed onto test point "channels" through resistive networks. One DAC from each of the quad-DAC packages feeds into a network. The TAM varies each DAC individually to isolate which ones failed. Similarly, 10 digitally-controlled lines feed into a network and are monitored by the TAM. The channels used to monitor the DACs are listed below:

Channel A .... A5J9 pin 1 (MS1)

Channel B .... A5J9 pin 3 (MS3)

Channel C .... A5J9 pin 4 (MS4)

Channel D .... A5J9 pin 2 (MS2)

1. On the 8562E/EC spectrum analyzer, press **PRESET**, **MODULE**, and **Diagnose**. Select **Cal Osc Troubleshooting Mode**.

2. On the 8562E/EC spectrum analyzer, disconnect W27 (coax 3) from A5J5 and monitor the output of A5J5 with a second spectrum analyzer.

3. Set the other spectrum analyzer controls as follows:

   Span .... 5 MHz
   Reference level .... −20 dBm
   Center frequency .... 10.7 MHz

4. On the 8562E/EC spectrum analyzer, set the cal oscillator to 10.7 MHz by selecting **Fixed Tuned to 10.7 MHz**.

5. A −25 dBm signal from A5J5 should be displayed. If the signal is missing, disconnect W52 (coax 9) from A5J4. This is the cal oscillator signal input from the cal oscillator on the A4 assembly.

6. Connect the end of cable W52 to the input of the second spectrum analyzer. The signal coming from cable W52 should be −35 dBm at 10.7 MHz. If the cal oscillator signal from cable W52 is correct, the A5 IF assembly is probably at fault.

Troubleshooting the Cal Oscillator with the TAM

1. Enter the TAM Cal Osc Troubleshooting Mode.

2. On the 8562E/EC spectrum analyzer, disconnect cable W52 (coax 9) from A5J4 and connect this end of cable W52 to the input of a second spectrum analyzer.

3. Set the controls of the second spectrum analyzer connected to cable W52 to the following:

   Span .... 5 MHz
   Reference level .... −30 dBm
   Center frequency .... 10.7 MHz

4. Select each of the fixed-tuned frequencies. Verify at each frequency that the signal amplitude measures −35 dBm. If the frequency is incorrect, do the following:

   a. Verify that the reference divider output (A4U811 pin 9) is 100 kHz. If it is not, verify that the 10 MHz reference is present at A4U811 pin 1.

   b. Verify that the frequency found on the output of the divider (A4U808 pin 15) matches the output of the reference divider. Matching frequencies indicate the oscillator loop is locked. If the loop is not locked, troubleshoot the divider, oscillator, or phase detector.

c. Verify that the frequency found at the divider input (A4U808 pin 3) matches the CW frequency chosen in step a. Matching frequencies indicate a properly working oscillator. If the frequency is different, troubleshoot the divider.

d. Repeat step c for all the CW frequencies provided by the test.

5. Select each of the sweep widths (these sweeps are centered about 10.7 MHz).

6. Reduce the span of the other spectrum analyzer to check that the cal oscillator is actually sweeping. If the oscillator is not sweeping, perform the following steps:

a. The output of the sweep generator circuit (A4U804 pin 8 of function block Z) should be a series of negative-going parabolas (frequency and amplitude vary depending on the sweep width chosen). Table 9-3 on page 438 lists the RANGE, MA0, and MA1 values for the sweep widths. If a failure is indicated in the IF/LOG CHECK, press **More Info** to provide more detailed information about the detected failure. If a GPIB printer is available, connect it to the 8562E/EC spectrum analyzer GPIB connector, then press **Print Page** for a hard-copy output.

Table 9-3   **Sweep Width Settings**

Sweep Width	Sweep Time	Res BW Adjusted	RANGE A4U105 Pin 6	MA1 A4U105 Pin 2	MA0 A4U105 Pin 5
20 kHz	5 ms	10 kHz	+5 V	0 V	0 V
10 kHz	10 ms	3 kHz	+5 V	0 V	+5 V
4 kHz	30 ms	1 kHz	+5 V	+5 V	0 V
2 kHz	15 ms	300 Hz	+5 V	+5 V	+5 V

Automatic IF Adjustment

The spectrum analyzer performs an automatic adjustment of the IF Section whenever needed.

The cal oscillator on the A4 assembly provides a stimulus signal which is routed through the IF during the retrace period.

The A3 Interface assembly measures the response using its analog-to-digital converter (ADC). The spectrum analyzer turns the cal oscillator off during a sweep.

When IF ADJ is ON, the spectrum analyzer readjusts part of the IF circuitry during each retrace period to readjust the IF completely every 5 minutes.

Automatic IF adjustment is performed upon the following conditions:

- Power on: (unless **STOP ALIGN** is pressed). The IF parameter variables are initialized to values loaded in program ROM and all possible IF adjustments are made. If **STOP ALIGN** is pressed, the adjustment is halted.

- If **REALIGN LO &IF** is selected: All possible IF adjustments (and LO adjustments) are made with the most recent IF parameter variables used as the starting point.

- If **FULL IF ADJ** is selected: All possible IF adjustments are made with the most recent IF parameter variables used as the starting point. (**FULL IF ADJ** is located in the **CAL** menu.)

- If **ADJ CURR IF STATE** is selected: All amplitude data and some resolution bandwidths are adjusted. The bandwidths adjusted are a function of the currently selected resolution bandwidth setting.

- Between sweeps: IF ADJ must be set to ON. When IF ADJ is OFF, an A is displayed along the left side of the graticule.

If a FULL IF ADJ sequence cannot proceed beyond the amplitude portion, check the output of the cal oscillator on the A4 board as follows:

1. Disconnect cable W52 (coax 9) from A5J4. Connect cable W52 to the input of a second spectrum analyzer.

2. Set the second spectrum analyzer center frequency to 10.7 MHz and the reference level to –30 dBm.

3. On the spectrum analyzer under test, press **FULL IF ADJ** and observe the display of the second spectrum analyzer.

4. If a –35 dBm signal does not appear, the cal oscillator is probably at fault.

Parameters Adjusted

The following IF parameters are adjusted in the sequence listed:

1. Amplitude

   a. Video Offsets: analog (using log amplifier video offset DAC) and digital (applying stored constant to all readings)

      1. Linear Scale Offset

      2. Log Scale Offset

         1. Wideband and Narrowband modes

         2. 0 to 60 dB range in 10 dB steps

         3. 10 dB/division and 2 dB/division (log expand) modes

   b. Step Gains (A5 IF Assembly)

      1. First Step Gain for 16 different DAC settings

      2. Second Step Gain for 16 different DAC settings

      3. Third Step Gain for 0, 15, and 30 dB attenuation relative to maximum gain

      4. Fine Attenuator for 32 evenly-spaced DAC settings

   c. Log Amplifier Slopes and Fidelity

      1. Wideband (RES BW 300 kHz through 2 MHz) and Narrowband modes (RES BW 300 Hz through 100 kHz)

      2. 10 dB/division and 2 dB/division (log expand) modes

   d. Linear Scale Gains - On the log amplifier assembly (P/O A4)

   e. Peak Detector Offsets (both positive and negative peak detectors with respect to normal sample path used by Auto IF Adjust)

2. LC Bandwidths

   a. 300 kHz resolution bandwidth center frequency, bandwidth, and gain

   b. 1 MHz resolution bandwidth center frequency, bandwidth, and gain

   c. 2 MHz resolution bandwidth gain

   d. 100 kHz resolution bandwidth center frequency, bandwidth, and gain

   e. 30 kHz resolution bandwidth center frequency, bandwidth, and gain

   f. Gain of all resolution bandwidth relative to the 300 kHz RES BW

3. Crystal Bandwidths

   a. The cal oscillator sweep rate is measured against the 100 kHz resolution bandwidth filter skirt. This result is used in compensating the sweeps used for adjusting the crystal bandwidths.

   b. 10 kHz resolution bandwidth

      1. Center frequency of LC tank that loads the crystal

      2. Symmetry adjustment to cancel crystal case capacitance

      3. Bandwidth

   c. 3 kHz resolution bandwidth: center frequency of LC tank and bandwidth of resolution bandwidth

   d. 1 kHz resolution bandwidth: bandwidth

   e. 300 Hz resolution bandwidth: bandwidth

   f. Gain of all resolution bandwidth relative to the 300 kHz RES BW

4. Digital Bandwidths (1 Hz through 100 Hz; 10 Hz through 100 Hz if Option 103)

   a. VCXO (final LO) tuned to align digital bandwidths with crystal bandwidth center frequency

   b. Overall gain

   c. Gain variation with input frequency

Requirements

For the Automatic IF Adjustment routine to work, the spectrum analyzer must provide the following basic functions:

- Power supplies

- Control signals

- ADC

- 10 MHz frequency reference to the A4 log amp/cal oscillator

- A15 RF assembly isolation from the RF signal during IF adjustment

A15 RF assembly isolation is a function of the REDIR signal in the A15 Flatness Compensation Control block.

The references against which the Automatic IF Adjustment routine aligns are:

- 10 MHz reference (A15)

- Linear scale fidelity, especially the 10 dB gain stage in A4 linear amplifier block

- 15 dB reference attenuator (A5)

- Cal Oscillator output power (A4)

Performance Test Failures

Failures in IF-Section-related performance tests may be investigated using the following information.

IF Gain Uncertainty Performance Test

Failure of this performance test indicates a possible problem with the spectrum analyzer IF gain circuits. Assuming no major IF problems causing IF adjustment errors, IF gain problems in the first 50 dB of IF gain (REF LVLs of 0 dBm to −50 dBm with 10 dB ATTEN) are a result of faults on the A5 IF Assembly. IF gain problems in the next 60 dB of IF gain (REF LVLs of −60 dBm to −110 dBm, 10 dB ATTEN) result from log amplifier faults on the A4 assembly.

A signal level of −5 dBm is required at input (A5J3) for displaying a signal at top screen with 10 dB input attenuation and a 0 dBm reference level.

Isolate IF gain problems on the log amplifier assembly (A4) with the following steps:

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, −50 dBm.

2. Press **CAL** and **IF ADJ OFF**.

3. Disconnect cable W27 (coax 3) from A5J5 and connect cable W27 to the output of a signal generator.

4. Set the signal generator controls as follows:

   Amplitude .... +10 dBm
   Frequency .... 10.7 MHz

5. Simultaneously decrease the signal generator output and the spectrum analyzer REF LVL in 10 dB steps. The signal displayed by the spectrum analyzer should remain at the reference level for each step. If the signal deviates from the reference level, troubleshoot the video offset circuitry on the A4 assembly.

6. Repeat steps 1 through 5 with the spectrum analyzer set to linear.

Scale Fidelity Performance Test

Failure of this performance test indicates a possible problem with the A4 assembly.

- If the Linear, 5 dB/div, or 10 dB/div scales are out of specification, the fault is most likely on the log amplifier assembly (P/O A4).

- If only the 1 dB/div or 2 dB/div scales are out of specification, the fault is most likely on the A3 interface assembly.

Resolution Bandwidths Performance Tests

Most resolution bandwidth problems are a result of A5 IF assembly failures. The resolution bandwidths are adjusted in the following sequence using 300 kHz as the reference: 1 MHz, 2 MHz, 100 kHz, 30 kHz, 10 kHz, 3 kHz, 1 kHz, 300 Hz, 100 Hz, 30 Hz, 10 Hz, 3 Hz, and 1 Hz. The 3 Hz and 1 Hz bandwidths are not available with Option 103.

If the IF adjustment routine encountered an error, the previously adjusted resolution bandwidths should be working properly and default DAC values are used for the remaining resolution bandwidth settings.

If the IF bandpass adjustments and the automatic IF adjustments fail to bring the resolution bandwidths within specification, troubleshoot the A5 IF assembly.

Log Amplifier (P/O A4 Assembly)

The log amplifier on the A4 assembly performs several functions. It provides log and linear paths converting the 10.7 MHz IF signal to video. In addition it also provides offset circuitry, AM/FM demodulator circuitry, a frequency counter output, and down conversion of the 10.7 MHz IF to 4.8 kHz for use by the digital IF.

The log amp results are realized by using a wide dynamic range linear detector followed by a video log amp. The detector is used for both linear and log paths and contains a mixer that acts as the down converter mixer for the digital IF.

CAUTION

For troubleshooting, it is recommended that you use an active probe, such as an 85024A, and another spectrum analyzer. If an 1120A active probe is being used with a spectrum analyzer having dc coupled inputs, such as the 8566A/B, 8569A/B and the 8562A/B, either set the active probe for an ac-coupled output or use a dc-blocking capacitor between the active probe and the spectrum analyzer input. Failure to do this can result in damage to the spectrum analyzer or the probe.

Log Amplifier

Refer to function blocks K, L, and AE of A4 Log Amplifier Schematic Diagram (sheets 3 of 4 and 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*. The log amplifier receives the detected video signal from the detector/mixer and outputs a voltage proportional to the log of the input voltage. The linear output is tapped off at the emitter of U501D. U507 provides input offset adjustment capability and adjusts the offset of the op amp formed by U501A, B, C, and D. Q502 is a buffer. Q501 switches in additional offset for digital RBWs. The logarithmic characteristic of the base-emitter junction of U502B is used in the feedback path to produce the logging affect. U502D is used to adjust for nonlinearities in the linear mode. R531 is used to adjust log fidelity at the top of the screen.

Use the following steps to verify proper operation of the log amplifier chain:

1. Press **CAL** and **IF ADJ OFF**. Set the digital multimeter to read dc volts and connect the negative lead to the chassis of the 8562E/EC spectrum analyzer.

2. Remove W27 from A4J3 and inject a 10.7 MHz signal of +10 dBm into A4J3.

3. Set the 8562E/EC spectrum analyzer to log mode, with a resolution bandwidth of 300 kHz and single sweep.

4. Using the DMM, check the voltage at U503 pin 6.

5. Verify that this level is about −700 mV.

6. Adjust the source amplitude to place the signal at the reference level.

7. Reduce the input signal level in 10 dB steps, down to −60 dBm, while noting the voltage displayed on the DMM. The voltage should increase (become less negative) at a rate of 30 mV for each 10 dB decrease in input power. Troubleshoot the A4 assembly if the signal does not decrease properly.

8. Set the 8562E/EC spectrum analyzer resolution bandwidth to 100 kHz to place the wide/narrow filter in narrow mode.

9. Repeat steps 2 through 7.

10. If log fidelity is poor near the bottom of the screen or the 1 MHz resolution bandwidth is narrow, a fault might exist in the wide/narrow filter switch. (Refer to function block G of A4 log amplifier schematic diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.) Check this switch as follows:

    a. Monitor voltages on A4U302 pins 1 and 7 while changing the 8562E/EC spectrum analyzer resolution bandwidth from 100 kHz to 300 kHz.

    b. If the voltages do not come within a few volts of the +15 V and −15 V supplies, U103 and U302 are suspect.

    c. Disconnect the digital multimeter and reconnect W27 to A4J3.

Linear Amplifiers

Refer to function block C of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The linear amplifiers consist of two variable gain stages, U201C and U201E as well as the buffer amplifier A4U201B, A4U201D, and A4Q201. The linear amplifiers provide 0 to 40 dB of IF gain in 10 dB steps. The gain of A4U201C can be increased by 20 dB by turning on A4CR201 and A4CR210 with the control line LIN_20B. The gain of A4U201E can be increased by either 10 dB or 20 dB with the control lines LIN_10 or LIN_20A respectively. The gain can be selected by setting the 8562E/EC spectrum analyzer reference level.

Table 9-4   **IF Gain Application Guidelines (ATTEN=10 dB)**

Power into A4J3	Reference Level	Gain of A4U201C (Pin 8 in; Pin 3 out)	Gain of A4U201E (Pin 3 in; Pin 10 out)	Total Gain
+6 dBm	−50 dBm	0 dB	0 dB	0 dB
−4 dBm	−60 dBm	0 dB	10 dB	10 dB
−14dBm	−70 dBm	0 dB	20 dB	20 dB
−24 dBm	−80 dBm	20 dB	10 dB	30 dB
−34 dBm	−90 dBm	20 dB	20 dB	40 dB

Total gain can be measured by injecting the specified power into A4J3 and measuring the total gain provided by A4U201C and A4U201E. The following procedure provides a means of troubleshooting the linear amplifiers:

1. On the 8562E/EC spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, **IF ADJ OFF**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, −50 dBm, **LINEAR**, **MORE**, **AMPTD UNITS**, **dBm**, and **AMPLITUDE**.

2. Disconnect W27 (coax 3) from A4J3 and connect the output of a signal generator to A4J3.

3. Set the signal generator controls as follows:

    Amplitude .... +6 dBm
    Frequency .... 10.7 MHz

4. Simultaneously decrease the signal generator output and 8562E/EC spectrum analyzer REF LVL in 10 dB steps to −90 dBm. At each step, the signal displayed on the spectrum analyzer should be within one division of the previous position.

5. If a problem exists, isolate it by comparing the actual gain of A4U201C and A4U201E with those listed in the above gain guidelines.

6. Reconnect W27 (coax 3) to A4J3.

Video Offset

Refer to function block P of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The circuit provides a programmable video offset, with a step size of 5 mV, from −300 mV to +900 mV.

1. On the 8562E/EC/ spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, −50 dBm, **CAL**, **IF ADJ OFF**.

2. Disconnect W27 (coax 3) from A4J3 and connect a signal generator to A4J3.

3. Set the signal generator controls as follows:

   Amplitude .... +10 dBm
   Frequency .... 10.7 MHz

4. Simultaneously decrease the signal generator output and 8562E/EC spectrum analyzer reference level in 10 dB steps down to −110 dBm. At each step, the signal displayed on the spectrum analyzer should be close to the reference level.

5. Reconnect W27 (coax 3) to A4J3 and cycle the spectrum analyzer power. Press **STOP REALIGN** when it appears.

6. On the 8562E/EC spectrum analyzer, press **SWEEP**, **SINGLE**, **CAL**, and **IF ADJ OFF**.

7. The offset DAC, A4U102 pin 2, should now be at its default value of approximately +2.45 V. The voltage at U601 pin 3 should be approximately 0 V for a DAC output of 2.45 V.

8. If this default offset voltage is incorrect, DAC U102 is the most probable cause.

Video Output

1. On the 8562E/EC spectrum analyzer, press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 100 **Hz**, **AMPLITUDE**, −10 dBm, **SGLSWP**, **CAL** and **IF ADJ OFF**.

2. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Disconnect W54 (coax 2) from A4J4. Connect a short SMB to SMB cable from A4J4 to an SMB tee and connect W54 to the tee. Connect a test cable from the tee to the input of an oscilloscope.

4. Set the oscilloscope controls as follows:

   Amplitude scale .... 200 mV/div
   Offset .... +400 mV
   Coupling .... dc
   Sweep time .... 50 μs/division

5. The oscilloscope should display a 4.8 kHz sine wave.

6. Disconnect the cable from the CAL OUTPUT and the INPUT 50Ω connectors.

7. Set the resolution bandwidth to 2 MHz.

8. Broadband noise should be displayed on the oscilloscope from approximately +200 mV to +400 mV.

9. As the **REF LVL** is decreased in 10 dB steps from −10 dBm to −70 dBm, the noise displayed on the oscilloscope should increase in 100 mV increments. If this response is not observed, refer to "Step Gains" on page 474 and "Video Offset" on page 448.

10. Reconnect cable W54 to A4J4.

Frequency Counter Prescaler/Conditioner

Refer to function block Q of A4 Log Amplifier Schematic Diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The frequency counter prescaler/conditioner divides the frequency by two, and then attenuates it. The circuit consists of frequency divider (U703A) and an output attenuator. The frequency divider turns on only when the instrument is counting.

AM/FM Demodulator

Refer to function block R of A4 Log Amplifier Schematic Diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The demodulator circuitry on the log amplifier on A4 produces a low-level audio signal. This audio signal is then amplified by the audio amplifier on A4. The FM demodulator demodulates narrowband FM (5 kHz deviation) signals. The detector (block J) demodulates AM signals.

1. If demodulation problems occur when the spectrum analyzer is in the frequency domain, perform the Frequency Span Accuracy performance test and, if necessary, the YTO Adjustments procedure.

2. If an FM signal cannot be demodulated, perform the Demodulator Adjustment procedure. If the output of A4C707 cannot be adjusted as described in the Demodulator Adjustment procedure, troubleshoot the FM Demodulator or Audio MUX circuits on A4.

4.8 kHz IF Filters

Refer to function block N of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Problems with the 4.8 kHz filters can result in spurious signals appearing 2.88 kHz to 3.52 kHz above the frequency of the desired response. Also, `ERR 536 RBW <300` may occur when problems exist with the 4.8 kHz IF filters.

Measure the passband of the 4.8 kHz IF filters as described in the following procedure.

1. On the 8562E/EC spectrum analyzer, press **CAL**, **IF ADJ OFF**, **SPAN**, and 600 **Hz**.

2. Disconnect W27 from A4J3 and inject a 10.7 MHz signal of −20 dBm into A4J3.

3. Fine-tune the frequency of the signal generator to center the signal on the screen. Set the signal generator to sweep one 2 kHz span about this center frequency. Press **SGL SWP** on the 8562E/EC spectrum analyzer.

4. Set another spectrum analyzer, such as the 8566A/B, to 4.8 kHz center frequency and 2 kHz span.

CAUTION   If a dc block is not used, damage to the 8566A/B results. The 8566A/B and many other spectrum analyzers have dc-coupled inputs and cannot tolerate dc voltages on their inputs.

5. Connect the VIDEO OUTPUT (rear panel) of the 8562E/EC spectrum analyzer through a 20 dB attenuator and dc block to the input of the 8566A/B. Set the sweep time of the 8566A/B to 10 seconds.

6. Set the 8566A/B to single trigger and press TRACE A **CLEAR-WRITE**. Trigger a sweep of the 8566A/B and the signal generator simultaneously. The 8566A/B shows the passband of the 4.8 kHz IF filters. The 3 dB bandwidth of the filters should be 1.2 kHz. The passband of the filters should be flat within 2 dB over 800 Hz.

7. Reconnect W27 (coax 3) to A4J3.

10.7 MHz IF Filters

1. Press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 600 **Hz**, **CAL**, and **IF ADJ OFF**.

2. Disconnect W29 (coax 7) from A5J3. Set the signal generator for a 10.7 MHz signal at –50 dBm and connect it to A5J3.

3. Fine tune the frequency of the signal generator to center the signal on the 8562E/EC spectrum analyzer display. Set the signal generator to sweep one 2 kHz span about this center frequency.

4. On the 8562E/EC spectrum analyzer, press **SGL SWP**.

5. Disconnect W27 (coax 3) from A5J5. Connect a test cable from A5J5 to the input of an 8566A/B.

6. Set the 8566A/B as follows:

> Center frequency .... 10.7 MHz
> Span .... 2 kHz
> Reference level .... +10 dBm
> Sweep .... Single

7. Press TRACE A **CLEAR-WRITE** on the 8566A/B.

8. Trigger a sweep on the signal generator and on the 8566A/B simultaneously. The 8566A/B should display a 3 dB bandwidth of approximately 500 Hz.

9. Reconnect W27 (coax 3) to A5J5 and W29 (coax 7) to A5J3.

4.8 kHz and 10.7 MHz IF Filters

1. On the 8562E/EC spectrum analyzer, press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 600 **Hz**, **CAL**, and **IF ADJ OFF**.

2. Disconnect W29 (coax 7) from A5J3. Set the signal generator for a 10.7 MHz signal at −60 dBm and connect it to A5J3.

3. Fine tune the frequency of the signal generator to center the signal on the 8562E/EC spectrum analyzer display. Set the signal generator to sweep one 2 kHz span about this center frequency.

4. On the 8562E/EC spectrum analyzer, press **SGL SWP**.

5. Set the 8566A/B to 4.8 kHz center frequency and 2 kHz span.

CAUTION   Damage to the 8566A/B results if a dc block is not used. The 8566A/B and many other spectrum analyzers have dc-coupled inputs and cannot tolerate dc voltages on their inputs.

6. Connect the VIDEO OUTPUT (rear panel) of the 8562E/EC spectrum analyzer through a 20 dB attenuator and dc block to the input of the 8566A/B. Set the sweep time of the 8566A/B to 10 seconds.

7. Set the 8566A/B to single trigger and press TRACE A **CLEAR-WRITE**. Trigger a sweep on the 8566A/B and on the signal generator simultaneously. The 8566A/B should show a 3 dB bandwidth of 600 Hz ±100 Hz.

8. Reconnect W29 (coax 7) to A5J3.

10.6952 MHz VCXO

Refer to function block E of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The purpose of the 10.6952 MHz voltage-controlled crystal oscillator (VCXO) is to provide an LO for down-converting the peak of the 10.7 MHz IF filter passband to 4.8 kHz. Since the peak of the passband of the 10.7 MHz IF filters is 10.7 MHz ±300 Hz, the frequency of the VCXO is between 10.6949 MHz and 10.6955 MHz. This frequency can best be measured at the collector of A4Q202.

The center frequency of the 300 Hz resolution-bandwidth filters and the 1 Hz to 100 Hz filters should differ no more than 10 Hz. If the center frequency is different by more than this, or if no signal is present in the 1 Hz to 100 Hz resolution-bandwidth settings, troubleshoot the 10.6952 MHz VCXO.

Error message `ERR 539` may occur if the VCXO is not oscillating. If problems exist with the VCXO control voltage, error messages `ERR 536` or `ERR 530` may occur.

Between sweeps the VCXO, at times, is turned off. To prevent the oscillator from turning off, press **PRESET**, **FREQUENCY**, 0.3 **GHz**, **SPAN**, 1 **kHz**, **SGL SWP**, **CAL**, and **IF ADJ OFF**.

Input Switch

Refer to function block D of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The input switch switches between log and linear modes. In addition it contains a 20 dB attenuator which is used only in digital resolution bandwidth settings. CR207, CR208, and CR209 form the input switch. CR205 and CR206 switch in R234 when in linear mode to maintain a constant impedance at J3. CR210, CR211, CR212, and CR221 switch the 20 dB attenuator in and out.

LO Switch

Refer to function block F of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The LO switch switches the limiter input between the 10.7 MHz path or the 10.6952 MHz VCXO path.

Synchronous Detector

A wide dynamic range linear detector is realized by the limiter (block G), the isolation amplifier (block H), the LO amplifier (block I), and the detector/mixer (block J). The combination of these circuits form what is commonly known as a synchronous detector.

The input signal is split between two paths. One path flows through the isolation amplifier and the other path flows through the limiter and LO amplifier The path flowing through the limiter generates the LO for the detector/mixer block. The path through the isolation amplifier drives the RF port.

To troubleshoot this group of circuits set the RBW to 300 kHz. Inject 10.7 MHz at +6 dbm into J3. Probe the gate of A4Q404 or A4Q405 with a scope. Look for a 0 to –3 V square wave. Decrease the input power from +6 dBm to –84 dBm in 10 dB steps. The square wave signal should remain unchanged. It is normal for the phase of the signal to jitter at the lowest signal levels.

The signals at the gates of A4Q404 and A4Q405 should be 180 degrees out of phase from each other. If they are not 180 degrees out of phase or one of the signals are not present, troubleshoot the LO Amplifier or the FETs in the mixer. If the signal is not a symmetrical square wave, troubleshoot the LO amplifier. If the signal drops out prematurely or is not present at all, troubleshoot the limiter or LO amplifier.

Repeat the procedure for an RBW ≤ 100 kHz. If the log amplifier works in the 300 kHz RBW but not in the narrower RBWs, troubleshoot the log narrow filter in the limiter or isolation amplifier. A4CR302 and A4CR303 are varactor diodes in the limiter filter and are used to tune the filter.

Limiter

Refer to function block G of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The limiter consists of 7 identical 20 dB gain stages. A "log narrow filter" is switched in for RBWs ≤100 kHz. This filter is switched in using the control lines NARROW between the 4th and 5th stages. During normal operation, the limiter serves to amplify even the smallest 10.7 MHz signals up to a level sufficient to drive the LO Amplifier and subsequent detector/mixer. This signal serves as the LO for the mixer circuitry.

Isolation Amplifier

Refer to function block H of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The isolation amplifier prevents LO port to RF port feedthrough in the mixer from feeding back to the input of the limiter and causing loop oscillations. In addition, the isolation amplifier matches the phase of the non-limited signal path to the phase of the limited signal path. The isolation amplifier should have a gain of about 4 dB and also has a "log narrow filter" that is switched with the control line NARROWB.

Detector/Mixer

Refer to function block J of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Sum and difference frequencies are produced in the detector/mixer. The difference frequency produces video (dc to approximately 3 MHz), since the two signals are at the same frequency. During digital resolution bandwidths the two signals are separated by about 4.8 kHz.

Log Offset/Gain Compensation

Refer to function blocks L and M of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

Log Offset Compensation

The gain of A4U503 is set to unity, with A4R539 and A4R540 combining for a gain of 0.5. Therefore, the gain from A4U503 pin 3 to A4U508 pin 3 should be 0.5.

Log Gain Compensation

The gain of A4U508 is nominally 6.8, measuring from pin 3 to pin 8. To check the log offset/gain compensation circuits, inject a +10dBm signal into J3 with the 8562E/EC spectrum analyzer set to log mode. Measure A4U503 pin 3, V_{in} (1) and A4U508 pin 3, V_{out} (1) and record the results. Decrease the input level to −40 dBm and make the same measurements recording V_{in} (2) and V_{out} (2).

The gain is then:

$$\frac{(V_{OUT}(1) - V_{OUT}(2))}{(V_{IN}(1) - V_{IN}(2))}$$

This gives an offset-independent gain measurement.

Video MUX

The video MUX switches the video output between linear, log and
4.8 kHz IF (for digital RBWs). The demod video is an unused feature.
The easiest way to troubleshoot this circuit is to look for blown FETs.
Bad FETs are characterized by having significant gate current. Only
one of the signal lines LIN_VIDEO, IF_VIDEO or LOG_VIDEO should
be high (+15 V) at any given time. The others should be low (–15 V).
Also look for a voltage drop of several volts across the gate resistors
R601, R605, R609, or R613 when in either the off or on state. This
indicates gate current and thus a bad FET.

A5 IF Assembly

The input switch connects the IF to either the cal oscillator on the A4 assembly or the 10.7 MHz IF output from the A15 RF assembly. The automatic IF adjustment uses the cal oscillator on A4 at instrument turn-on and between sweeps to align the IF filters and step-gain amplifiers. During sweeps the input switch selects the 10.7 MHz IF output from A15. The LC filters are variable-bandwidth filters that provide resolution bandwidths from 30 kHz to 2 MHz. The automatic IF adjustment sets the bandwidths and center frequencies of each filter stage.

The crystal filters are variable-bandwidth filters that provide resolution bandwidths from 300 Hz to 10 kHz. The automatic IF adjustment sets the filter bandwidths and symmetry.

The step-gain amplifiers consist of the first step-gain stage, second step-gain stage, and third step-gain stage. These amplifiers provide gain when the 8562E/EC spectrum analyzer reference level is changed. The amplifiers also provide gain range to compensate for variations in the IF filter gains, which change with bandwidth and environmental conditions, and band conversion loss in the front end. Fixed-gain amplifiers shift the signal levels to lower the noise of the IF chain.

The assembly has two variable attenuators. The fine attenuator provides the 0.1 dB reference level steps. The reference 15 dB attenuator provides a reference for automatic adjustment of the step-gain amplifiers and the log amplifier. The reference 15 dB attenuator also provides gain for changes in spectrum analyzer reference level.

Various buffer amplifiers provide a high-input impedance to prevent loading of the previous filter pole and a low-output impedance to drive the next filter pole.

Digital control signals from the W2 control cable, the "analog bus," drive the control circuitry. At the beginning of each sweep, the analog bus sets each control line for instrument operation. At the end of each sweep, the analog bus sets each control line for the next portion of the automatic IF adjustment routine. IF adjustments continuously remove the effects of component drift as the spectrum analyzer temperature changes.

The assembly contains a reference limiting amplifier. This amplifier provides a known amount of limiting for the automatic IF adjustment routines. (Limiting occurs only during the automatic IF adjustment routines.) The LC34_Short switches are open during sweeps. The current in the reference limiter is increased during sweeps to prevent limiting.

CAUTION   For troubleshooting, it is recommended that you use an active probe, such as an 85024A, and another spectrum analyzer. If an 1120A active probe is being used with a spectrum analyzer having dc-coupled inputs, such as the 8566A/B, 8569A/B and the 8562A/B, either set the active probe for an ac-coupled output or use a dc-blocking capacitor between the active probe and the spectrum analyzer input.

CAUTION   Do not short control voltages to ground. These voltages are not short-circuit protected. DACs damaged by shorting these voltages might not fail until several weeks after the shorting takes place.

Do not short power-supply voltages to ground. The 8562E/EC spectrum analyzer power-supply current limiting cannot protect the resistors in series with the power supply.

NOTE   Some transistors have collectors connected to the case. Electrical connection of the case to the collector might not be reliable, making collector voltage measurements on the transistor case unreliable.

IF Signature

1. Disconnect W27 (coax 3) from A5J5.

2. Connect an SMB tee to A5J5, using a short coaxial cable with SMB connectors.

3. Connect one output of the tee to cable W27 (coax 3).

4. Connect an 85024A active probe, with a 10:1 divider installed, to the other output of the tee.

5. Connect the output (type N connector) of the active probe to the input of the 8566A/B spectrum analyzer.

6. Connect the probe power cable to the 8562E/EC spectrum analyzer front-panel PROBE POWER connector (you may need to use a probe power extension cable, 10131B).

7. Set the 8566A/B controls as follows:

    Reference level .... +10 dBm
    Center frequency .... 10.7 MHz
    Span .... 0 Hz
    Resolution bandwidth .... 300 kHz
    Video bandwidth .... 300 kHz
    Sweep time .... 5.5 s
    Trigger .... Single

8. On the 8566A/B, press **SHIFT** (trace A blank) to set detector to SAMPLE mode.

9. On the 8562E/EC spectrum analyzer, press **PRESET** and set the controls as follows:

    Center frequency .... 300 MHz
    Span .... 5 MHz

10. On the 8562E/EC spectrum analyzer, press **SGL SWP** and **CAL**.

11. Simultaneously press **SINGLE** on the 8566A/B and **ADJ CURR IF STATE** on the 8562E/EC spectrum analyzer. The IF signature is displayed on the 8566A/B display. It may be necessary to experiment with different time intervals between initiating the sweep on the 8566A/B and initiating the current IF state adjustment on the 8562E/EC spectrum analyzer.

12. Compare the IF signature to the signature of a properly operating spectrum analyzer illustrated in Figure 9-3 on page 460. If the signatures do not closely resemble each other, a more detailed view of the signature may show the failed hardware.

    a. Set the 8566A/B controls as follows:

        Sweep time .... 550 ms
        dB/division .... 5 dB
        Reference level .... − 5 dBm

    b. Press **SINGLE** on the 8566A/B and, a very short time later, press **ADJ CURR IF STATE** on 8562E/EC spectrum analyzer. Figure 9-4 on page 461 through Figure 9-8 on page 465 illustrate detailed IF signatures of a properly operating 8562E/EC spectrum analyzer. It may be necessary to experiment with different time intervals between initiating the sweep on the 8566A/B and initiating the current IF state adjustment on the 8562E/EC spectrum analyzer to obtain the waveforms shown. Note the changes in the 8566A/B video bandwidth and sweep time.

13. Reconnect W27 (coax 3) to A5J5.

Figure 9-3   IF Adjust Signature


```
   IF Adjust signature                    MKR 5.044 sec
   REF  10.0 dBm    ATTEN 20 dB              -42.30 dBm

10 dB/                                FIG. 8-7

SAMPLE




                      FIG. 8-4
                   FIG. 8-5



                       FIG. 8-6          FIG. 8-8

CENTER 10.700 000 MHz                    SPAN 0 Hz
     RES BW 300 kHz    VBW 300 kHz    SWP 5.50 sec
```
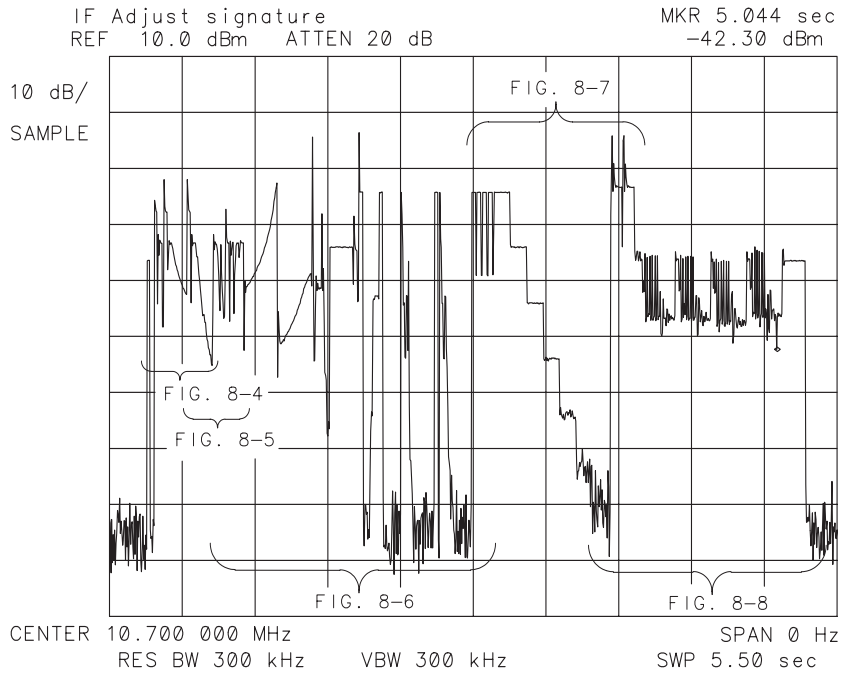
sp143e

Figure 9-4 **Detailed IF Adjust Signature (1)**
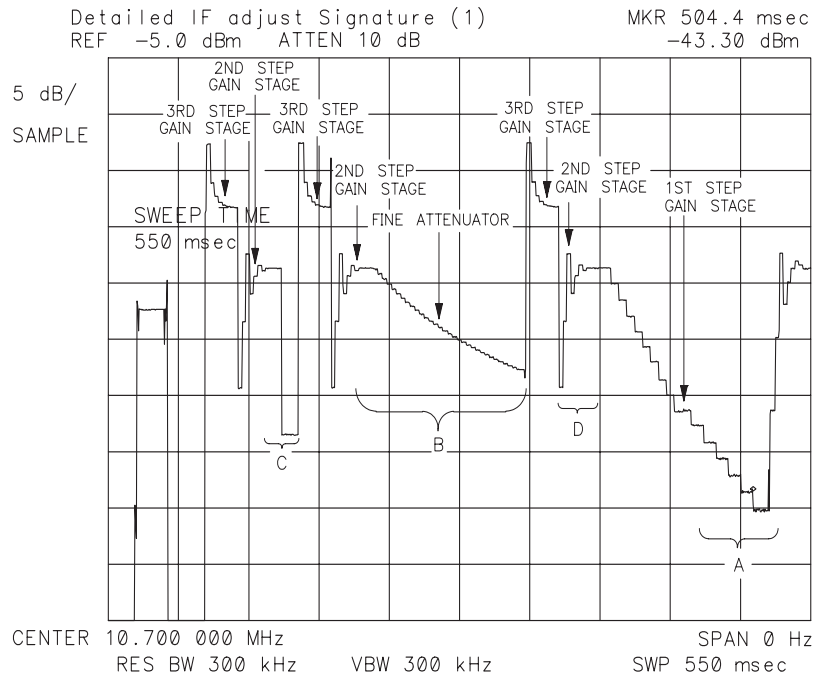
Figure 9-5   Detailed IF Adjust Signature (2)


```
Detailed If Adjust Signature (2)          Mkr 504.4 msec
  REF  -5.0 dBm    ATTEN 10 dB                  -30.80 dBm
```
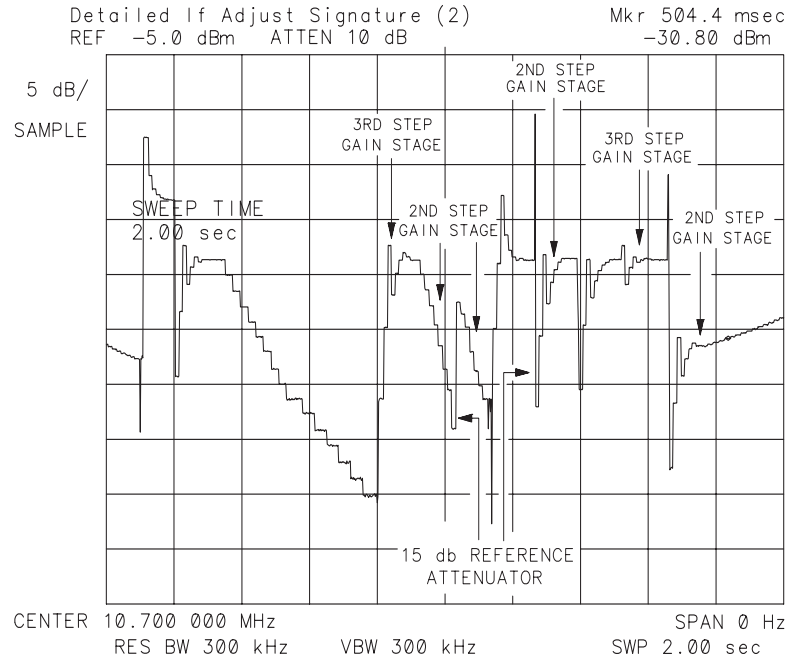
Figure 9-6   Detailed IF Adjust Signature (3)

Detailed If Adjust Signature (3)   MKR 1.834 sec
REF −5.0 dBm   ATTEN 10 dB   −14.60 dBm
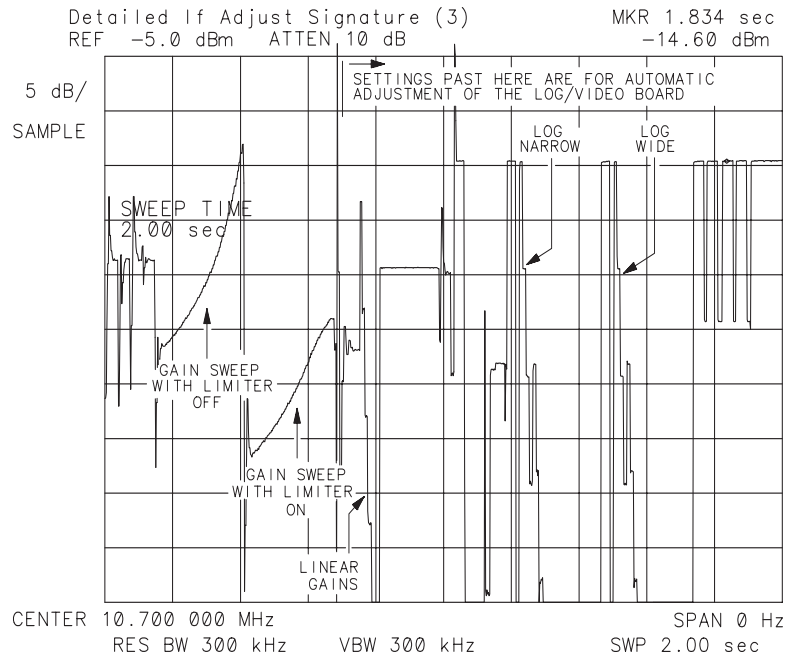
Figure 9-7   Detailed IF Adjust Signature (4)
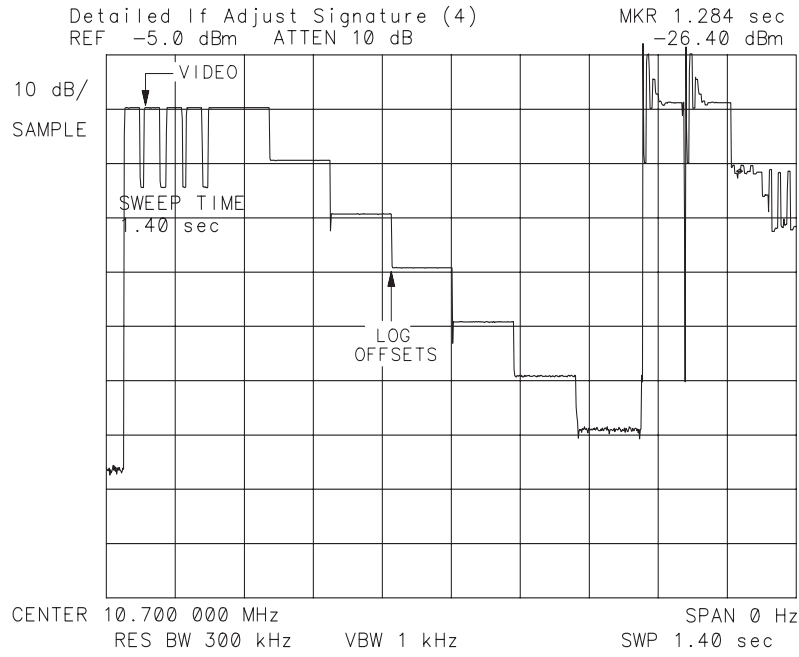
Figure 9-8   Detailed IF Adjust Signature (5)


```
Detailed If Adjust Signature (5)          MKR 1.834 sec
REF  -5.0 dBm    ATTEN 10 dB                   -84.40 dBm
```

10 dB/

SAMPLE

SWEEP TIME
2.00 sec

1ST   2ND   3RD   4TH
LC POLE LC POLE LC POLE LC POLE

SETTINGS PAST HERE ARE FOR
AUTOMATIC ADJUSTMENT OF THE
30kHz RESOLUTION BANDWIDTH

```
CENTER 10.700 000 MHz                     SPAN 0 Hz
      RES BW 300 kHz    VBW 1 kHz      SWP 2.00 sec
```
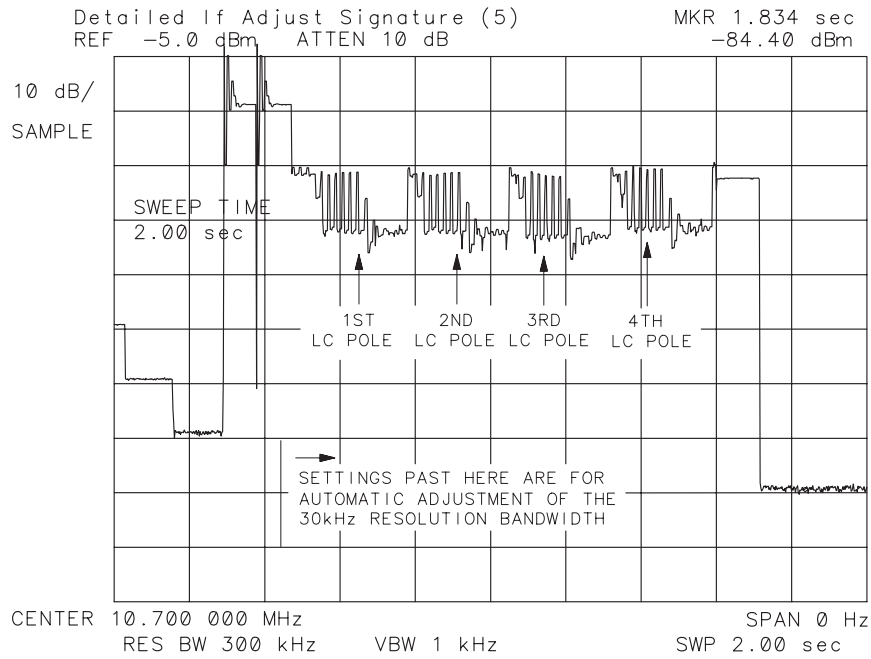
sp148e

Common IF Signature Problems

Region A of is noisy:

Suspect the first LC pole.

Region B of is flat:

Suspect the third step-gain stage, the fine attenuator, or the fourth LC-pole output amplifier.

Region C of has no 15 dB step:

Suspect the reference 15 dB attenuator.

Region D of is flat:

Suspect the second step-gain stage.

Entire signature noisy:

If the signature resembles, suspect a broken first step-gain stage or a break in the signal path in the input switch, first crystal pole, or second crystal pole.

Correct shape but noisy:

If the signature resembles, suspect the second crystal-pole output amplifier.

Amplitude of Region B of varies more than 12 dB:

Suspect the third step-gain stage output amplifier.

Region B of is kinked:

Suspect the fourth LC-pole output amplifier.

Figure 9-9   Noisy Signature

REF 10.0 dBm   ATTEN 20 dB
5 dB/
SAMPLE

CENTER 10.700 000 MHz   SPAN 0 Hz
       RES BW 300 kHz   VBW 300 kHz   SWP 500 sec
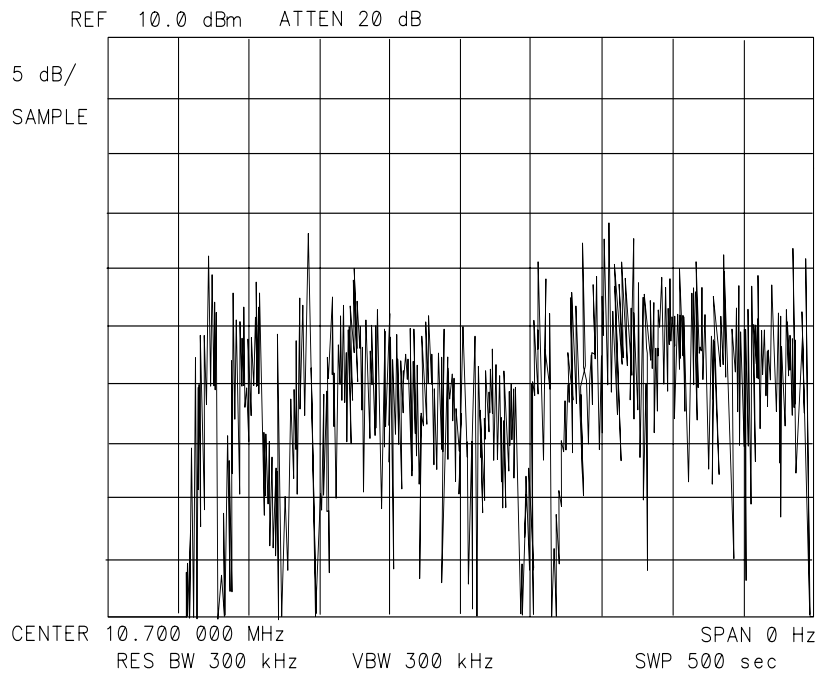
SK178

Figure 9-10   Noise with Correct Shape


```
        REF   10.0 dBm    ATTEN 20 dB
5 dB/
SAMPLE

 CENTER 10.700 000 MHz                          SPAN 0 Hz
        RES BW 300 kHz      VBW 300 kHz      SWP 500 sec
```
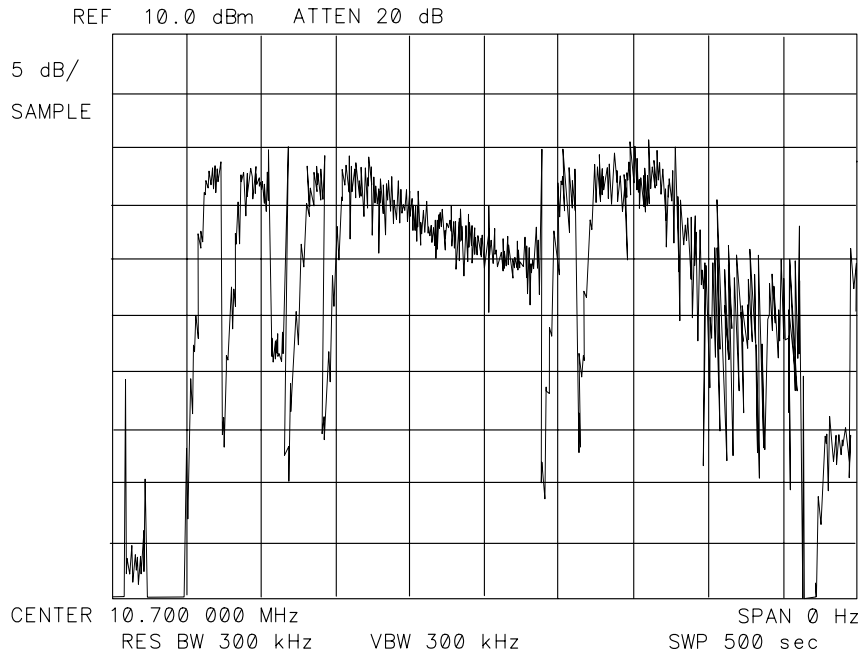
SK179

Figure 9-11   Region B Amplitude Variation


```
     REF   10.0 dBm    ATTEN 20 dB

5 dB/

SAMPLE



CENTER 10.700 000 MHz                              SPAN 0 Hz
     RES BW 300 kHz       VBW 300 kHz         SWP 500 sec
```
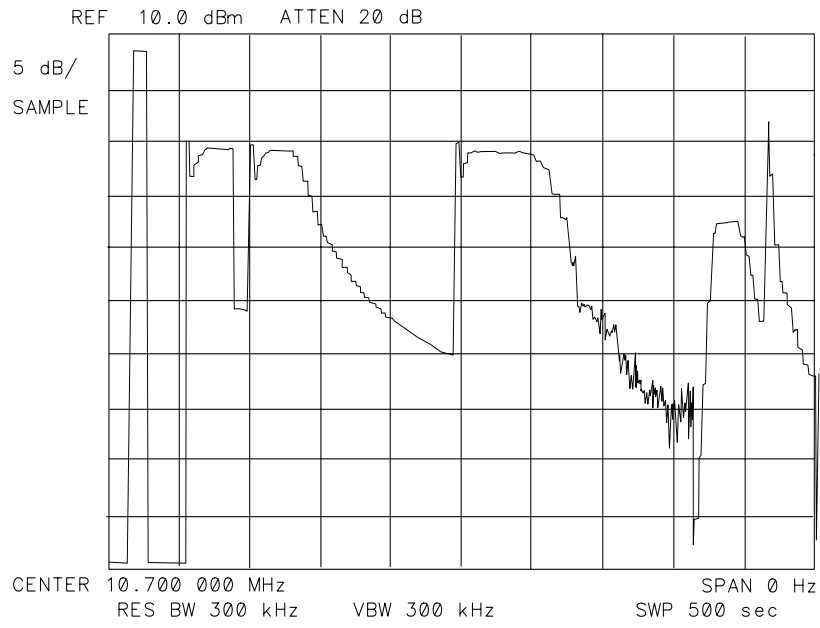
SK180

Figure 9-12   **Region B Amplitude Offset**
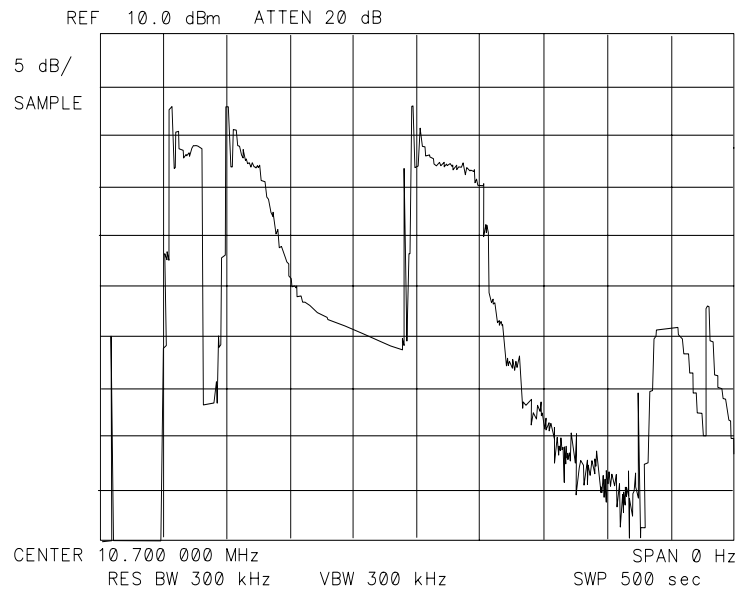
SK181

1 MHz Resolution Bandwidth Problems

Check the crystal shorting switches as follows:

1. On the 8562E/EC spectrum analyzer, press **PRESET** and set the
    controls as follows:

> Resolution bandwidth .... 1 MHz
> Span .... 500 kHz
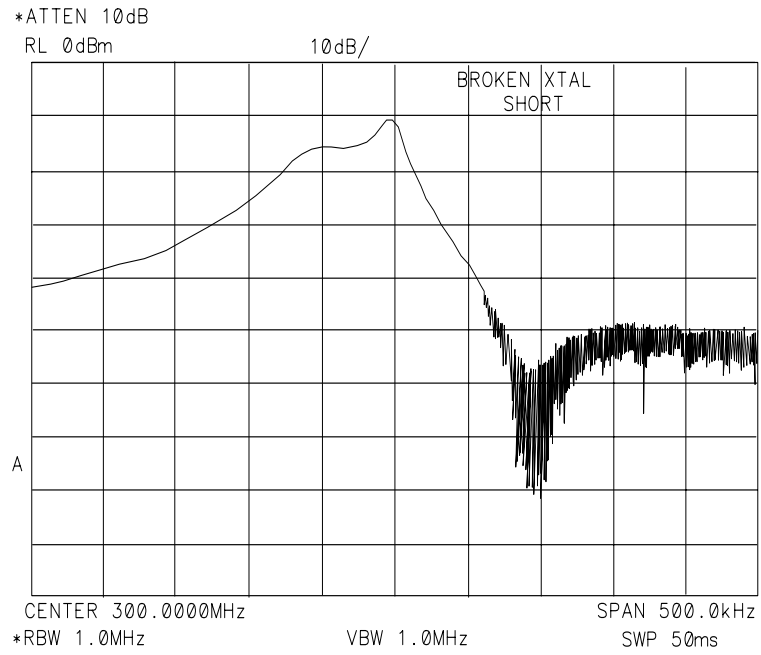> Center frequency .... 300 MHz

2. On the 8562E/EC spectrum analyzer, connect the 300 MHz
    CAL OUTPUT to the INPUT 50Ω .

3. If the trace flatness is not within 2.5 dB, a failure probably exists.

4. A trace similar to indicates a crystal short failure.

5. Press **SPAN** to set the spectrum analyzer to 3 MHz. A trace that
    slopes across the screen (see) indicates a failed LC pole. To isolate
    the broken pole refer to the shape factor information in

Figure 9-13   **Faulty Crystal Short**


```
*ATTEN 10dB
 RL 0dBm                    10dB/
                                    BROKEN XTAL
                                       SHORT



A


 CENTER 300.0000MHz                    SPAN 500.0kHz
 *RBW 1.0MHz            VBW 1.0MHz      SWP 50ms
```

SK182

Figure 9-14 **Faulty LC Pole**


```
*ATTEN 10dB
 RL 0dBm                   10dB/
                                    BROKEN LC POLE




 A




 CENTER 300.0000MHz                      SPAN 3.000MHz
*RBW 1.0MHz              VBW 1.0MHz        SWP 50ms
```
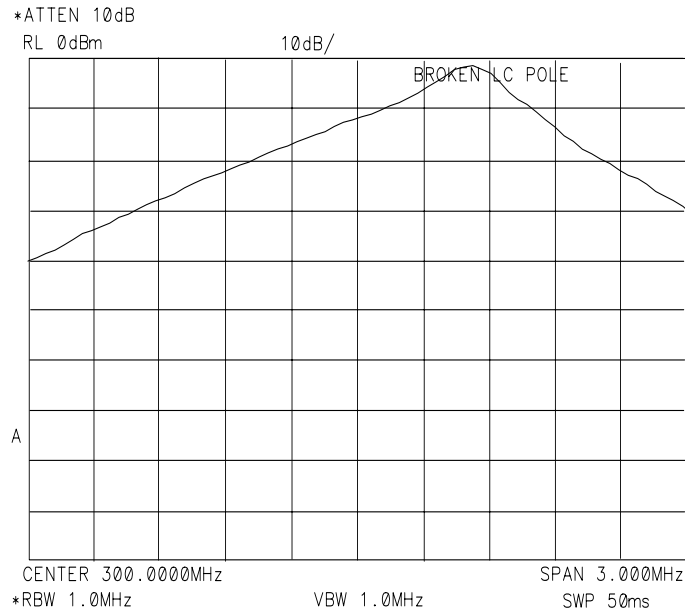
SK183

30 kHz Resolution Bandwidth Problems

Shape factor too high: Shape factor is the ratio of the 60 dB bandwidth to the 3 dB bandwidth. Shape factor should be less than 15:1. If one of the LC poles malfunctions, the shape factor may be the only indication of the failure. Isolate the non-functioning pole with the IF signature. Region E of illustrates the four LC-pole adjustments. Take several signatures to examine the LC-pole adjustments. If one of the four sections of Region E is consistently longer than the others, the corresponding LC pole is faulty.

IF gain compression: FET transistors Q301, Q303, Q700, and Q701 can deteriorate with age. Measuring less than 0 volts on the FET source indicates a bad FET.

Bandwidth too wide: Check for contamination on the printed-circuit board. Clean the board as required.

## 3 kHz and 10 kHz Resolution Bandwidth Problems

Asymmetric Filter Response: Check the crystal symmetry control with the following steps:

1. Press **PRESET**.

2. Set the 8562E/EC spectrum analyzer controls as follows:

   Resolution bandwidth .... 3 kHz
   Span .... 100 kHz
   Center frequency .... 300 MHz

3. On the 8562E/EC spectrum analyzer, connect the 300 MHz CAL OUTPUT to the INPUT 50Ω .

4. A trace similar to indicates a failed crystal-symmetry circuit.

Narrow 10 kHz resolution bandwidth: Check for printed-circuit board contamination. Clean the board as required.

IF Gain Compression in 10 kHz resolution bandwidth: FET transistors Q202, Q203, Q501, and Q503 can deteriorate with age. Measuring less than 0 volts on the FET source indicates a bad FET.

Figure 9-15   Faulty Crystal Symmetry
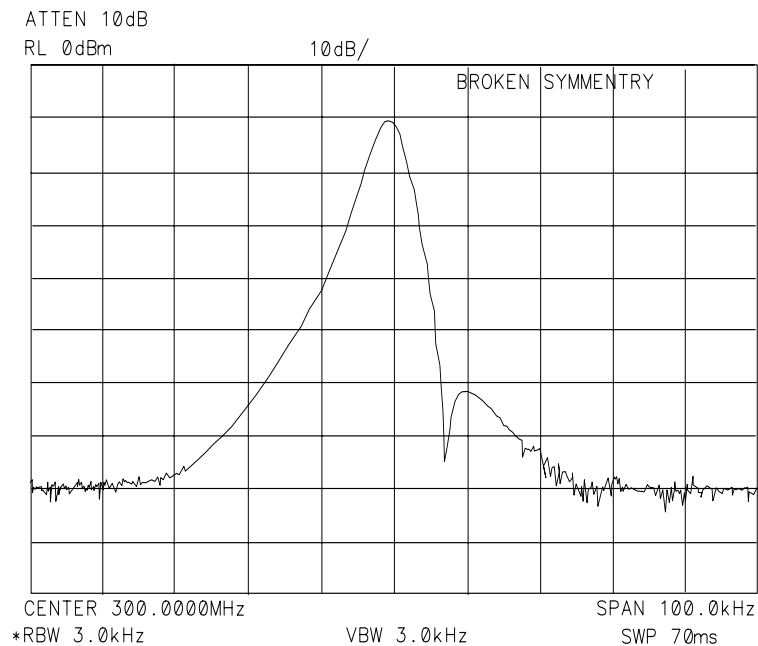
Step Gains

Refer to function blocks B, H, and I of A5 IF filter schematic diagram (sheets 1 of 3 and2 of 3) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. On the 8562E/EC spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, and 1 **GHz**.

2. Press **CAL** and **IF ADJ OFF**.

3. Disconnect W29 (coax 7) from A5J3 and W27 (coax 3) from A5J5.

4. Inject a −5 dBm, 10.7 MHz signal into A5J3.

5. Monitor the output of A5J5 with another spectrum analyzer.

6. Simultaneously decrease the signal generator output and 8562E/EC spectrum analyzer reference level in 10 dB steps down to a −50 dBm reference level.

7. At each step, the signal displayed on the other spectrum analyzer should be close to +10 dBm. (More subtle IF gain problems might require smaller signal generator and reference level steps.)

8. Reconnect W29 to A5J3 and W27 (coax 3) to A5J5.

Cal Oscillator (P/O A4 Assembly)

The cal oscillator on the A4 assembly supplies the stimulus signal for automatic IF adjustments. Normally, the oscillator operates only during retrace (for a few milliseconds) to adjust part of the IF. (All IF parameters are to be readjusted about every 5 minutes.) With continuous IF adjust ON, a group of IF parameters are adjusted during each retrace period (non-disruptive). If continuous IF adjust is OFF, the most recent IF calibration data is used.

The IF parameters adjusted include step gains, log amplifier gain and offset, bandwidth centering, 3 dB bandwidth, bandwidth amplitude, and crystal-filter symmetry.

The cal oscillator provides three types of output signals (all –35 dBm):

- 10.7 MHz

- 9.9 to 11.5 MHz in 100 kHz steps

- Frequency sweeps from 20 kHz to 2 kHz centered at 10.7 MHz (lasting 5 to 60 ms respectively)

The signals perform the following functions:

- Adjust gains, log amps, and video slopes and offsets.

- Adjust 3 dB bandwidth and center frequencies of LC resolution bandwidth filters (30 kHz through 1 MHz).

- Adjust 3 dB bandwidth, symmetry, and gain of the crystal resolution bandwidth filters (300 Hz through 10 kHz).

The cal oscillator uses a phase-locked loop (PLL). The oscillator (function block X) is locked to the instrument 10 MHz reference. The reference divider (function block U) divides the reference and delivers a 100 kHz TTL signal to the phase detector (function block V). The divide-by-N circuitry (function block Y) divides the oscillator output of 9.9 MHz to 11.5 MHz (by 99 to 115) resulting in a 100 kHz output to the phase detector. When the cal-oscillator PLL is locked, narrow positive and negative of equal width pulses occur at the phase detector output. Since the phase detector drives a low-input impedance at the loop integrator, observe the positive pulses at A4CR808 anode and negative pulses at A4CR809 cathode.

The loop integrator acts as a low-pass filter that filters the pulses and inverts the result. If the anode of A4CR808 is more positive (with respect to ground) than the cathode of A4CR809 is negative, the loop integrator output should saturate to approximately –13 V. Conversely, if the anode of A4CR808 is less positive than the cathode of A4CR809 is negative, the integrator should saturate to a positive voltage.

NOTE

If error messages `ERR 581 AMPL` or `ERR 582 AMPL` appears, refer to error message `ERR 582 AMPL` in Chapter 7 , "General Troubleshooting," and perform the procedure provided.

1. The oscillator output frequency should exceed 11.5 MHz if the CAL OSC TUNE line, A4U804 pin 14, exceeds +9 V. The oscillator frequency should be less than 9.9 MHz if CAL OSC TUNE is below −9 V. The oscillator only operates when CALOSC_OFF is low (0 V).

2. If the cal oscillator remains locked (no error code `ERR 499` displayed) but does not have the correct output level, troubleshoot the output leveling circuitry (function blocks AA, AB, and AC) or output attenuator (function block AD).

Cal Oscillator Unlock at Beginning of IF Adjust

1. Press **LINE** to turn the 8562E/EC spectrum analyzer off and then on. The words `IF ADJUST STATUS` appear on the display 10 seconds after the instrument is turned on (assuming the rest of the instrument is working correctly). Immediately observe the lower right corner of the display for error messages. If the message `ERR 499 CAL UNLK` appears (before errors `ERR 561`, `ERR 562` and `ERR 565`), the cal oscillator is unable to phase-lock. Expect to see the `ERR 499` message for only about 1 second.

2. If the 8562E/EC spectrum analyzer registers an unlocked cal oscillator, continue with step 3 to verify the presence of externally supplied signals.

3. Check A4U811 pin 9 for a 100 kHz TTL-level square wave verifying operation of A4U811, A4Q802, and the 10 MHz input signal from A4J7.

4. Check the +15 VF, +5 VF and −15 V power supplies, and +10 V reference on the A4 assembly.

5. Check that A4U807 pin 5 (CALOSC_OFF) becomes TTL low (0 V) at the start of a FULL IF ADJ (press **CAL** and **FULL IF ADJ**). The phase modulation output at A4U804 pin 8 should also remain at 0 volts. If these checks are correct, troubleshoot blocks V, W, X, and Y. See, A4 log amplifier/cal oscillator Block Diagram.

Inadequate CAL OSC AMPTD Range

Refer to function block AC of A4 Log Amplifier Schematic Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. If A4R826, CAL OSC AMPTD, has inadequate range to perform the IF Amplitude Adjustment, press **CAL**.

2. Rotate A4R826 fully clockwise and disconnect W52 (coax 9) from A5J4.

3. Connect A5J4 to the input of a second spectrum analyzer.

4. Set the other spectrum analyzer controls as follows:

   Center frequency .... 10.7 MHz
   Reference level .... −30 dBm

5. Observe the spectrum analyzer display while pressing **FULL IF ADJ**. The signal level should be above −34.55 dBm. If the signal level is incorrect, continue with step 7.

6. Rotate A4R826 fully counterclockwise. The signal should be below −36.25 dBm. If the signal level is correct at both settings, troubleshoot the A5 IF assembly. If the signal level is incorrect, continue with step 7.

7. Troubleshoot the ALC loop on this assembly using the following steps:

   a. Connect a positive DVM probe to A4J9 pin 4.

   b. On the 8562E/EC spectrum analyzer, press **CAL**.

   c. Press **FULL IF ADJ**. Observe the DVM reading between the displayed messages `IF ADJUST STATUS: 300 kHz RBW` and `IF ADJUST STATUS: 3 kHz RBW`. During this time period, the voltage should be within a 2 to 10 Vdc range.

   d. Observe the DVM reading while `IF ADJUST STATUS: AMPLITUDE` is displayed. The reading should be within the 2 to 10 Vdc range.

   e. If the DVM reading is outside the range in step c but inside the range in step d, suspect a reactive component of the filter.

8. If the ALC loop is working correctly (A4J9 pin 4 within the test tolerances given), then either the output attenuator is defective, or A4U810 pin 6 (in ALC loop integrator) is outside of its +3 to +6 Vdc range.

9. Reconnect W52 (coax 9) to A5J4.

300 Hz to 3 kHz Resolution Bandwidth Out of Specification

1. If the 3 dB bandwidth of one of these filters is incorrect, suspect a failure of one of the five available sweeps from the cal oscillator sweep generator (function block Z). These sweeps are generated by changing the switch settings of A4U803 which routes signals through A4U802 and A4U804.

2. Disconnect W52 (coax 9) from A4J8.

3. Connect an SMB tee to A4J8, using a short coaxial cable with SMB connectors.

4. Connect one output of the tee to cable W52 (coax 9).

5. Connect an 85024A active probe to the other output of the tee.

6. Connect the output (type N connector) of the active probe to the input of the 8566A/B spectrum analyzer.

7. Connect the probe power cable to the 8562E/EC spectrum analyzer front-panel PROBE POWER connector (you may need to use a probe power extension cable, 10131B).

8. Press **INSTR PRESET** on the 8566A/B and set the controls as follows:

Center frequency	10.8 MHz
Span	0 Hz
Reference level	−43 dBm
Resolution bandwidth	100 kHz
Video bandwidth	10 kHz
Sweep time	50 ms
Scale	1 dB/division
Sweep	Single

9. On the 8562E/EC spectrum analyzer, press **PRESET** and **CAL**.

10. Press **FULL IF ADJ**. When the display reads `ADJUSTING IF:
    10 kHz RBW`, press **SINGLE** on the 8566A/B.

11. The 8566A/B screen illustrates frequency versus time of the cal oscillator output sweeps. See . The slope of the 8566A/B 100 kHz resolution bandwidth is used to detect frequency changes. Sweeps that vary (greater than 30 percent) from the normal levels, trigger error code `ERR 581` or `ERR 582`.

12. Press **FULL IF ADJ**. When the display reads `ADJUSTING IF: 3 kHz`, press **SINGLE** on the 8566A/B.

13. Figure 9-17 on page 481 illustrates normal operation. Severe failures (slope error greater than 30 percent) and subtle 3 kHz resolution bandwidth errors (less than 30 percent) indicate a problem with A4U802, A4U803, A4U804, or A4U106.

14. Severe failure of the bandwidth accompanied by subtle errors in the output signal indicate an A5 failure.

15. Set the 8566A/B controls as follows:

> Center frequency .... 10.710 MHz
> Resolution bandwidth .... 10 kHz
> Video bandwidth .... 1 kHz
> Sweep time .... 200 ms

16. On the 8562E/EC spectrum analyzer, press **FULL IF ADJ**. When the message `IF ADJUST STATUS:1 kHz RBW` appears, press **SINGLE** on the 8566A/B.

17. Figure 9-18 on page 482 illustrates normal operation. Severe failures (slope error greater than 30 percent) and subtle 3 kHz resolution bandwidth errors (less than 30 percent) indicate a problem with A4U802, U803, U804, or U106.

18. On the 8562E/EC spectrum analyzer, press **FULL IF ADJ**. When the message `IF ADJUST STATUS: 300 Hz RBW` appears, press **SINGLE** on the 8566A/B.

19. Figure 9-19 on page 483 illustrates normal operation. Severe failures (slope error >30 percent) and 3 kHz resolution bandwidth errors (less than 30 percent) indicate a problem with A4U802, U803, U804, or U106.

20. Reconnect W52 (white) to A4J8.

Figure 9-16   Output Waveform, 10 kHz Resolution Bandwidth

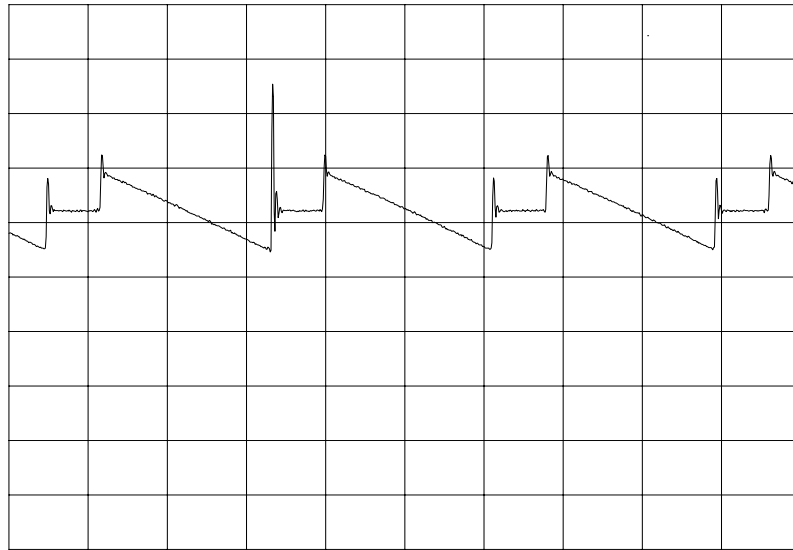**Figure 9-17** **Output Waveform, 3 kHz Resolution Bandwidth**

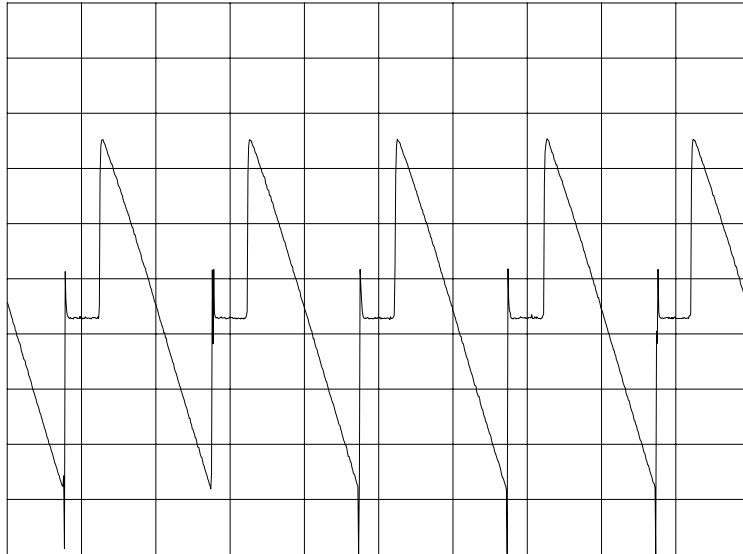**Figure 9-18   Output Waveform, 1 kHz Resolution Bandwidth**

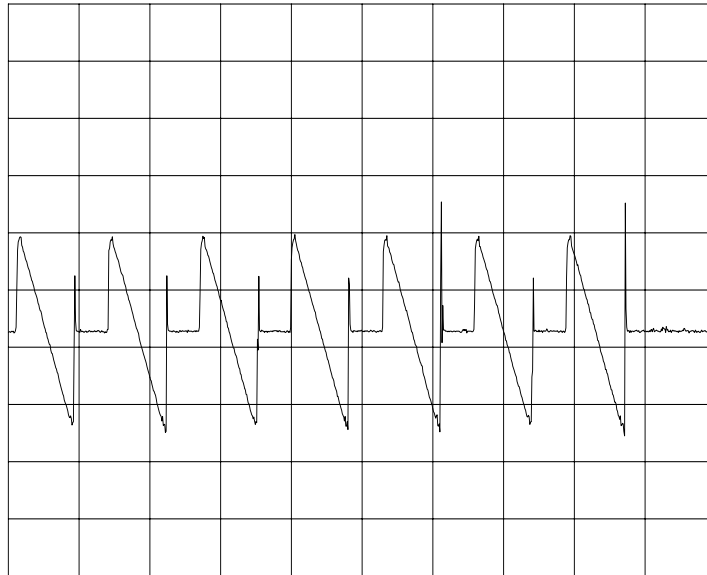**Figure 9-19   Output Waveform, 300 Hz Resolution Bandwidth**

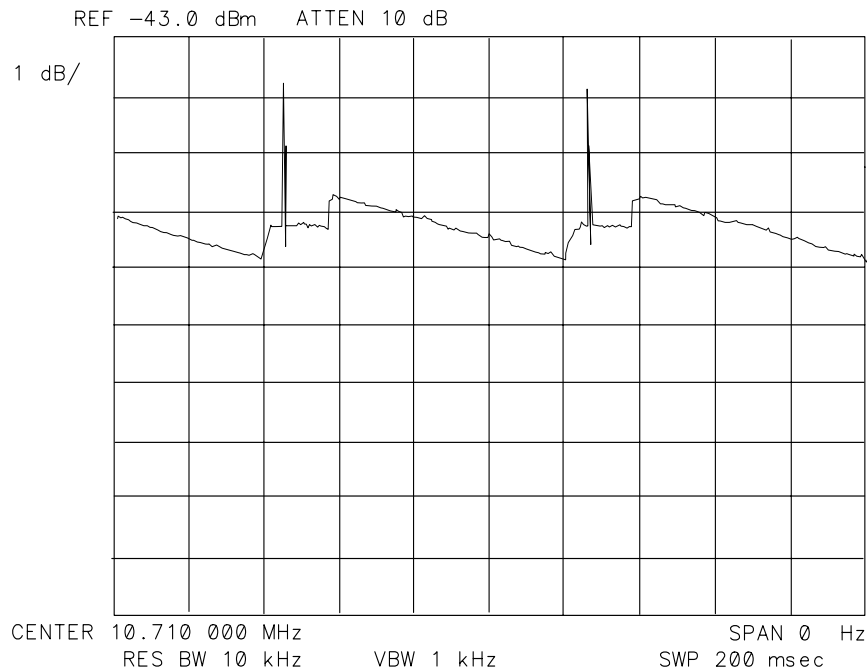**Figure 9-20   Failed Crystal Set Symptoms**

REF −43.0 dBm   ATTEN 10 dB
1 dB/

CENTER 10.710 000 MHz   SPAN 0   Hz
RES BW 10 kHz   VBW 1 kHz   SWP 200 msec

SK189

Low-Pass Filter

Refer to function block AB of A4 Log Amplifier Schematic Diagram
(sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level
Information*.

1. Connect a DVM positive probe to A4J9 pin 4.

2. On the 8562E/EC spectrum analyzer, press **CAL**.

3. Press **FULL IF ADJUST**. Observe the DVM reading between the
   displayed messages `IF ADJUST STATUS: 300 kHz RBW` and
   `IF ADJUST STATUS: 3 kHz RBW`. During this time period, the
   voltage should be within a 2 to 10 Vdc range.

4. Observe the DVM reading while `IF ADJUST STATUS: AMPLITUDE` is
   displayed. The reading should be within the 2 to 10 Vdc range.

5. If the DVM reading is outside the range in step 3 but inside the
   range in step 4, suspect one of the reactive components of the filter.

Sweep Generator

Refer to function block Z of A4 Log Amplifier Schematic Diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

A properly operating sweep generator generates a series of negative-going parabolas. Before the sweep, switches A4U802C and A4U802D turn on, shorting A4C802 and A4C801 (the output is at 0 volts). These switches open to start the sweep. The output of A4U804A, pin 1, is 0.35 V to 10 V, depending on the sweep width selected by A4U802A and A4U803A. This voltage appears across A4R801. Capacitor A4C801 integrates the current through A4R801. The output of A4U804B is a straight, negative-going ramp. Capacitor A4C802 and resistor A4R802 integrate the output of A4U804A which starts a negative ramp (A4U804C) at the beginning of the sweep. The ramp from A4U804B is added to the current in A4R802 via A4U803B. Integrating this ramp results in the parabolic output waveform.

AM/FM Demodulation, Audio Amplifier, and Speaker

Refer to function blocks R, S, and T of A4 Log Amplifier Schematic (sheet 4 of 4) Diagram in the *8560 E-Series Spectrum Analyzer Component Level Information*.

If the audio circuits are not functioning use the following procedure to isolate the problem:

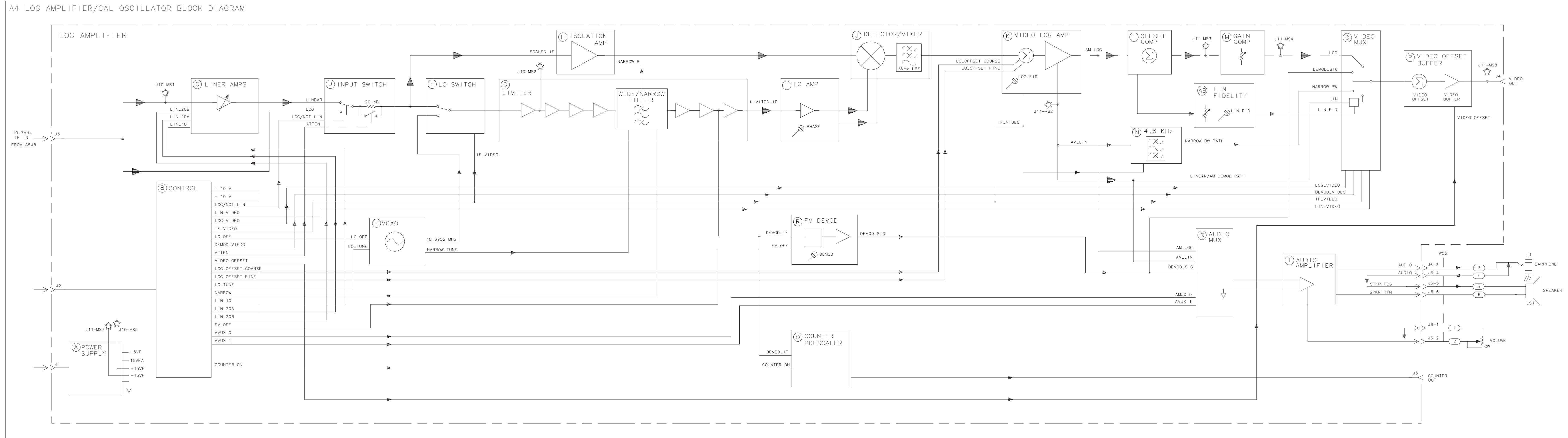1. Set an AM signal generator controls as follows:

   Frequency .... 100 MHz
   Amplitude .... −6 dBm
   Modulation type .... 80% AM
   Modulation frequency .... 400 Hz

2. Set the 8562E/EC spectrum analyzer controls as follows:

   Center frequency .... 100 MHz
   Span .... 0 Hz
   Sweep time .... 50 ms
   Reference level .... 0 dBm
   Resolution bandwidth .... 10 kHz
   Amplitude scale .... LINEAR

3. Adjust the 8562E/EC spectrum analyzer reference level and center frequency to display the 400 Hz modulation frequency eight divisions peak-to-peak.

4. On the 8562E/EC spectrum analyzer, press **AUX CTRL**, **AM/FM DEMOD**, **AM DEMOD ON**, and set the sweep time to 5 seconds.

5. Vary the volume and listen for the variation in speaker output level. Clipping is normal at the highest volume levels.
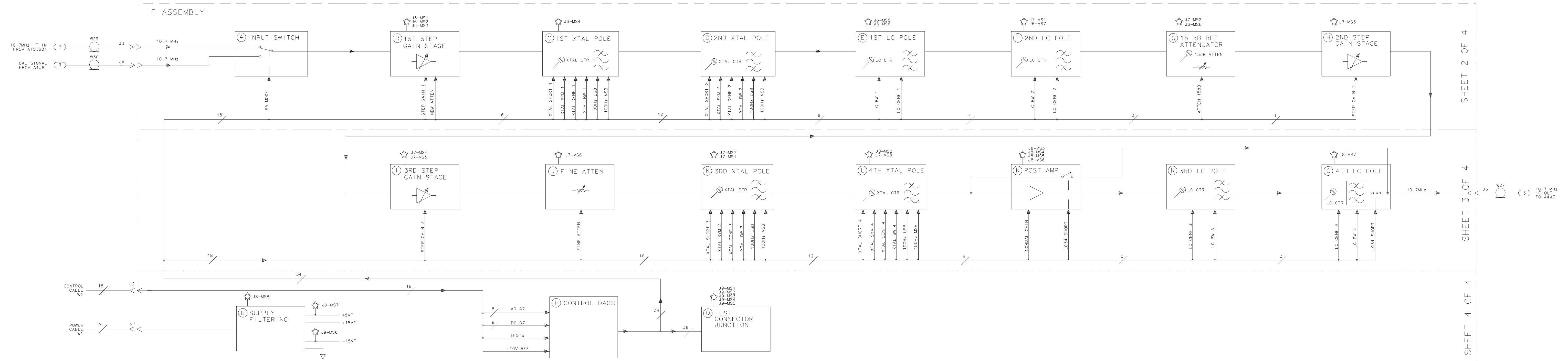
6. If the audio is not working correctly, monitor the signal at A4U704 pin 3 with an oscilloscope. The signal should be 20 mV peak-to-peak ±25 percent (with +2.5 V of dc bias). If the signal measures outside these limits, the fault is prior to the audio amplifier (block T).

7. If the signal is correct, troubleshoot the audio amplifier and speaker.

A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM

A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM

CAL OSCILLATOR

s1139e

FIGURE 9-21. A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM (2 of 2)

A5 IF ASSEMBLY BLOCK DIAGRAM

IF ASSEMBLY

10.7MHz IF IN FROM A15J601

CAL SIGNAL FROM A4J8

W29 J3 10.7 MHz
W30 J4 10.7 MHz

A INPUT SWITCH

B 1ST STEP GAIN STAGE

C 1ST XTAL POLE XTAL CTR

D 2ND XTAL POLE XTAL CTR

E 1ST LC POLE LC CTR

F 2ND LC POLE LC CTR

G 15 dB REF ATTENUATOR 15dB ATTEN

H 2ND STEP GAIN STAGE

I 3RD STEP GAIN STAGE

J FINE ATTEN

K 3RD XTAL POLE XTAL CTR

L 4TH XTAL POLE XTAL CTR

K POST AMP

N 3RD LC POLE LC CTR

O 4TH LC POLE LC CTR

W27 J5 10.7 MHz IF OUT TO A4J3

R SUPPLY FILTERING

P CONTROL DACS

Q TEST CONNECTOR JUNCTION

CONTROL CABLE W2 J2

POWER CABLE W1 J1

SHEET 2 OF 4
SHEET 3 OF 4
SHEET 4 OF 4

sl140e

FIGURE 9-22. A5 IF ASSEMBLY BLOCK DIAGRAM

10 Controller Section

Introduction

The controller section includes the A2 controller assembly, A19 GPIB assembly, and BT1 battery. The presence of a display (graticule and annotation) verifies that most of A2 controller assembly is operating properly.

NOTE   When measuring voltages or waveforms, make ground connections to A2TP3. The metal board-standoffs are not grounded and should not be used when taking measurements.

Troubleshooting Using the TAM (8562E)

Refer to Chapter 7 , "General Troubleshooting," for information on enabling the TAM for use with the 8562E Spectrum Analyzer.

Table 10-1 on page 495 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 10-1 on page 496 illustrates the location of the A2 test connectors.

Table 10-1   **TAM Tests versus Test Connectors**

| Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A2J11	ADC/MUX Test	MS1, MS3 through MS6, MS8
	DAC test	MS2, MS7, OS1
A2J201	10 volt reference test	MS4
	Switch drive test	MS8
	Buffered X &Y DAC outputs	MS2, MS7
	X line generator test	MS6
	Y line generator test	MS1
	Intensity offset output	MS3
A2J202	Revision	MS1
	X, Y, &Z Output Offset	MS3, MS4, MS7
	X output amplifier	MS7
	Y output amplifier	MS3
	Blanking test	MS8
	Focus DAC test	MS2

Blank Display

Use the following procedure if the instrument display is blank. This procedure substitutes a GPIB printer for the display.

1. Connect the printer to the spectrum analyzer and set the printer address to the value required by the TAM. This is usually 1.

2. All of the power-supply indicator LEDs along the edge of the A2 controller assembly should be lit.

3. The rear-panel CRT +110 VDC ON indicator might not be lit, even if the +110 V is present.

4. Connect the TAM probe cable to A2J11.

5. Press **MODULE**, **SOFT KEY #3**, ⇓, **SOFTKEY #1**. (The top softkey is #1.)

6. The yellow LED next to A2J11 should blink approximately ten times. If the LED fails to blink correctly, troubleshoot the digital section of the A2 controller assembly.

7. Move the probe cable to A2J202. Press **SOFT KEY #1** and wait 5 seconds.

8. Press **SOFT KEY #4**. The results should be sent to the printer.

9. If a failure is indicated in any of these tests, the fault lies on the A2 controller assembly. To obtain more information:

   a. Press the step down key, ⇓ one less time than the test number. (For example, press it twice for the third test on the list.)

   b. Press **SOFT KEY #3**, then **SOFT KEY #4**, and when the printout is complete, **SOFT KEY #6**.

Figure 10-1   A2 Test Connectors
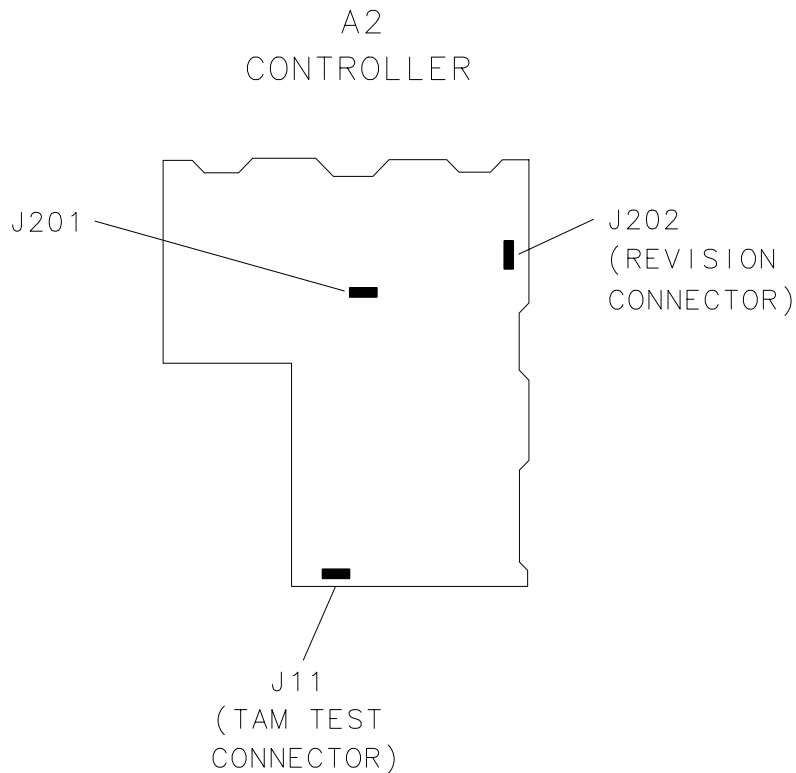
10. Move the probe cable to A2J201, press **SOFT KEY #1** and wait
    5 seconds.

11. Press **SOFT KEY #4**. The results will be sent to the printer. Follow the
    procedure in step 9 to obtain more information on any of the tests.

12. If no failures were indicated in testing the A2 controller, move the
    probe cable to A17J4.

13. Press **SOFT KEY #1** and wait 5 seconds.

14. Press **SOFT KEY #4**. The results will be sent to the printer.

15. If no failure is indicated in the printout, refer to "High Voltage
    Supplies (8562E)" on page 657.

Digital Signature Analysis –DSA (8562E)

Digital signature analysis (DSA) places microprocessor, A2U1, in a simplified known state. This simplified state consists of placing a one-word instruction, MOVE QUICK, (0111 XX10 XXXX XXX0) on the data bus. The microprocessor cycles through its address range continually reading the instruction. Perform the following DSA procedure to test the operation of microprocessor, A2U1:

1. Press **LINE** to turn the spectrum analyzer off.

2. Move the DSA jumper on J13 (located in the middle of the A2 assembly) from the DISable position to the ENAble position.

3. Remove jumper A2E1. A2E1 is a 16 pin dual-in-line package located in the middle of the A2 Assembly. Press **LINE** to turn the spectrum analyzer on.

4. Use an oscilloscope to confirm that address lines, address strobe, and chip selects are toggling at proper levels.

5. Use an oscilloscope to check the address line sequencing. The signal on each line (starting with A1 and ending with A23) should be one-half the frequency of the previous line.

6. If step 4 reveals problems, microprocessor A2U1 is probably faulty.

7. Press **LINE** to turn the spectrum analyzer off. Replace jumper A2E1. Move the DSA jumper from connecting E5 and E6 back to connecting E6 and E7.

Display Problems (8562E)

Line Generators

Refer to function blocks D and I of A2 controller schematic diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information.*

The line generators convert the digital display information to an analog output suitable to drive the A17 CRT driver assembly. These circuits change the digital words into vectors, or lines, which move the beam of the CRT. The vectors are each 6 μs long (width of the INTEGRATE pulse) followed by a 1 μs SAMPLE pulse. When characters of text are being drawn, the vectors are 3 μs long.

1. On the spectrum analyzer, press **PRESET**.

2. On the spectrum analyzer, press **CAL MORE CRT ADJ PATTERN**. If the display is blank, press the bottom softkey and then the top softkey.

3. Set an oscilloscope to the following settings:

   Amplitude scale ....3 V/div
   Sweep time .... 1 ms/div
   Triggering ....External

4. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

5. Compare the signals at the following test points with those illustrated in Figure 10-2 on page 500.

   X POS: A2J202 pin 14

   Y POS: A2J202 pin 3

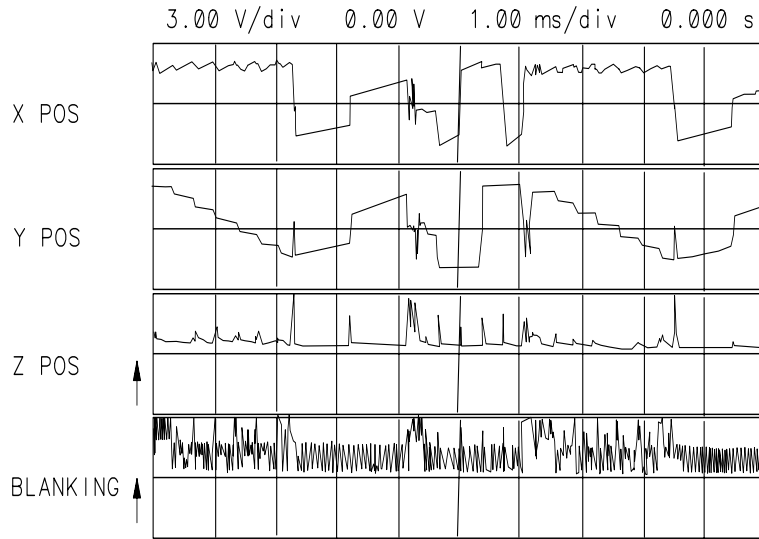   Z OUT: A2J201 pin 3

   BLANKING: A2J202 pin 15

NOTE   Waveforms displayed on an analog scope may show considerably more spikes. This is normal and is due to the wider displayed bandwidth.

6. Troubleshoot the circuits associated with any bad waveforms.

Figure 10-2   **Line Generator Output Waveforms**

3.00 V/div   0.00 V   1.00 ms/div   0.000 s

X POS

Y POS

Z POS

BLANKING

SK19

Blanking

Refer to function block J of A2 Controller Schematic Diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Using an oscilloscope, check for blanking pulses at A2J202 pin 15. A2U206 pin 6 should be at a TTL high. Blanking pulses turn the CRT beam off during the sample time of the line generators and when moving the CRT beam to a new position for drawing the next vector.

2. Set an oscilloscope to the following settings:

    Amplitude scale ....4 V/div
    Amplitude offset ....+2.5 V
    Sweep time .... 20 µs/div
   Triggering ....External

3. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

4. Compare the blanking-circuit input signals at the following test points with those illustrated in .

    BLANKING: J202 pin 15

    BLANK: U214 pin 12

    VECTOR: U214 pin 11

                      U213 pin 13

5. The waveforms in Figure 10-3 on page 501 must match the timing of the vectors being drawn. To do this, U215B is used to adjust the leading edge, and U215A is used to adjust the trailing edge. The first six horizontal divisions show the line drawing mode where the VECTOR pulses are 6 µs apart. The remaining divisions shows character mode (VECTOR pulses 3 µs apart). The BLANK pulses are synchronized to the VECTOR pulses by U214B. The fourth trace shows the double pulses which delay the leading and trailing edges of the blanking pulses.

6. Set the oscilloscope to the following settings to expand the first and fourth traces. This displays how the rising edges of U213-13 determine the transitions of the blanking pulses. See Figure 10-4 on page 502.
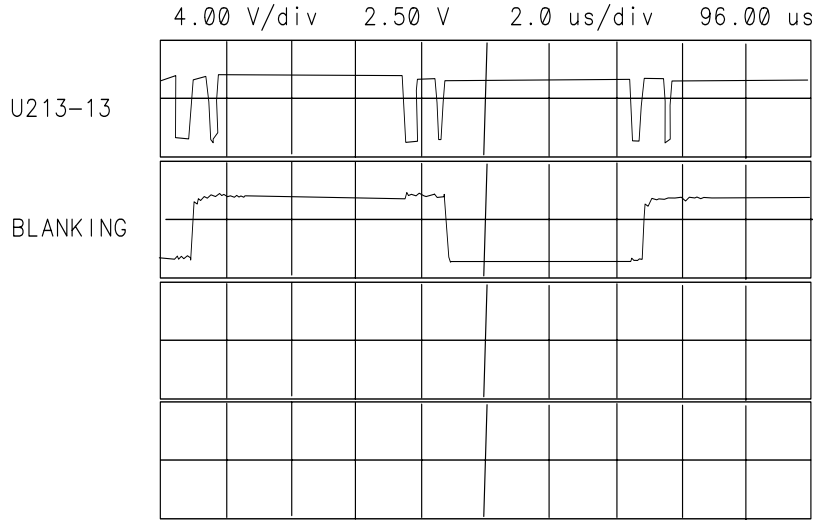
Amplitude scale ....4 V/div
Amplitude offset ....+2.5 V
Sweep time .... 2 µs/div
Delay from trigger ....96 µs
Triggering ....External

Figure 10-3   Blanking Waveforms
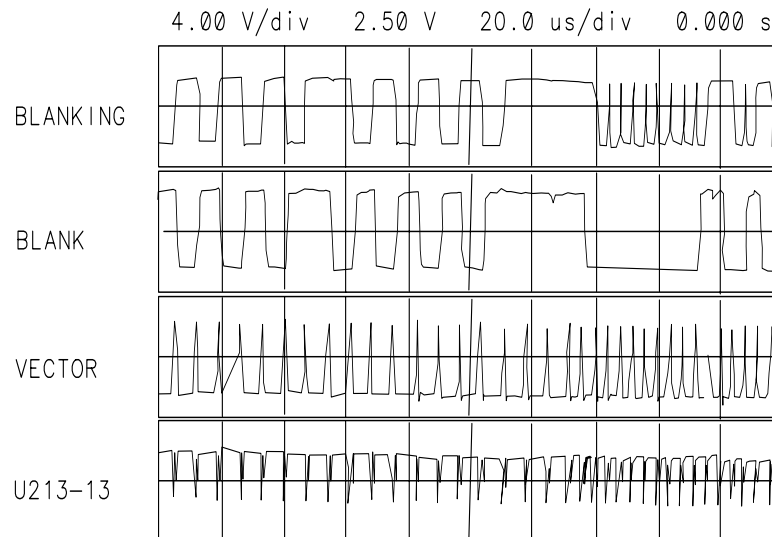
SK192

Figure 10-4   **Expanded Blanking Waveforms**

Display Jumbled or Trace Off Screen

Refer to function blocks D and I of A2 controller schematic diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information.*

The two line generators are identical circuits, so the following steps apply to both. The X generator is referenced below, with Y generator references in parentheses.

1. The voltage at A2U202B pin 7 should measure 10.0 V.

2. Perform steps 1 through 5 of "Line Generators" on page 499. If the X POS and Y POS waveforms look different from those illustrated in Figure 10-2 on page 500, check the waveforms at the low-pass filter input (function block E in the component-level information binder).

3. The waveform at the low-pass filter should look like X POS in Figure 10-2 on page 500 but have an amplitude from 0 V to +5 V.

4. If the waveform in step 3 is incorrect, set an oscilloscope to the following settings:

    Amplitude scale ....10 V/div
    Sweep time .... 20 μs/div
    Triggering ....External

5. Trigger the oscilloscope on the signal at U207 pin 8 (LBRIGHT).

6. Compare the line-generator input signals at the following test points with those illustrated in Figure 10-5 on page 503. INTEGRATE and SAMPLE waveforms are replicas of VECTOR except for polarity and amplitude. LCHAR is low when characters are drawn.

INTEGRATE: Q202 collector

SAMPLE: Q201 collector

LCHAR: U207 pin 9

VECTOR: U213 Pin 9

Figure 10-5   Switch Driver Waveform LCHAR
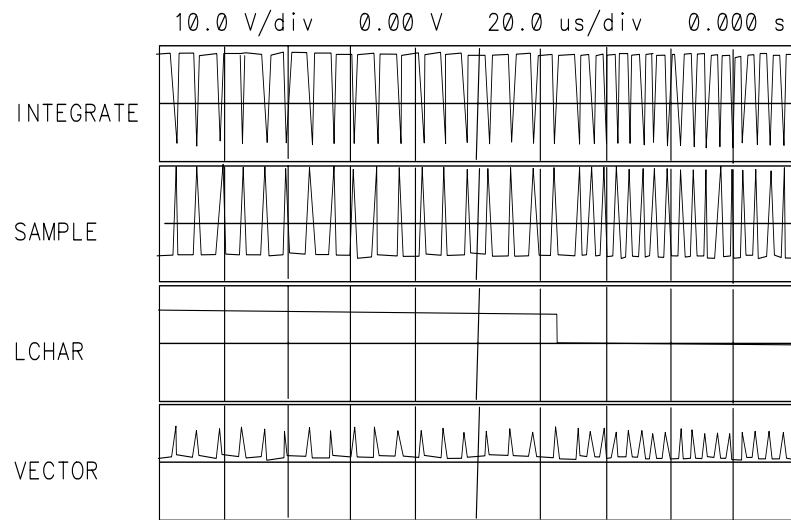
SK194

7. All of the DAC inputs should change state two or more times within a 5 ms window. If one or more DAC bits are not working correctly, this will effect the entire display, especially the diagonal lines that go from lower left to upper right. When these lines are drawn, both the X and Y DACs are stepped one count at a time. A "stuck" bit will distort the diagonal in a repetitive manner. The quicker the repetition, the less significant the "stuck" bit. Horizontal distortions apply to the X LINE GENERATOR DAC, while vertical distortions apply to the Y LINE GENERATOR DAC. The DACS have current outputs so they are not readily observable with an oscilloscope. Continue with step **8** to observe the DAC outputs.

8. To break the effect of feedback in the line generators and to observe the output of the DACs, short J201 pin 13 (J201 pin 1) to TP3 (GND) to observe U201 pin 1 and TP2 (U203 pin 1 and TP1.) Continue with step 9.

9. Set an oscilloscope to the following settings:

     Amplitude scale ....5 V/div
     Sweep time .... 1 ms/div
     Coupling .... AC
     Triggering ....External

10. Trigger the oscilloscope on the signal at U207 pin 8 (LBRIGHT).

11. The following waveforms should look like
     on the oscilloscope. The top two traces are for the X line generator
     and the bottom two traces for the Y line generator.

     X line generator

     — U201 pin 1

     — TP2

     Y line generator

     — U203 pin 1

     — TP1

12. illustrates the waveforms in step 11
     expanded to show relative timing. the second and fourth traces are
     delayed by 5 ms from the first and third. The oscilloscope settings
   are changed as follows:

     Sweep time .... 20 μs/div

13. illustrates the waveforms of properly
     working line generators. Whenever there is a pulse on TP2 (or TP1),
     the appropriate integrator U201B (or U203B) generates a ramp (the
     output vector) which feeds back to U201A (U203A) and shows on its
     output.

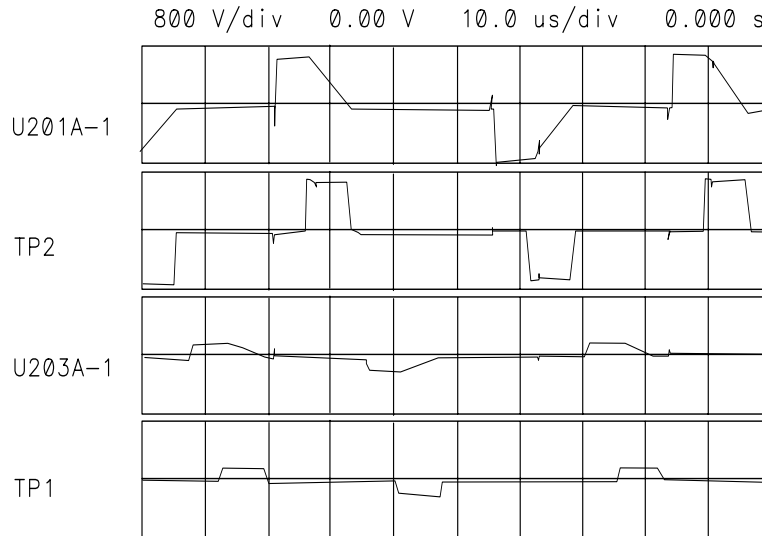**Figure 10-6   Distorted X/Y Line Generator Waveforms**
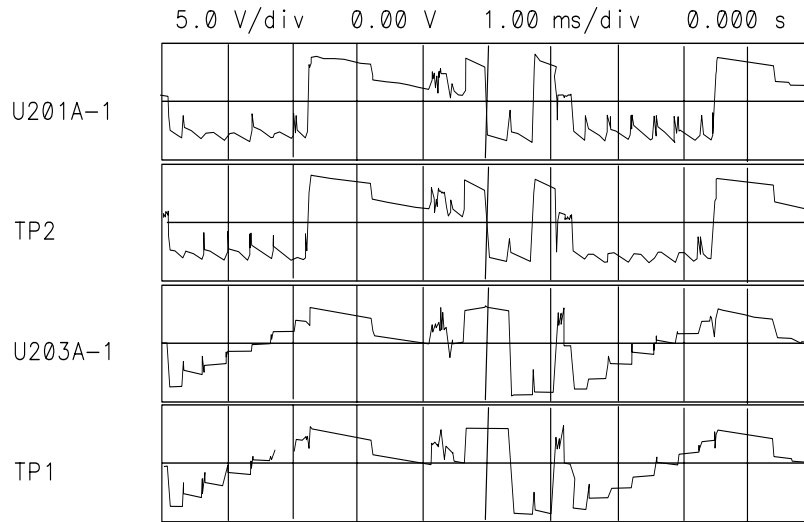
SK195

Figure 10-7   Expanded X/Y Line Generator Waveforms
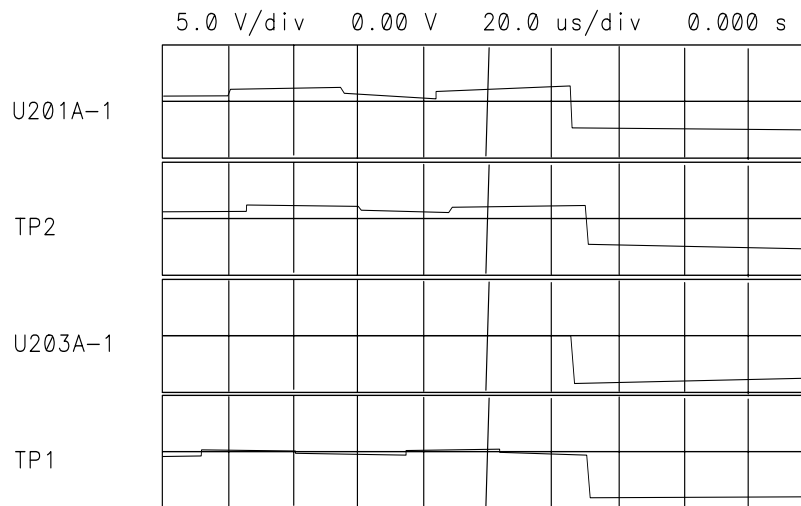
SK196

Figure 10-8   **Normal X/Y Line Generator Waveforms**

SK197

Intensity

1. The length of the vector being drawn can effect intensity. U210A, U210C, and U210D sum the lengths of the X and Y vectors. Refer to "Long Lines Dimmer Than Short Lines" on page 507.

2. Short A2U207 pin 6 to pin 7. If the display does not brighten, troubleshoot LBRIGHT switch, U207B. This switch intensifies trace A and active softkeys.

3. Short A2U207 pin 2 to pin 3. If the display does not brighten, troubleshoot DEF1 switch, U207A. This switch is used in analog zero-span.

4. Change the intensity (under **DISPLAY**). If the intensity does not change, troubleshoot the intensity DAC, A2U212A. (A2U212A is controlled from the front panel.) The amplitude of the waveform at U211A pin 1 should increase or decrease with intensity changes.

5. Clamp U211B limits the voltage to about 4.2 V. Short A2J201-1 to ground and set the intensity DAC to a number greater than 80. A major portion of the waveform should be limited to 4.2 V.

6. If a major portion of the waveform is not limited to 4.2 V, troubleshoot the maximum brightness clamp, A2U211C.

Bad Characters or Graticule

If the displayed characters are bad but the graticule is correct (or if the symptoms are reversed), troubleshoot the X- and Y- generator switches A2U207D and A2U207C. Check that the switch driver signal LCHAR is working properly. Refer to "Display Jumbled or Trace Off Screen" on page 502.

Long Lines Dimmer Than Short Lines

Refer to function block M of A2 controller schematic diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The Z output function block contains the absolute value circuits which determine the intensity of vectors drawn on the display. The vector length is approximated by the sum of the X length and Y length. The voltage corresponding to the X length, ΔX, is converted to current by R274. If the voltage is negative, it is amplified by 2 in A2U210C, converted to current by A2R246, and added to the current from A2R274. This effectively turns both negative and positive voltages into positive currents, hence absolute value.

1. Short A2J201 pin 13 to ground (A2TP3).

2. Connect channel A of an oscilloscope to A2J201 pin 2. Connect channel B to A2U210D-14.

3. Set an oscilloscope to the following settings:

   Amplitude scale ....10 V/div
   Sweep time .... 1 ms/div
   Triggering ....External

4. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

5. The waveforms should look like those illustrated in Figure 10-9 on page 508. If the waveform at J201 pin 2 is bad, troubleshoot the X line generator (function block D of the A2 controller schematic, sheet 1 of 4).

6. If the waveform at U210D pin 14 is bad, troubleshoot the Z output circuit (function block M of A2 controller schematic, sheet 1 of 4).

7. Remove the short from J201 pin 13 to ground. Short A2J201 pin 1 to ground.

Figure 10-9   **Delta X Waveform**

```
           10.0 V/div    0.00 V    1.00 ms/div    0.000 s

  J201-2


  U210D-14
```
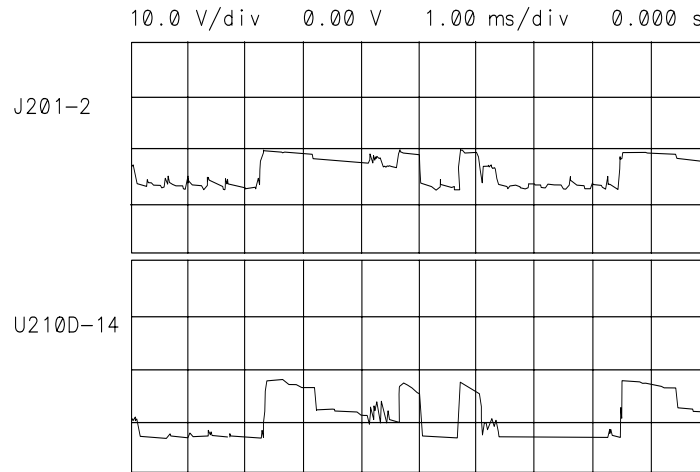
                                                                SK198

8. Move the oscilloscope channel A probe to J201 pin 14.

9. The waveforms should look like those illustrated in Figure 10-10 on page 508. If the waveform at J201 pin 14 is bad, troubleshoot the Y line generator (function block I of A2 controller schematic, sheet 1 of 4).

10.If the waveform at U210D pin 14 is bad, troubleshoot the Z output circuit (function block M of A2 controller schematic, sheet 1 of 4).

11.Remove the jumpers.

Figure 10-10   **Delta Y Waveform**

```
           10.0 V/div    0.00 V    1.00 ms/div    0.000 s

  J201-14


  U210D-14
```
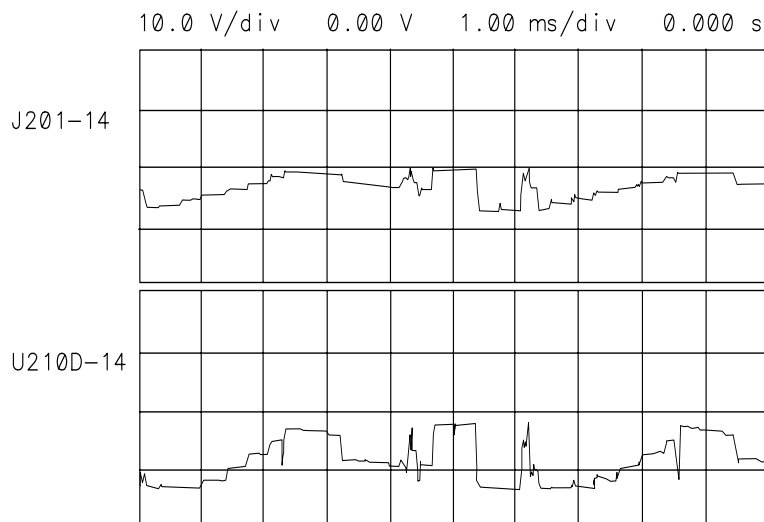
   SK199

Analog Zero-Span Problems (8562E, Non-Option 007)

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **SWEEP**, **1**, **ms**, **CAL**, **MORE**, and **CRT ADJ PATTERN**.

2. Set an oscilloscope to the following settings:

    Amplitude scale ....10 V/div
    Sweep time .... 1 ms/div
    Triggering ....External

3. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

4. The display should be similar to Figure 10-11 on page 509 except that the untriggered trace should show at the left edge of the screen. In these settings, DEF1 causes switching between the line generators and the analog inputs (sweep and video). DEF1 remains high when the CRT adjust pattern is on. Refer to function block M of the A2 controller schematic, 1 of 4.

5. The sweep input from J1-41 should go from 0 V to +10 V; the video In signal should go from about 0 V to 1 V from the bottom to the top of the screen. Apply a dc voltage to A2J4, Video In, to test the circuit.

6. In Figure 10-11 on page 509, there is no synchronization between DEF1 and the video patterns X POS and Y POS when DEF1 is TTL high. The Y POS level when DEF1 is low is the Video In level.

Figure 10-11   **DEF1 Synchronization**
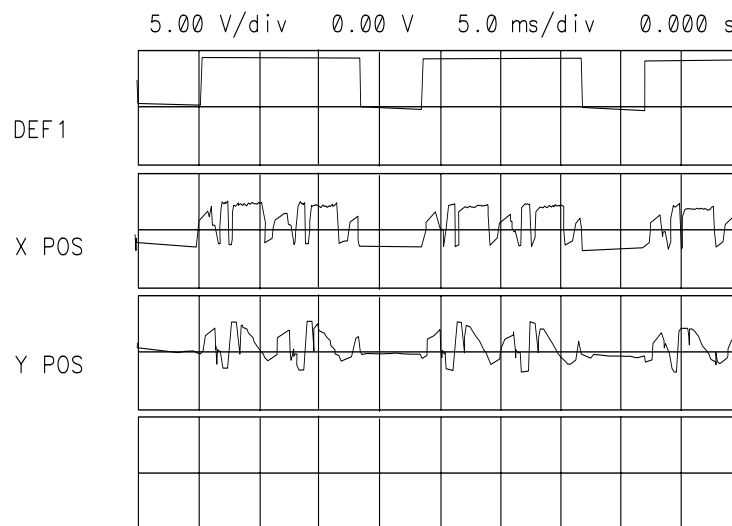
SK1100

Frequency-Count Marker Problems (8562EC)

The FREQ COUNT function works by dividing the 10.7 MHz IF signal by two (prescaling) and counting the divided-down signal using the frequency counter on the A2 controller assembly . The prescaler is on the A4 Log amplifier/cal oscillator assembly . Perform the following steps to determine whether the problem is on the A4 log amplifier/cal oscillator or the A2 controller assembly:

1. Disconnect W53 from A2J13.

2. Connect the output of a synthesized source, such as an 3335A, to A2J13.

3. Set the synthesized source to the following settings:

    Amplitude .... +10 dBm
    Frequency .... 5.35 MHz

4. Set the spectrum analyzer to the following settings:

    Center frequency .... 300 MHz
    Span .... 1 MHz

5. On the spectrum analyzer, press **FREQ COUNT**. The frequency counter actually reads one half the frequency of the 10.7 MHz IF. If the CNT frequency display reads all asterisks, the frequency counter is probably at fault.

6. If a valid frequency is displayed, troubleshoot the prescaler on the A4 log amplifier/cal oscillator assembly.

7. Reconnect W53 to A2J13.

Frequency-Count Marker Problems (8562E)

The FREQ COUNT function works by dividing the 10.7 MHz IF signal by two (prescaling) and counting the divided-down signal using the frequency counter on the A2 controller assembly (block Z of the A2 schematic diagram). The prescaler is on the A4 Log amplifier/cal oscillator assembly (block Q of the A4 schematic diagram). Perform the following steps to determine whether the problem is on the A4 log amplifier/cal oscillator or A2 controller assembly:

1. Disconnect W53 from A2J7.

2. Connect the output of a synthesized source, such as an 3335A, to A2J7.

3. Set the synthesized source to the following settings:

   Amplitude .... +10 dBm
   Frequency .... 5.35 MHz

4. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 1 MHz

5. On the spectrum analyzer, press **FREQ COUNT**. The frequency counter actually reads one half the frequency of the 10.7 MHz IF. If the CNT frequency display reads all asterisks, the frequency counter is probably at fault.

6. If a valid frequency is displayed, troubleshoot the prescaler on the A4 log amplifier/cal oscillator assembly.

7. Reconnect W53 to A2J7.

Frequency Counter (8562EC)

The frequency counter counts the frequency of the last IF and provides accurate timing signals for digital zero-spans. The circuit also provides timing signals to the ADC (analog to digital converter) on the A3 interface assembly. The nominal input frequency is 5.35 MHz (10.7 MHz divided by 2). The 10 MHz reference from the A15 RF assembly provides the frequency reference in the frequency count mode. The frequency reference in digitized zero spans (sweep times ≥30 ms) is the 4 MHz GPIB_CLK, selected by a clock select multiplexer in U35.

The 10 MHz reference from the A15 RF assembly is first filtered and passed through a comparator to generate a TTL, 50 percent duty cycle signal. C128, L16, and R91 provide a bandpass filter centered at 10 MHz. The output of comparator U33B is the actual reference used for the Frequency Counter. An additional stage of filtering is performed on this signal to provide a 10 MHz signal for the A17 LCD Driver assembly.

In the frequency count mode, the 10 MHz reference is prescaled by 5 to generate a 2 MHz timebase. This timebase feeds through the clock select multiplexer in U35 to the CLK2 input of programmable timer U15. The output (OUT2) of programmable timer U15 is the gating signal (HBKT_PULSE); it performs the frequency count. The gating time interval is a function of the counter resolution which may be set between 10 Hz and 1 MHz. Table 10-2 on page 513 lists the gate time for each setting of COUNTER RES. The gate time is the period during which HBKT_PULSE (pin 20 of U15) is low.

The FREQ COUNT input, A2J13, is gated by HBKT_PULSE. The gated signal clocks divide-by-16 counters within U35. These counters are cascaded to form a divide-by-256 counter. The MSB of this counter, CD7, clocks the CLK0 input of U15. The frequency of CD7 is a function of COUNTER RES as shown in Table 10-2 on page 513. If timer U15 overflows, OUT0 will be set, generating CNTOVFLIRQ, which will interrupt the CPU.

If IRQAK2 is high, HBKT_PULSE will generate FREQCNTLIRQ. Upon receiving the FREQCNTLIRQ interrupt, the CPU latches the CD0 to CD7 onto the BID bus by setting LCDRD (low counter data read) low and reading the counter data from the BID bus. The CPU will also read the data from the timer, U15, by setting L8254CS and LCNTLRD low, placing the timer data on the BID bus. The CPU then resets IRQAK2 low.

Table 10-2   **Gate Times**

Counter Res	Gate Time* (U15 pin 20 low state)	A2TP16	A2TP15
10 Hz	200 ms	2 MHz	4.18 kHz
100 Hz	20 ms	2 MHz	418 Hz
1 kHz	2 ms	2 MHz	41.8 Hz
10 kHz	2 ms	2 MHz	41.8 Hz
100 kHz	2 ms	2 MHz	41.8 Hz
1 MHz	2 ms	2 MHz	41.8 Hz
* U15 pin 10 = (FREQ COUNT input $\times$ Gate Time)/256			

1. Disconnect W22 from A2J9.

2. If a 10 MHz, TTL-level signal is not present at the end of W22, continue with step 3. If a 10 MHz signal is present at W22, proceed as follows:

   a. Reconnect W22 to A2J9.

   b. Set the spectrum analyzer to the following settings:

      Span .... Zero Span
      Sweep time .... 20 ms

   c. Monitor the signal at A2J2 pin 21. This is an output of the frequency counter, HBUCKET PULSE.

   d. If HBUCKET PULSE is stuck high, troubleshoot the frequency counter.

3. Check for a 10 MHz signal at A15J302. If the signal is not present at A15J302, the A15 RF assembly is probably defective.

Frequency Counter (8562E)

See function block Z of A2 schematic diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information.*

The frequency counter counts the frequency of the last IF and provides accurate timing signals for digital zero-spans. The circuit also provides timing signals to the A3 interface assembly ADC (analog to digital converter). The nominal input frequency is 5.35 MHz (10.7 MHz divided by 2). The circuit frequency reference in the frequency count mode is the 10 MHz reference from the A15 RF assembly. The frequency reference in digitized zero spans (sweep times $\geq$30 ms) is the 4 MHz GPIB_CLK, selected by MUX U704.

In the frequency count mode, U702 prescales the 10 MHz reference by 5 to generate a 2 MHz timebase. This timebase feeds through MUX U704 to programmable-timer U700 CLK2 input. Programmable-timer U700 output (OUT2) is the gating signal (HBKT_PULSE) for performing the frequency count. The gating time interval is a function of the counter resolution which may be set between 10 Hz and 1 MHz. Table 10-2 on page 513 lists the gate time for each setting of COUNTER RES. The gate time is the period during which U511 pin 3 is high.

The FREQ COUNT input, A2J7, is gated in U511B by HBKT_PULSE. The gated signal clocks divide-by-16 counters U703A and U703B. These counters are cascaded to form a divide-by-256 counter. The MSB of this counter, CD7, clocks the CLK0 input of U700. The frequency of CD7 is a function of COUNTER RES as shown in Table 10-2 on page 513. If timer U700 overflows, OUT0 will be set and U701B clocked, generating CNTOVFLIRQ, which will interrupt the CPU.

If IRQAK2 is high, HBKT_PULSE will clock U701A, generating FREQCNTLIRQ. Upon receiving the FREQCNTLIRQ interrupt, the CPU latches the CD0 to CD7 onto the BID bus by setting LCDRD (low counter data read) low and reading the counter data from the BID bus. The CPU will also read the data from the timer, U700, by setting L8254CS and LCNTLRD low, placing the timer data on the BID bus. The CPU resets U701A by setting IRQAK2 low via the BID bus and latch U506.

Table 10-3   **Gate Times**

Counter Res	Gate Time* (U511 pin 3 high state)	A2TP16	A2TP15
10 Hz	200 ms	2 MHz	4.18 kHz
100 Hz	20 ms	2 MHz	418 Hz
1 kHz	2 ms	2 MHz	41.8 Hz
10 kHz	2 ms	2 MHz	41.8 Hz
100 kHz	2 ms	2 MHz	41.8 Hz
1 MHz	2 ms	2 MHz	41.8 Hz
* TP15 = (FREQ COUNT input × Gate Time)/256			

1. Disconnect W22 from A2J8.

2. If a 10 MHz, TTL-level signal is not present at the end of W22, continue with step 3. If a 10 MHz signal is present at W22, proceed as follows:

   a. Reconnect W22 to A2J8.

   b. Set the spectrum analyzer to the following settings:

      Span .... Zero Span
      Sweep time .... 20 ms

   c. Monitor the signal at A2J2 pin 21. This is an output of the frequency counter, HBUCKET PULSE.

   d. If HBUCKET PULSE is stuck high, troubleshoot the frequency counter.

3. Check for a 10 MHz signal at A15J302. If the signal is not present at A15J302, the A15 RF assembly is probably defective.

Video Input Scaling Amplifiers and Limiter (8562EC)

The video input scaling amplifiers help provide scaling (10 dB/div, 5 dB/div, 2 dB/div, or 1 dB/div) and buffer the flash video output. When the GAINX2 control line is low, switch U44D is open and switch U44C is closed. Thus, the scaled video at TP26 virtually follows the video input (0 - 1 V). When the GAINX2 control line is high, switch U44C is open and switch U44D is closed. Amplifier U43 then provides a gain of $2(V_{in}) -1$ V. Voltage clamp CR4 prevents the scaled video input to amplifier U45 from going more negative than –0.35 V or more positive than +1.25 V.

NOTE

When measuring voltages or waveforms on the Fast ADC section of the A2 controller assembly, connect the ground (or common) lead to the ground-plane trace associated with the shield. This digital ground plane is totally isolated from the chassis.

1. Press **PRESET** on the 8560 EC-series spectrum analyzer and set the controls as follows:

Center frequency	300 MHz
Span	0 Hz
Reference level	–10 dBm
Log/division	10 dB/DIV
Sweep time	20 ms

2. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Adjust the spectrum analyzer reference level to place the signal at the top graticule line on the LCD display.

4. Measure the dc level at pin 3 of U10. If the voltage measured is not +1.0 ±0.15 V, troubleshoot the A3 interface assembly.

5. Measure the dc level at pin 3 of U17. The level should be approximately the same as the level measured at pin 3 of U10. If not, suspect switch U9.

6. Set the spectrum analyzer scale to 5dB per division.

7. Adjust the spectrum analyzer reference level to place the signal at the top graticule line on the LCD display.

8. Measure the dc level at pin 3 of U10 and pin 3 of U17. The level should be +1.0 ±0.25 V. If the level measured at pin 3 of U17 differs from the level measured at pin 3 of U10 by more than 0.25 volts, troubleshoot U10 and associated circuitry.

9. Disconnect the CAL OUTPUT signal from the INPUT 50Ω connector.

10. The level at pin 3 of U10 should drop to –0.35 Vdc. If the level is less (more negative) than –0.35 Vdc, replace voltage clamp D3.

11. Measure the dc level of the flash video at pin 2 of R47. The level should be near 0 Vdc with the signal at the bottom graticule line (no input to the spectrum analyzer).

12. Connect the CAL OUTPUT to the INPUT 50Ω connector.

13. Measure the dc level of the flash video at pin 2 of R47. The level should be near +1.7 Vdc.

12-Bit Flash ADC (8562EC)

The flash ADC (U22) converts the analog video signal into 12-bit digital values at a fixed rate of 12 megasamples per second.

When measuring voltages or waveforms on the Fast ADC of the A2 controller assembly, connect the ground (or common) lead to the ground-plane trace associated with the shield. This digital ground plane is totally isolated from the chassis.

1. Press **PRESET** on the spectrum analyzer and set the controls as follows:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Reference level .... −20 dBm
   Log/division .... 5 dB/DIV
   Sweep time .... 20 ms

2. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Pins 2 through 13 (ADC0-ADC11) of U22 should all be high (logic 1), corresponding to an ADC digital count of 255 for the analog input of +2 volts or greater.

4. Disconnect the CAL OUTPUT signal from the INPUT 50Ω connector.

5. Pins 2 through 13 (ADC0-ADC11) of U22 should all be low (logic 0), corresponding to an ADC digital count of zero for the analog input of 0 volts or less.

32 K-Byte Static RAM (8562EC)

The static RAM stores the ADC samples that are taken when the Fast ADC circuitry is in the "write" mode. When not in the "write" mode, the static RAM is read by the CPU to retrieve the fast ADC data. The 8-bit DFADC bus connects the outputs of latches within U35 to the data port of static RAM U21.

Reference Clock (8562EC)

The reference clock circuitry takes the 8 MHz square wave clock and triples the frequency to 24 MHz. This is accomplished through two stages of filtering of the 8 MHz signal, to extract the third harmonic. The 8 MHz signal is first passed through a high pass filter consisting of C123 and L15. The the signal passes through a bandpass filter centered at 24 MHz, consisting of C106, C08, L13, and R80. The comparator U28B generates a square wave. The signal then passes through a second stage of filtering by using the bandpass filter consisting of C89, C88, L12, and R77. Comparator U28A then regenerates the square wave. A divide-by-two flip flop in U16 divides the 24 MHz signal to create the 12 MHz signal used by the ADC.

16 MHz Harmonic Filter (8562EC)

The 16 MHz Harmonic Filter generates a 16 MHz signal through a series of stages, consisting of a filter and a comparator. The 10 MHz reference signal from the A15 RF assembly is first prescaled by 2.5 to yield a 4 MHz signal with a 20 percent duty cycle. This prescaling is performed within U35. The 4 MHz signal is then passed, first, through a high pass filter, and then, through a bandpass filter at 16 MHz. The high pass filter consists of R85, C122, and L14. The bandpass filter consists of L19 and C139. The filter basically filters the fourth harmonic of the 4 MHz signal to generate a 16 MHz signal. The resulting signal is then passed through comparator U34A to generate a 16 MHz square wave. Three more stages, consisting of a bandpass filter followed by a comparator, further filter the signal so that a clean 16 MHz signal results. The 16 MHz signal which is the result of these successive stages of filtering is output at pin 10 of U34. U35 buffers this signal to provide the 16 MHz clock for the CPU. In addition, divide-by-two flip flops are located within U35, which generate 8 MHz and 4 MHz signals.

State- and Trace-Storage Problems

State storage is in the two of the four Program RAMs and trace storage is in the two display RAMs. With low battery voltage, it is normal for states and traces to be retained if the power is off for less than 1 minute. If the power is left off for more than thirty minutes with low battery voltage, the stored states and traces will be lost.

The following steps test battery backup for EC-series instruments:

1. Measure the voltage on W6 at A2J3. If the voltage is less than 2.6 V, check the BT1 battery.

2. If the battery voltage is correct, reconnect W6 to A2J3, turn the analyzer power off and wait 5 minutes.

3. Measure the voltage at A2U19 pin 32and A2U26 pin 32.

4. If the voltage is less than 2.0 Vdc, the RAM power battery-backup circuitry on the A2 controller assembly is probably at fault.

The following steps test battery backup for E-series instruments:

1. Measure the voltage on W6 at A2J10. If the voltage is less than 2.6 V, check the BT1 battery.

2. If the battery voltage is correct, reconnect W6 to A2J10, turn the analyzer power off and wait 5 minutes.

3. Measure the voltage at A2U101 pin 28 and A2U102 pin 28.

4. If the voltage is less than 2.0 Vdc, the RAM power battery-backup circuitry on the A2 controller assembly is probably at fault.

Keyboard Problems

If the analyzer does not respond to keys being pressed or the knob being rotated, the fault could be either on the A3 interface assembly or the A2 controller assembly. To isolate the A2 controller assembly, use the following procedure. This procedure tests the analyzer response over GPIB and the keyboard/RPG interrupt request signal.

1. Enter and run the following BASIC program:

    ```
    10 OUTPUT 718; "IP; SP 1 MHz;"

    20 WAIT 2 ! Wait 2 seconds

    30 OUTPUT 718;"AT 70 DB;"

    40 WAIT 2 ! Wait 2 seconds

    50 OUTPUT 718;"AT 30 DB;"

    60 WAIT 2 ! Wait 2 seconds

    70 OUTPUT 718;"AT 10 DB;"

    80 END
    ```

2. When the program runs, three or four clicks should be heard. This is the A9 input attenuator changing attenuation value.

3. If the display shows the analyzer to be in RMT and the ATTEN value displayed on the LCD (CRT on E-series instruments) changed according to the program, the A2 controller assembly is working properly. Refer to Chapter 8 , "ADC/Interface Section."

4. If there was no response over GPIB, the A2 controller is probably defective. Be sure to also check the A19 GPIB assembly and A19W1.

5. If there was an improper response (for example, the displayed ATTEN value changed but no clicks were heard), the A2 controller is probably working properly.

6. On EC-series instruments, attach a logic probe to A2U35 pin 213. On E-series instruments, attach a logic probe to A2U2 pin 2.

    Look for pulses while pressing a key and rotating the knob (RPG). This is the interrupt request signal for the keyboard and RPG.

7. If the interrupt request signal is always low, troubleshoot the A2 controller assembly.

8. If the interrupt request signal is always high, the fault is on either the A3 interface or A1A1 keyboard assembly.
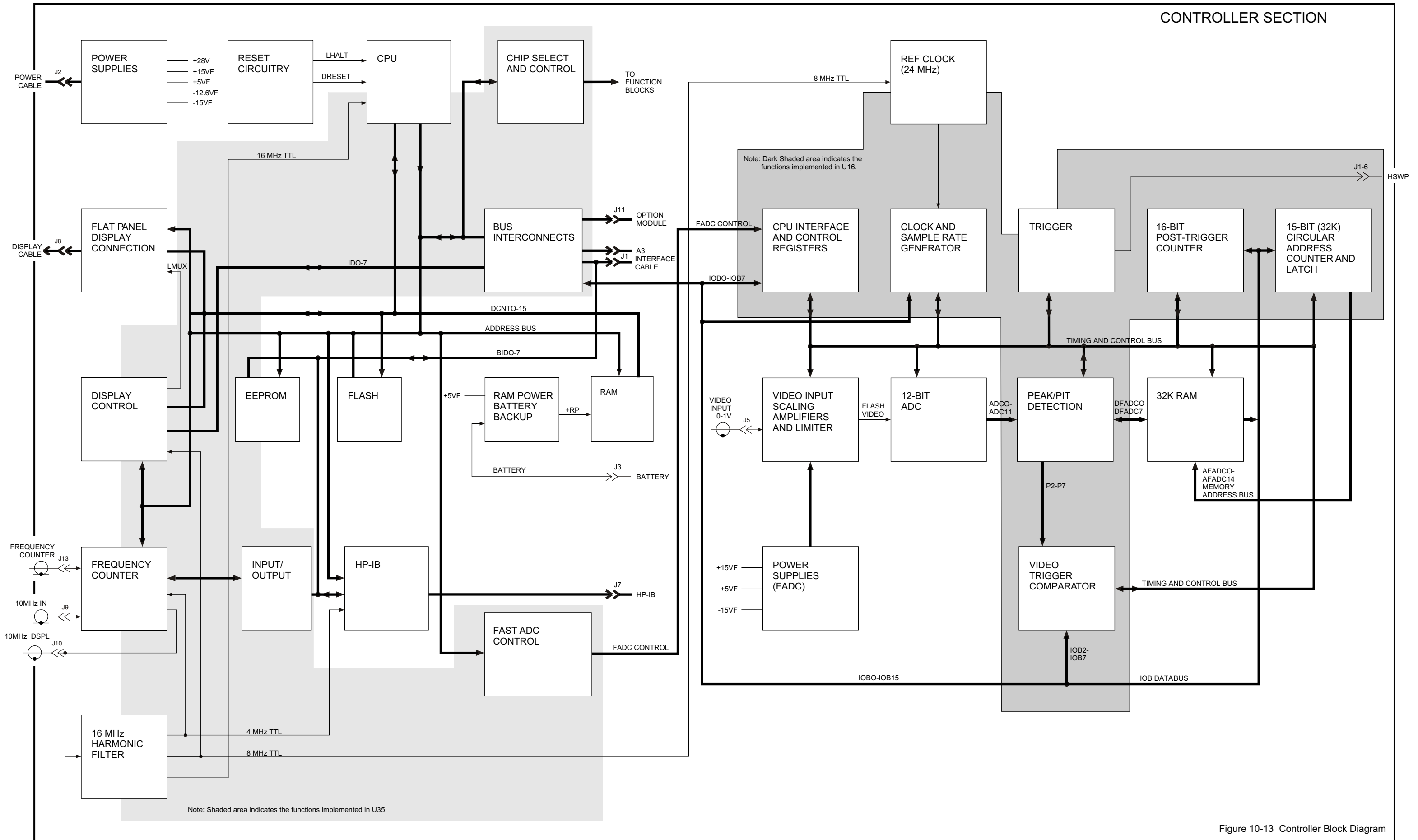
sl141e
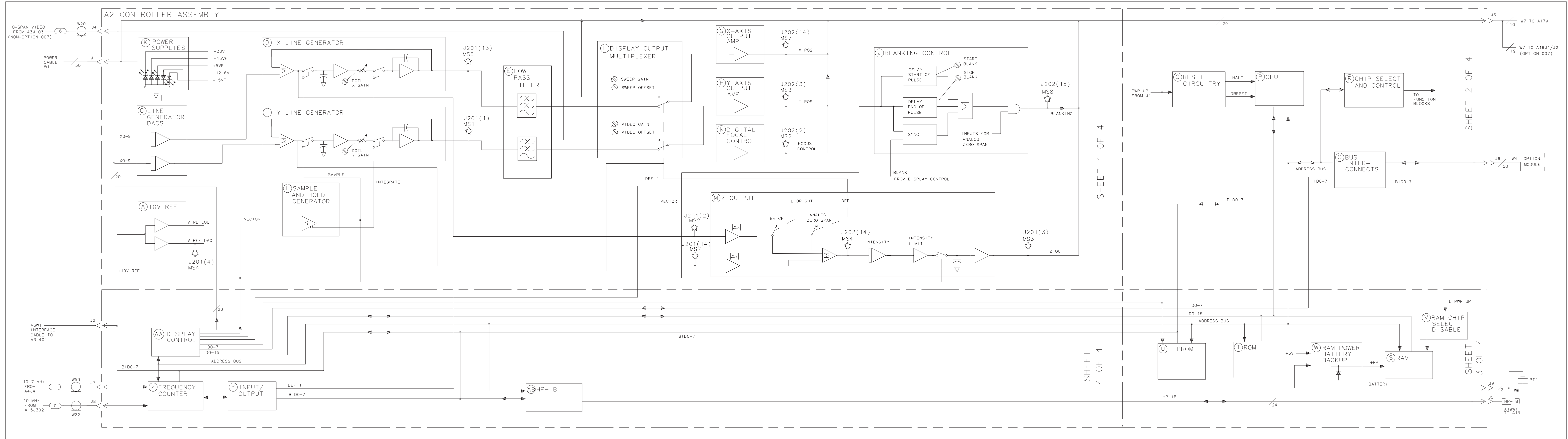
FIGURE 10-12. A2 CONTROLLER BLOCK DIAGRAM

8560 EC-SERIES

Figure 10-13 Controller Block Diagram

sj118c

11   Synthesizer Section

Information

The synthesizer section includes the A7 switched first LO distribution amplifier, the A11 YTO, and parts of the A14 frequency control and A15 RF assemblies. Simplified and detailed block diagrams for each assembly are located at the end of this chapter.

CAUTION

All of the assemblies are extremely sensitive to electrostatic discharge (ESD). For further information regarding electrostatic cautions, refer to "Electrostatic Discharge" on page 32.

CAUTION

Using an active probe, such as an 85024A, with a spectrum analyzer is recommended for troubleshooting the RF circuitry. If an 1120A active probe is being used with a spectrum analyzer, such as the 8566A/B, or 8569A/B having dc coupled inputs, either set the active probe for an ac coupled output or use a dc blocking capacitor (11240B) between the active probe and the spectrum-analyzer input. Some spectrum analyzers can be set to ac coupled. Failure to do this can result in damage to the analyzer or the probe.

Troubleshooting Using the TAM

Refer to Chapter 7 , "General Troubleshooting," for information on enabling the TAM for use with the 8562E/EC Spectrum Analyzer.

When using automatic fault isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 11-2 on page 534 to locate the manual procedure.

Table 11-3 on page 536 lists assembly test connectors associated with each manual probe troubleshooting test. Figure 11-1 on page 533 illustrates the location of A14 and A15 test connectors.
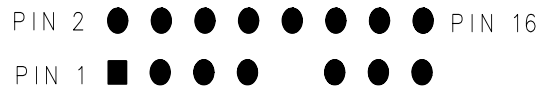
The pin locations of a 16-pin TAM connector are indicated in Figure 11-2 on page 533. Table 11-1 on page 534 indicates the correspondence between a measured signal line and the TAM connector pin.

Figure 11-1 **A14 and A15 Test Connectors**
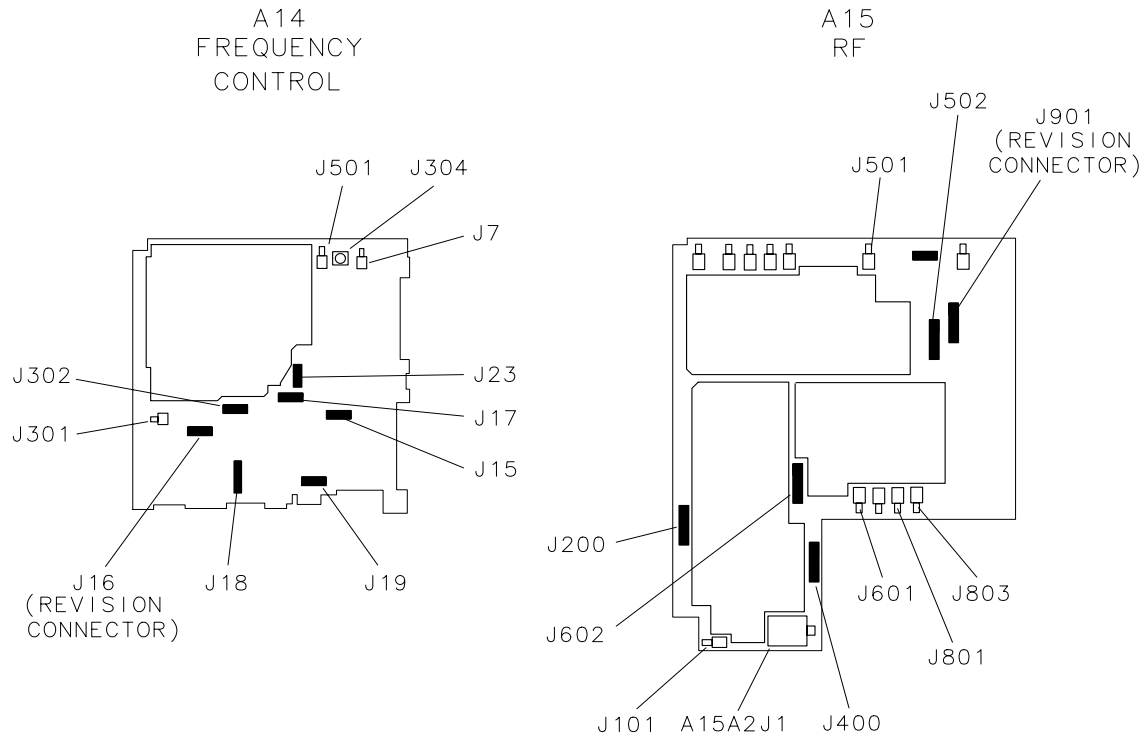
Figure 11-2 **TAM Connector Pin Locations**

Table 11-1 **Measured Signal Line Location**

Measured Signal Line	Connector Pin
MSL1	pin 1
MSL2	pin 2
MSL3	pin 3
MSL4	pin 4
MSL5	pin 5
GND	pin 6
MSL6	pin 13
MSL7	pin 14
MSL8	pin 15

Table 11-2 **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check the YTO loop	Confirming a Faulty Synthesizer Section *(steps 12-33)*
Check first LO	Confirming a Faulty Synthesizer Section *(steps 9-11)*
Check first LO pretune frequency and amplitude	Unlocked YTO PLL *(steps 9-12)*
Check the fractional N oscillator	Unlocked YTO PLL *(steps 13-17)*
Check 3rd LO drive	Third LO Driver Amplifier *(steps 1-6)*
Check 10 MHz reference to phase/frequency detector	Unlocked Reference PLL *(steps 8-13)*
Check for 10 MHz signal at other input to phase/frequency detector	Unlocked Reference PLL *(steps 12 and 13)*
Check A3 ADC MUX function block	Confirming a Faulty Synthesizer Section *(steps 1-4)*
Check A14 frequency control assembly	Confirming a Faulty Synthesizer Section *(steps 12-18)*
Check A14J301 10 MHz REF input	Confirming a Faulty Synthesizer Section *(steps 5-8)*
Check A15 RF assembly	Confirming a Faulty Synthesizer Section *(steps 18-25)*

Table 11-2   **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check current source U307	First LO Span Problems (All Spans) *(steps 14-21)*
Check FM loop sense	Unlocked YTO PLL *(steps 27-34)*
Check YTF gain and offset DACs	YTF Driver Circuit *(steps 10-23)*
Check level at amplifier Input	Third LO Driver Amplifier *(steps 1-6)*
Check levels into mixer U400	Unlocked Offset PLL *(steps 3-13)*
Check loop references	Unlocked Offset PLL *(steps 1 and 2)*
Check main coil tune DAC	Unlocked YTO PLL *(steps 45-49)*
Check main coil coarse and fine DACs	Unlocked YTO PLL *(steps 41-44)*
Check offset span accuracy	First LO Span Problems ≤ 2 MHz *(step 8)*
Check phase/frequency detector	Unlocked Reference PLL *(steps 17-22)*
Check path to phase/frequency detector	Unlocked Offset PLL *(steps 3-7, 14-19)*
Check sampler drive output of A7	Unlocked YTO PLL *(steps 18-21)*
Check sampler IF	Unlocked YTO PLL *(steps 22-26)*
Check sampler/sampler IF operation	Sampler and Sampler IF *(steps 1-15)*
Check span attenuator	First LO Span Problems (All Spans) *(steps 6-13)*
Check sweep generator	Sweep Generator Circuit
Check sweep + tune multiplier	YTF Driver Circuit *(steps 4-9)*
Check the 600 MHz reference loop amplifier	Unlocked Reference PLL *(steps 23-26)*
Check the YTO loop	Unlocked YTO PLL
Check YTO FM coil driver	First LO Span Problems (2.01 MHz to 20 MHz) *(step 6)*
Check YTO FM coil driver and main loop error voltage driver	Unlocked YTO PLL *(steps 35-40)*

Table 11-3   **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A14J15	Sweep generator	MS8
	Span attenuator DAC	MS7
	Span attenuator switches	MS7
	Sweep + tune multiplier input amp	MS1, OS1
	Sweep + tune multiplier input switches	MS1, MS3
A14J16	FAV generator	MS4
	FAV generator 0.5 V/GHz output	MS5
	YTF offset DAC	MS6
	YTF gain and offset input	MS2
	YTF gain DAC	MS1
	YTF drive	MS3
	Band switch driver	MS8
A14J17	Main coil coarse DAC	MS3
	Main coil fine DAC	MS2
	Main coil DACs output	MS5
	Main loop error volt DVR	MS4
	Option drive	MS8
	Option drive switch	MS7
	Option drive DAC	MS6
A14J18	±10 V reference	MS1, MS2
	LODA drive	MS5, MS6, MS7, MS8
	Main coil tune DAC	MS3
A14J19	Second converter PIN switch	MS8
	Second converter mixer bias	MS1
	Second converter drain bias	MS3
	Second converter doubler bias	MS4
	Second converter driver bias	MS5
	First mixer drive switch	MS7
	First mixer drive DAC	MS6

Table 11-3   **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A14J302	Revision	MS7
	Fractional N out	MS1
	Divided reference	MS4
	Feedback buffer bias	MS5
	Outamp bias	MS6
A15J200	Positive 15 volt supply	MS1
	Sampler drive buffer bias	MS2
	Sampling oscillator bias	MS3
	Offset lock drive buffer	MS4
	OFL error voltage	MS6
	Negative 10 volt supply	MS8
	Offset lock loop BW DAC	MS5,MS7,MS8
A15J400	Positive 15 volt supply	MS2
	Offset lock RF buffer	MS4
	IF AMP/limiter bias	MS6
	Offset lock loop buffer D	MS7
	Offset lock loop buffer C	MS8
	Sampler bias test	MS3
A15J502	Positive 15 volt supply	MS2
	Third LO tune voltage	MS3
	Offset lock loop buffer	MS4
	600 MHz oscillator bias	MS5
	Calibrator AGC amp bias	MS6
	Calibrator amplitude adj	MS7
	3rd LO driver amp	MS1, MS8
A15J602	Positive 15 volt supply	MS8
	Flatness compensation 3	MS2
	Flatness compensation 2	MS5
	Flatness compensation 1	MS6
	SIG ID collector bias	MS7
	RF gain control test	MS1, MS3

Table 11-3 **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A15J901	Revision	MS3
	External mixer switch	MS1, MS8
	Signal ID switch	MS5, MS6
	Ten volt reference	MS4
	External mixer bias	MS7

Troubleshooting Test Setup

Some synthesizer section problems require placing the YTO PLL in an unlocked condition. This is done by moving jumper A14J23 to the TEST position. This grounds the YTO ERROR signal, disabling the ability of the CPU to detect an unlocked YTO. The FM coil driver output is set to its mid-range level causing the YTO to be controlled only by the main coil tune DAC.

Synthesizer section troubleshooting is best done with the spectrum analyzer SPAN set to 0 Hz (even though it is still possible to sweep the Main and FM coils of the YTO).

With the YTO in its unlocked conditions and the SPAN set to 0 Hz, the nominal YTO frequency is not necessarily the value listed as LO FREQ in the Frequency Diagnose menu. The YTO has an initial pretune accuracy of ±20 MHz. To display the nominal YTO frequency, press **CAL**, **MORE 1 OF 2**, **FREQDIAGNOSE**, **LO FREQ**.

The fractional N oscillator frequency is the same as the desired sampler IF. To display the fractional N oscillator frequency, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ**. If the sampler IF is negative (YTO frequency is lower than the desired sampling oscillator harmonic), the fractional N frequency will be displayed as a negative number.

Confirming a Faulty Synthesizer Section

The A11 YTO (the spectrum analyzer first LO) is a YIG-tuned oscillator which tunes from 2.95 to 6.8107 GHz. The A7 switched LO distribution amplifier (SLODA) levels the output of A11 and distributes the signal to the A8 low band mixer, A10 YIG-tuned mixer/filter (RYTHM), A15U100 sampler, and the front panel 1ST LO OUTPUT. The synthesizer section includes the following PLLs (Phase Locked Loops):

YTO PLL	A7, A11, A14 and A15 assemblies
Offset PLL (sampling oscillator PLL)	A15 RF assembly
Fractional N PLL	A14 frequency control assembly
Reference PLL	A15 RF assembly

The fractional N PLL is sometimes swept backwards (higher frequency to lower frequency). This is necessary because of the way in which the sampler IF signal is produced.

NOTE

The frequency control board is digitally controlled. If multiple failures appear in unrelated areas of the circuitry, the control may be at fault. Refer to the troubleshooting procedures in this chapter for further help on isolating those failures.

The TAM tests the signal path circuitry by digitally controlling the hardware and monitoring the control lines to make sure they are responding properly. Use the TAM automatic fault isolation routine or verify the RF levels manually to ensure proper operation.

Check A3 ADC MUX Function Block (steps 1-4)

1. Connect the positive lead of a DVM to A15J200 pin 13 and the negative lead to A15J200 pin 6. This measures the sampling oscillator tune voltage which is an input to the A3 interface assembly ADC MUX.

2. Set the spectrum analyzer to the following settings:

   Span .... 0 Hz
   Center frequency .... 389.5 MHz
   Trigger .... Single

3. Use the data entry keys to tune the **CENTER FREQ** to the values listed in .

4. As the sampling oscillator frequency is increased, the DVM reading should also increase. If the tune voltage is correct, but the ADC measures the voltage and determines it to be out of specification, troubleshoot the A3 assembly ADC MUX.

Table 11-4   Center Frequency Tuning Values

8562E/EC Center Frequency (MHz)	Sampling Oscillator Frequency (MHz)
2156.3	285.000
2176.3	286.364
2199.5	287.500
2230.3	288.462
799.3	288.889
2263.3	290.000
2282.3	290.909
2302.3	291.667
2155.3	292.500
2158.3	293.478
2336.3	294.444
2196.3	295.000
1.3	296.000
2378.3	296.471
2410.3	297.000
2422.3	297.222

Check A14J301 10 MHz reference input (steps 5-8)

5. Disconnect W37 from A14J301.

6. Connect a test cable from W37 to the input of another spectrum analyzer. Tune the other spectrum analyzer to the following settings:

    Center frequency .... 10 MHz
    Span .... 2 MHz

7. The amplitude of the 10 MHz reference signal should measure >−1 dBm. If the signal does not measure >−1 dBm, troubleshoot the 10 MHz distribution on A15 and A21 OCXO (If not Option 103).

8. Reconnect W37 to A14J301.

Check First LO (steps 9-11)

9. Connect the CAL OUTPUT to INPUT 50Ω .

10. Set the spectrum analyzer to the following settings:

     Center frequency .... 300 MHz
     Span .... 100 MHz

11. If the first LO is present, a signal should be displayed at about −10 dBm (approximately ±20 MHz from the center frequency). If no signal is displayed and ERR 334 LO AMPL is not present, suspect the A7 SLODA. If no signal is displayed and ERR 334 LO AMPL is present, check the A11 YTO as follows:

    a. Set jumper A14J23 to the TEST position.

    b. Set the spectrum analyzer to the following settings:

         Center frequency .... 50 Hz
         CF step .... 300 MHz
         Span .... 0 Hz

    c. Connect a power meter directly to the output of the A11 YTO.

    d. Press the spectrum analyzer step-up key and measure the YTO output power at each step.

    e. Check that the A11 YTO output power is between +9 and +13 dBm.

    f. Set jumper A14J23 to the NORM position and reconnect the A11 YTO.

Check A14 frequency control assembly (steps 12-18)

12. On the spectrum analyzer press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. Note the fractional N oscillator frequency. (Ignore the minus sign, if present.)

 Fractional N Oscillator Frequency = _____MHz

13. Check A14J304 (FRAC N TEST) port with a spectrum analyzer for this exact frequency. The amplitude should be approximately −10 dBm.

14. Disconnect W32 from A14J501 and connect the output of a signal source to A14J501. Remove the jumper from A14J23. Connect the positive lead of a DVM to A14J23 pin 1 and negative lead to A14J23 pin 3. See Figure 11-3 on page 543.

15. Set the signal source to the following settings:

     Power .... 0 dBm
     Frequency .... Frequency recorded in step 12

16. Tune the source 1 kHz below the fractional N frequency. The voltage measured on the DVM should be approximately 12 Vdc.

17. Tune the source 1 kHz above the fractional N frequency. The voltage measured on the DVM should be approximately –12 Vdc.

18. If the DVM reading does not change, the A14 frequency control assembly is defective. Reconnect W32 to A14J501. Replace the jumper on A14J23 to the NORM position.

Figure 11-3   YTO Loop Test Setup
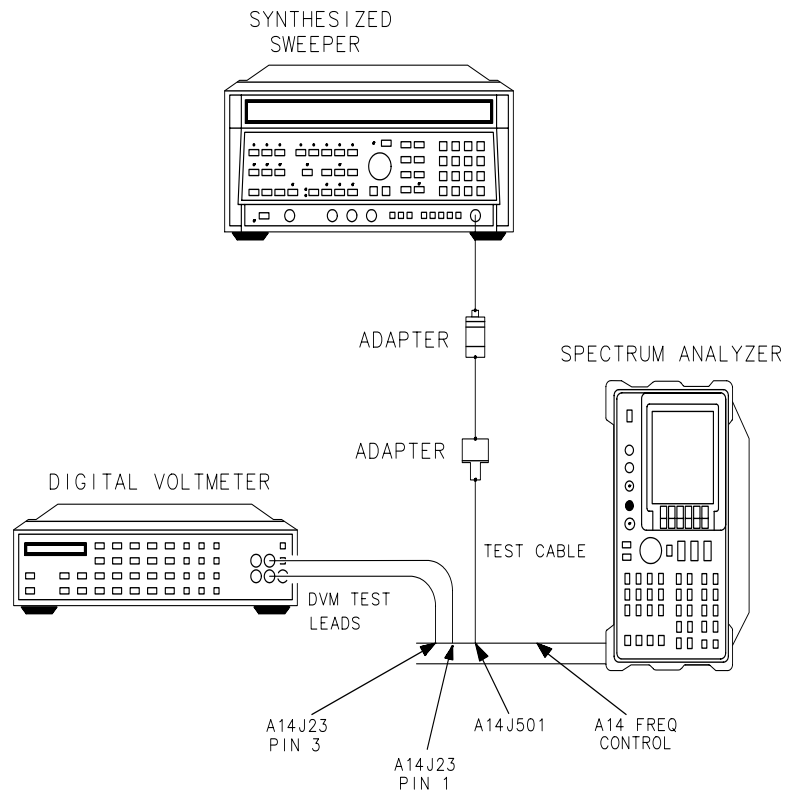
Sp127e

Check A15 RF assembly (steps 19-25)

19. Disconnect W34 from A15U100J1 and disconnect W32 from A15J101.

20. Connect a frequency counter to A15J101. Connect a high-frequency test cable from an 8340A/B synthesized sweeper to A15U100J1. See Figure 11-4 on page 544.

21. Connect a BNC cable from the spectrum analyzer 10 MHz REF IN/OUT to the 8340A/B FREQUENCY STANDARD EXT input.

22.Set the 8340A/B to the following settings:

Frequency standard .... EXT
Power level .... −5 dBm

23.Set the spectrum analyzer to the following settings:

Span .... 0 Hz
Trigger .... Single

24.Set the spectrum analyzer and 8340A/B frequencies to the combinations listed in Table 11-5 on page 545 and press **SGL SWP** on the spectrum analyzer.

Figure 11-4   Sampler and Sampling Oscillator Test Setup
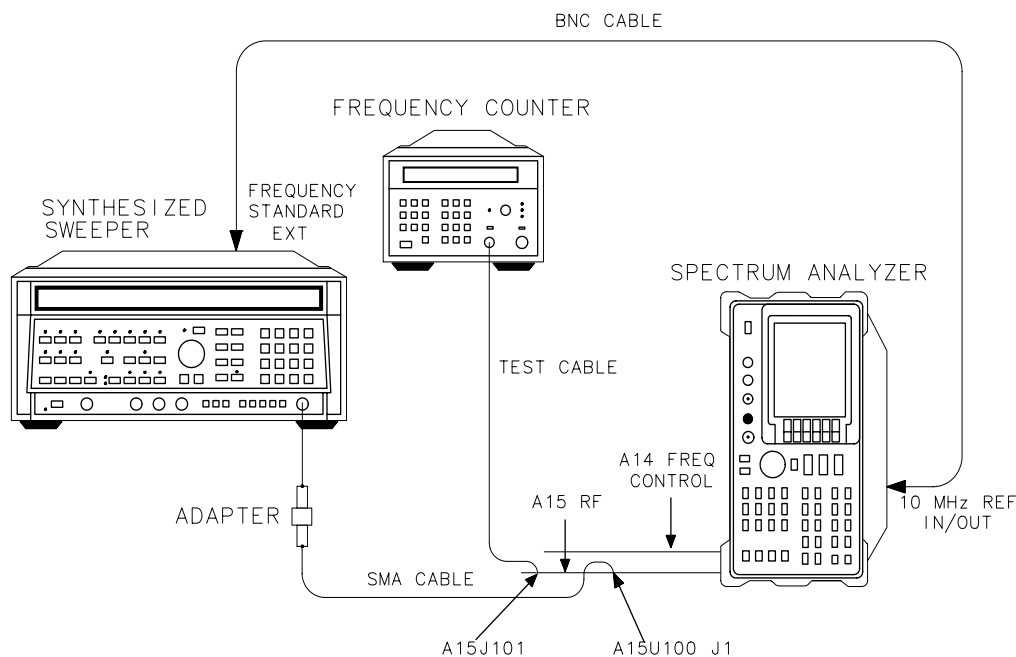
sm624e

25.At each combination, the frequency counter should measure a sampler IF as shown in Table 11-5 on page 545. (The sampling oscillator of the offset PLL tunes to the frequencies listed in the table.) If the frequency counter does not read the indicated sampler IF ±10 kHz, suspect the A15 RF assembly.

26.Reconnect W34 to A15U100J1 and W32 to A15J101.

27.The First LO OUTPUT, located on the front panel, must be terminated in 50 ohms. If the YTO unlocks only with certain center frequency and span combinations, check that the termination is in place.

28. Set the spectrum analyzer **CENTER FREQ** and **SPAN** to generate the unlock conditions.

29. On the spectrum analyzer press **SGL SWP**.

30. Move jumper A14J23 to the TEST position.

31. Disconnect W34 from A15U100J1 and measure the power of the signal at the end of W34.

32. If the power is less than –6.5 dBm, suspect W34, A7 SLODA, or A11 YTO.

33. Move jumper A14J23 to the NORM position.

Table 11-5   **Sampling Oscillator Test Frequencies**

8340A CW Frequency (GHz)	8563E Center Frequency (MHz)	Offset PLL Sampling Oscillator Freq (MHz)	Counter Reading Sampler IF (MHz)
6.067000	2156.3	285.000	82.000
6.087000	2176.3	286.364	73.364
6.110200	2199.5	287.500	72.700
6.141000	2230.3	288.462	83.308
4.710000	799.3	288.889	87.778
6.174000	2263.3	290.000	84.000
6.193000	2282.3	290.909	83.909
6.213000	2302.3	291.667	88.000
6.066000	2155.3	292.500	76.500
6.069000	2158.3	293.478	94.044
6.247000	2336.3	294.444	63.667
6.107000	2196.3	295.000	88.000
3.912000	1.3	296.000	64.000
6.289000	2378.3	296.471	63.118
6.321000	2410.3	297.000	84.000
6.333000	2422.3	297.222	91.333

General PLL Troubleshooting

The synthesizer section relies heavily on phase-locked loops (PLL). Typically, a faulty PLL is either locked at the wrong frequency or unlocked. The information below applies to troubleshooting these two classes of problems on a generalized PLL.

PLL Locked at Wrong Frequency

Numbers in the following text identify items in Figure 11-5 on page 547:

- Any frequency errors at reference (1) will be multiplied by N/M on the PLL output.

- A sampler reference-frequency error (2) will be multiplied by its harmonic on the PLL output.

- A mixer reference-frequency error (3) produces the identical error on the PLL output.

- If divider input or output frequencies (4) are wrong, check for incorrect divide numbers and data controlling the dividers.

Figure 11-5 **PLL Locked at Wrong Frequency**

sp129e

Unlocked PLL

An unlocked PLL can be caused by problems inside or outside the PLL. Troubleshoot this problem by working backward from the oscillator as described in the steps below. Numbers in the following text identify items in Figure 11-6 on page 548.

1. The loop integrator output voltage (1) should be attempting to tune the oscillator to the correct frequency:

   The voltage at (1) should increase as the frequency increases on all of the PLLs:

PLL	Measurement Point
YTO PLL	A14J23 pin 1 (YTO ERROR)
Reference PLL	A15J502 pin 3 (LO3 ERR)
Sampler PLL	A15J200 pin 13 (OFL ERR)
Fractional N PLL	A14TP13 (INTEGRATOR)

Figure 11-6   Unlocked PLL

sp130e

2. If the integrator output voltage changes in the manner described in step 1, the problem is external to the PLL. For example, the reference frequency could be faulty. If the integrator output voltage appears incorrect, confirm that the pulses out of the phase detector (2) are attempting to tune the oscillator in the correct direction.

3. If the phase detector output is bad, check the inputs to the detector (3). One input should be higher in frequency than the other; this should match the phase detector outputs.

4. Confirm proper power levels for the signals at the input to the "N" dividers (4), the reference inputs (5 and 7), and the loop feedback path (6).

Unlocked Reference PLL

Operation

The 600 MHz reference is generated by tripling, then doubling the output of the 100 MHz phase-locked loop. If the 600 MHz reference is off frequency, the 100 MHz phase-lock circuitry is probably at fault. If there is no signal present at A15J701, or if the level is less than −3 dBm, the 100 MHz VCXO, the tripler, or the doubler circuitry has probably failed. Refer to function blocks Q, R, and S of the A15 RF schematic (08563-90071, 08563-90072, or 08563-90073) sheet 2 of 4 in the *8560 E-Series Spectrum Analyzer Component Level Information* binder.

Troubleshooting

Check 100 MHz VCXO, tripler, and doubler (steps 1-7)

1. Using an active probe/spectrum analyzer combination, such as the 85024A/8566B, measure the tripler output at A15TP700. The tripler output should be +3 dBm ±2 dB.

2. If the tripler output is within tolerance, suspect the doubler circuitry. Refer to function block S of the A15 RF schematic.

3. If the tripler output is too low, probe the output of A15U700 RF amplifier. The level should be +16.5 dBm ±2 dB. The level at the input of A15U700 should be +8.5 dBm ±2 dB.

4. If the level at the input of A15U700 is too low, suspect a faulty 100 MHz VCXO. Refer to function block Q of the A15 RF schematic.

5. On the spectrum analyzer, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.

6. Measuring the tune voltage indicates if the 100 MHz PLL is locked. Connect the ground lead the voltmeter to A15J1 pin 3 and measure the voltage at A15J700 pin 3.

7. The tune voltage should be between +1 and +24 Volts. If the tune voltage is incorrect, place the P700 jumper (on A15J700) in the TEST position (pin 1 to pin 2). This sets the tune voltage for varactor A15CR700 to the nominal +13 Volts, making it easier to troubleshoot the 100 MHz VCXO, tripler, and doubler. Remember to return P700 jumper to the NORMAL position when you have finished troubleshooting the oscillator circuitry.

8. If the 100 MHz oscillator is working, the reason for the unlocked condition is either a problem in the 10 MHz reference or a fault in the signal path around the loop.

Check 10 MHz reference to phase/frequency detector (steps 9-14)

9. On the spectrum analyzer, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.

10. Check the 10 MHz reference frequency-accuracy by connecting a frequency counter to A15J301 and verify that the reference frequency is 10 MHz ±40 Hz after a 5 minute warmup period.

11. If a 10 MHz signal >1 V peak-to-peak is not present at A15J301, refer to "10 MHz Reference" on page 622.

12. Measure the signal at TP301 with an oscilloscope. Refer to function block M of A15 RF schematic.

13. Measure the signal at U502 pin 11 with an oscilloscope. Refer to function block X of A15 RF schematic. This signal should be TTL levels at 10 MHz with a 60 percent duty cycle.

14. If TTL-level signals (approximately 10 MHz) are not present, check signals backwards through the loop to find a fault in the signal path.

15. Measure the signals at the following test points with an active probe/spectrum analyzer combination:

Junction of **C570 and C571**	100 MHz, +2.5 dBm ±2 dB
Junction of R715, **R716, R567, and R568**	100 MHz, −3 dBm ±2 dB
U700 pin 3	100 MHz, +16.5 dBm ±2 dB
U700 pin 1	100 MHz, +8.5 dBm ±2 dB

16. If an approximately 10 MHz TTL signal is present at U502 pin 11 with 60 percent duty cycle, and the RF portion of the phase-lock loop is functioning, the fault probably lies in the phase/frequency detector or the 100 MHz lock loop integrator.

Check phase/frequency detector (steps 17-22)

17. Monitor U504 pin 5 and U503 pin 9 with an oscilloscope. These are the two outputs of the phase/frequency detector. Refer to function block O of A15 RF schematic.

18. A locked loop will exhibit stable, narrow (approximately 20 ns wide), and positive-going TTL pulses occurring at a 10 MHz rate at U504 pin 5 and U503 pin 9.

19. If the loop is unlocked, but signals are present on both inputs of the phase/frequency detector, the output pulses will be superimposed on each other.

20. If the loop is unlocked, and there is no signal at one of the phase/frequency detector inputs, one phase detector output will be at TTL low and the other will be at TTL high. For example, if there is no input signal at U504 pin 3, U504 pin 5 will be TTL low and U503 pin 9 will be TTL high. If there is no input signal at U503 pin 11, U503 pin 9 will be TTL low and U504 pin 5 will be TTL high.

21. To remove the 10 MHz reference input to the phase/frequency detector, press **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT** with no signal applied to the rear-panel 10 MHz REF IN/OUT connector.

22. To remove the divided-down 100 MHz signal from the phase/frequency detector, short R595. Refer to function block X of A15 RF schematic.

Check the 100 MHz lock loop integrator (steps 23-27)

23. Remove 10 MHz reference input to the phase/frequency detector by pressing **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT**. No signal should be connected to the rear-panel 10 MHz REF IN/OUT connector.

NOTE The outputs of phase/frequency detector are low-pass filtered to reduce the 10 MHz component of the signal. The filtered signals are then integrated by U506 and the result is fed to the tune line of the 100 MHz VCXO.

24. Check that the voltage on A15J502 pin 3 is less than 0 Vdc. Refer to function block P of A15 RF schematic.

25. Press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT** and remove the divided-down 100 MHz input to the phase/frequency detector by shorting R572.

26. Check that the voltage on A15J502 pin 3 is greater than 13 Vdc.

27. If the loop is locked, the voltage on A15J502 pin 3 should be between 0 and +6 Vdc.

28. If the front-panel CAL OUTPUT amplitude is out of specification and cannot be brought within specification by adjusting A15R561, CAL AMPTD, check the calibrator AGC amplifier with the following steps. Refer to function block W of A15 RF schematic.

NOTE The 300 MHz CAL OUTPUT signal comes from the tripled 100 MHz which is passed through a leveling loop. The 300 MHz signal passes through a low-pass filter for reducing higher harmonics. These harmonics can fool the detector. The 300 MHz signal passes through a variable attenuator controlled by PIN diode CR503 which is controlled by the feedback loop. Diode CR504 is the detector diode (the same type as CR505). Diode CR504 provides temperature compensation between the reference voltage and the detected RF voltage.

    a. Measure the level of 300 MHz at A15 TP505 with an active probe/spectrum analyzer combination. If the signal is less than +2 dBm, repeat the first 27 steps of this procedure.

    b. If the signal at this point is correct, place a short across the PIN diode CR503.

    c. If the signal level at the CAL OUTPUT is still less than –10 dBm with CR503 shorted out, troubleshoot the RF forward path through amplifier Q505. (The signal amplitude decreases.)

    d. If the CAL OUTPUT signal level is greater than –10 dBm, troubleshoot the PIN diode attenuator, the detector, or the feedback path.

29. Measure the detector voltage at A15J502 pin 14. The voltage should measure approximately +0.3 Vdc when the CAL OUTPUT signal is at –10 dBm. This voltage should change with adjustment of A15R561, CAL AMPTD.

30. Check that the voltage at U507A Pin 3 is +1.7 Vdc. If this voltage is not correct, there may be a problem with the +10 V reference.

31. Measure voltage at U507B pin 5 while adjusting R561. This is the temperature-compensated adjustable voltage reference to which the detected voltage is compared. It should vary between +0.15 V and +0.6 V.

32. Adjust R561 to its limits and verify that the output U507B pin 7 measures approximately +1 Vdc at one limit and –12 Vdc at the other limit.

Third LO Driver Amplifier

The third LO driver amplifier (Q503) amplifies the 300 MHz from the 300 MHz distribution amplifier to a sufficient level to drive the LO port of the double balanced mixer. During the SIG ID operation, diodes CR501 and CR502 turn off the 3rd LO driver amplifier in order to minimize the amount of 300 MHz going to the double-balanced mixer.

Check level at amplifier input (steps 1-6)

1. Press **AUX CTRL**, **INTERNAL MIXER**. Press **SIG ID OFF**, if Option 008 is installed.

2. Use an active-probe/spectrum-analyzer combination to confirm the power level of the 300 MHz signal at the following test points:

A15X602 pin 5	≥+7 dBm
A15TP504	≥+15 dBm

3. If the signal at A15X602 pin 5 is low, but the signal at A15TP504 is correct, press **AUX CTRL**, **INTERNAL MIXER**. Press **SIG ID OFF**, if present.

4. Check that PIN diode switches CR603 and CR605 are reverse biased by approximately +10 Vdc. Refer to function block F of A15 RF schematic.

5. Measure 300 MHz signal at A15TP503 using an active probe/spectrum analyzer combination. If the signal is not approximately +10 dBm, refer to "Unlocked Reference PLL" on page 549.

6. If the level at the TP503 is correct, but signal at TP504 is too low, the fault is probably in the amplifier.

Unlocked Offset Lock Loop (Sampling Oscillator)

Operation

The offset lock loop drives the A15U100 sampler. The offset lock loop sampling oscillator tunes to one of sixteen discrete frequencies between 285 MHz and 297.222 MHz. Refer to A15 schematic. Mixer A15U400 mixes the oscillator output with 300 MHz from the reference PLL, producing a 3 MHz to 15 MHz IF signal. The 3 MHz to 15 MHz signal is compared in the phase/frequency detector with the divided-down 300 MHz from the reference PLL. The phase/frequency detector drives a voltage-to-current diode switch which drives the loop integrator. Loop bandwidth switches vary the loop bandwidth to minimize noise sidebands. The sampling oscillator must produce low noise because the A15U100 sampler multiplies noise by a factor of approximately 24.

Table 11-6 on page 555 lists the prescaler and postscaler divide numbers in the offset loop reference divide chain, for each of the 16 discrete frequencies to which the offset lock loop may be set. It also indicates what the reference frequency into the phase/frequency divide chain is. Refer to function block AN on the RF schematic.

Troubleshooting

Check loop references (steps 1 and 2)

1. Use an active probe and spectrum analyzer to confirm the presence of the following reference to the offset lock loop input.

   A15TP404   300 MHz at +5 dBm

2. If this signal is not correct, refer to "Unlocked Reference PLL" on page 549.

Check levels into mixer (steps 3-13)

3. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Trigger .... Single

4. Force the PLL to unlock by shorting A15X201 pin 1 to A15X201 pin 5 with a short length of wire. Then connect a dc power supply to A15J200 pin 16.

5. Monitor A15TP201 with an active probe/spectrum analyzer combination. Vary the dc supply until the frequency of the sampling oscillator is 296 MHz.

6. The voltage required to tune the oscillator should measure between +15 Vdc and +19 Vdc. If the voltage is out of this range, perform the sampling oscillator adjustment in Chapter 2 , "Adjustment Procedures."

7. Vary the voltage to tune the sampling oscillator to 296 MHz.

8. Use an active probe/spectrum analyzer combination to measure the 300 MHz LO signal at the following test point:

   A15TP402   +7 dBm

9. If the signal is not measured near the indicated power, troubleshoot the offset lock loop buffer (function block AM of A15 RF schematic sheet 3 of 4).

Table 11-6   **Sampling Oscillator PLL Divide Numbers**

Sampling Oscillator Frequency (MHz)	Center Frequency* (MHz)	Reference Divide Chain		Reference Frequency (MHz)
		Prescaler	**Postscaler**	
285.000	2156.3	10	2	15.000
286.364	2176.3	11	2	13.636
287.500	2199.5	8	3	12.500
288.462	2230.3	13	2	11.538
288.888	799.3	9	3	11.111
290.000	2263.3	10	3	10.000
290.909	2282.3	11	3	9.091
291.666	2302.3	9	4	8.333
292.500	2155.3	8	5	7.500
293.478	2158.3	23	2	6.522
294.444	2336.3	9	6	5.556
295.000	2196.3	10	6	5.000
296.000	1.3	15	5	4.000
296.471	2378.3	17	5	3.529
297.000	2410.3	20	5	3.000
297.222	2422.3	18	6	2.778

* To set the sampling oscillator to a desired frequency, set span to 0 Hz and **CENTER FREQ** to the value listed in the table.

10. Measure the 296 MHz loop feedback signal at the following test point:

   A15TP400   +2 dBm

11. If the feedback signal is not near the indicated power, measure the signals at the following test points on the feedback path. Refer to function blocks AD, AG, and AH of A15 RF schematic.

A15TP200	+4 dBm
A15TP201	+9 dBm
A15TP202	+5.5 dBm

12. Measure the 4 MHz loop-IF signal at the mixer output. The frequency of the IF is the same as the reference frequency and can be found in Table 11-6 on page 555.

A15R447 (end nearest L414)   −6 dBm

13. If the IF signal is not near the indicated power, troubleshoot the loop mixer (function block AI).

Check path to phase/frequency detector (steps 14-19)

14. Measure the loop IF signal at the input to the IF amplifier/limiter (function block AK):

A15L428 (end nearest U411)   4 MHz
(approximately −6 dBm)

15. Confirm the presence of a 4 MHz square-wave reference frequency signal at U406 pin 3. The square wave is TTL and should go below +0.6 V and above +2.2 V.

16. Disconnect the jumper from X201 pins 1 and 5. Disconnect the dc power supply which is connected to A15J200 pin 16.

17. Set the spectrum analyzer to the following settings:

Center frequency .... 300 MHz
Span .... 0 Hz

18. Use an oscilloscope to confirm the presence of a 4 MHz TTL-level reference frequency signal at U406 pin 11.

19. Connect a short across A15R425. Connect A15U406 pins 3 and 11 together. This puts the same signal on both the phase/frequency detector inputs.

20. Observe the phase/frequency detector outputs, U406 pins 6 and 9, with an oscilloscope. Narrow TTL pulses should be present. Pin 9 is normally low, pulsing high, and pin 6 is normally high, pulsing low.

21. Check the end of L417 (nearest C445) with an oscilloscope. With the oscilloscope input ac-coupled, a triangle waveform approximately 20 mVp-p should be present.

22. Short C441 with a wire jumper. (Connect the jumper from the end of R462 nearest C441 to the end of R460 nearest C443.) This changes the loop integrator into a voltage follower. Refer to function block AB of A15 RF schematic.

23. Check the voltages at the following points:

A15U408 pin 6	+2.5 Vdc (approximately)
A15X201 pin 1	+2.5 Vdc (approximately)

24. If the voltages are not correct, suspect A15U408.

25. Remove the jumpers.

Unlocked YTO PLL

Operation

The A11 YTO is locked to two other oscillators, the fractional N oscillator and the offset PLL sampling oscillator. For LO spans of 2.01 MHz and above, either the FM or main coil of the YTO is swept directly. For LO spans of 2 MHz and below, the fractional N oscillator is swept. The sampling oscillator remains fixed-tuned during all sweeps.

The output of A11 YTO feeds through the A7 switched LO distribution amplifier to the A15U100 sampler. The offset PLL sampling oscillator, which drives the sampler, oscillates between 285 and 297.222 MHz. The sampler generates harmonics of the sampling oscillator and one of these harmonics mixes with the YTO frequency to generate the sampler IF frequency. As a result, the frequency of the sampler IF is determined by the following equation:

$$F_{IF} = F_{YTO} - (N \times F_{SAMP})$$

Where:

— F_{IF} is the sampler IF

— F_{YTO} is the YTO frequency

— N is the desired sampling oscillator harmonic

— F_{SAMP} is the sampling oscillator frequency

Notice that F_{IF} can be positive or negative depending upon whether the sampling oscillator harmonic used is below or above the YTO frequency. The actual sampler IF is always positive, but the sign is carried along as a "bookkeeping" function which determines which way to sweep the fractional N oscillator (up or down) and what polarity the YTO error voltage should have (positive or negative) to maintain lock.

To check if a negative sampler IF is selected, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ**. If the fractional N oscillator frequency is positive, the sampler IF is also positive. A negative fractional N frequency indicates that the sampler IF is negative.

Notice that the polarity of the YTO loop error voltage (YTO ERROR) out of the YTO loop phase/frequency detector changes as a function of the polarity of the sampler IF. That is, for positive sampler IFs, an increasing YTO frequency results in an increasing YTO ERROR signal. For negative sampler IFs, an increasing YTO frequency results in a decreasing YTO ERROR signal. This implies that to maintain lock in both cases, the sense of YTO ERROR must be reversed such that, with a negative sampler IF, an increasing YTO ERROR results in an increasing YTO frequency. This is accomplished with error-sign amplifier, A14U328B. This amplifier can be firmware-controlled to operate as either an inverting or non-inverting amplifier. Digital control line ERRSGN (from A14U313 pin 19) controls the polarity of this amplifier. When ERRSGN is high (positive sampler IF), the amplifier has a positive polarity.

In fractional N spans (LO Spans ≤2 MHz) the YTO remains locked to the sweeping fractional N PLL. Thus, the sampler IF must always equal the fractional N oscillator frequency (conditions for lock). Since the YTO must always sweep up in frequency, for negative sampler IFs, the fractional N oscillator must sweep from a higher frequency to a lower frequency. This is necessary since an increasing YTO frequency decreases the sampler IF for negative sampler IFs. The opposite is true for positive sampler IFs, so in these cases, the fractional N oscillator sweeps more conventionally from a lower frequency to a higher frequency.

Table 11-7 on page 560 summarizes the amplifier polarities for the various combinations of sampler IF polarities and LO spans.

The YTO main coil filter is used to improve residual FM in FM spans. See function block I of A14 frequency control schematic in the Component-Level Information binder. Transistors Q304 and Q305 switch the filter (capacitor C36 and resistor R48) into the circuit. Transistor Q303 and U333 keep C36 charged during main spans so the frequency does not jump when C36 is switch in.

Table 11-7 **Amplifier Polarities**

		YTO Error Sign Amplifier	ERRSGN (A14U313 pin 19)
Fractional N Oscillator Swept	Positive Sampler IF	Positive	TTL High
	Negative Sampler IF	Negative	TTL Low
FM/Main YTO Coils Swept	Positive Sampler IF	Positive	TTL High
	Negative Sampler IF	Negative	TTL Low

Troubleshooting an Unlocked YTO PLL

1. If the YTO PLL is unlocked, error code 301 should be displayed. Place the spectrum analyzer in ZERO SPAN. Figure 11-7 on page 561 illustrates the simplified YTO PLL.

2. Move the jumper on A14J23 to connect pins 2 and 3 (TEST position). Refer to Figure 11-1 on page 533 for the location of A14J23. Error code 301 should no longer be displayed. (The YTO PLL feedback path is now open and the YTO error voltage is forced to zero.)

3. On the spectrum analyzer, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **LO FREQ**. The displayed LO FREQ is the desired YTO frequency calculated. Record the calculated frequency of the YTO below:

   YTO Frequency (calculated) = _____MHz

4. Measure the YTO frequency at the front-panel First LO OUTPUT jack and record below:

   YTO Frequency (measured) = _____MHz

Figure 11-7   Troubleshooting an Unlocked YTO PLL


```
A14 FREQUENCY CONTROL ASSEMBLY

                                    MAIN COIL TUNING
        J18-3                                              A11
                                    J15-4                  YTO
MAIN COIL
TUNING DAC                                                 9 TO 17
        J17-2                                              dBm
                    J17-5                         J1
MAIN COIL                      1 NORM    FM COIL
COARSE DAC            J23     2 J17-1     TUNING
        J17-3                  3 TEST   U328D      8561E      8563E
                                                  A7 LO      A7 SWITCHING
MAIN COIL                             U207        DIST AMP   LO DIST AMP
FINE DAC                                              J4
                                                  BLACK
                                                  CABLE    A15A2J1
                                                  A15 RF
                                                  ASSEMBLY
                                                            SAMPLER
                                            J101            LO DRIVE
Fractional N   ÷2   ÷5,6,7       ø f              J501   S
   PLL                                                    SAMPLER

            J304                      -10 TO +5 dBm
            FRAC N TEST               60 TO 96 MHz
            APPROX -10 dBm            WHEN LOCKED, SAME
            60 TO 96 MHz              AS FRACTIONAL N FREQ

                                                  sm614e
```

5. Calculate the YTO frequency error by subtracting the frequency
   recorded in step 3 from the frequency recorded in step 4. Record the
   result below:

   YTO Frequency Error = _____MHz

   YTO Frequency Error = YTO Frequency $_{(MEASURED)}$ – YTO
   Frequency $_{(CALCULATED)}$

6. On the spectrum analyzer, press **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. Record the fractional N frequency below:

Fractional N frequency = _____MHz

CAUTION   Replacement of the phase/frequency detector chip A14U204 is not recommended. The part is very delicate and requires special tooling to install successfully.

---

7. If the YTO frequency error recorded in step 5 is greater than 20 MHz, do the following:

   a. Check the YTO Adjustments using the TAM or the procedure in Chapter 2 , "Adjustment Procedures."

   b. Check the YTO DACs using the procedure in steps 41 through 49 below, or using manual probe troubleshooting with the TAM on A14J17 and A14J18.

   c. Refer to steps 9 through 34 below.

8. If the YTO Frequency error recorded in step 5 is less than 20 MHz, do the following:

   a. Measure the frequency at A14J304. The frequency should be equal to the frequency recorded in step 6. If not, refer to "Unlocked Fractional N PLL" on page 568.

   b. Measure the input and output levels of the A15U100 sampler. If the sampler appears defective, check the LO drive to the sampler as described in "Sampler and Sampler IF" on page 583.

   c. Refer to steps 34 through 51 below.

Check First LO pretune frequency and amplitude (steps 9-12)

9. The pretuned frequency of the first LO must be sufficiently accurate for the YTO loop to acquire lock. The amplitude of the first LO must be sufficient to drive the A15U100 sampler. Perform the YTO Adjustment procedure, particularly the YTO main coil adjustments. (If available, use a synthesized microwave spectrum analyzer instead of the microwave frequency counter specified in the adjustment procedure.)

10. If the YTO main coil cannot be adjusted, proceed to step 33 to troubleshoot the main coil coarse and fine DACs and main coil tune DAC.

11. The front-panel first LO OUTPUT should measure between +14.5 and +18.5 dBm in amplitude.

12. If the first LO OUTPUT amplitude is out of the specified range, perform the first LO distribution amplifier adjustment procedure. Refer to Chapter 2 , "Adjustment Procedures."

Check the fractional N oscillator (steps 13-17)

13. Set the spectrum analyzer to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

14. Monitor the fractional N PLL output at A14J304 (FRAC N TEST) with a synthesized spectrum analyzer such as an 8568A/B or 8566A/B. Refer to function block AI of A14 frequency control schematic.

15. The signal at A14J304 (FRAC N TEST) should measure approximately –10 dBm at 66.7 MHz. If the loop is unlocked, the sampler IF frequency can also be seen on A14J304, about 30 dB below the fractional N signal.

16. If a problem exists only at particular CENTER FREQ and SPAN settings, determine the desired fractional N oscillator frequency by pressing **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ** and setting the 8563E to SINGLE trigger mode.

17. If the fractional N oscillator frequency is not correct, refer to "Unlocked Fractional N PLL" on page 568.

Check sampler drive output of A7 SLODA (steps 18-21)

18. Set jumper A14J23 to the TEST position and set the spectrum analyzer to the following settings:

    Center frequency .... 2.9 GHz
    Span .... 0 Hz

19. Disconnect cable W34 from A15U100J1.

20. Use a power meter to measure the A7 SLODA sampler-drive output at the end of W34. The power should measure greater than –9 dBm.

21. Place jumper A14J23 in the NORMAL position and reconnect W34 to A15U100J1.

Check sampler IF (steps 22-26)

22. Set the spectrum analyzer to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

23. Place jumper A14J23 in the TEST position.

24. Disconnect W32 from A15J101. Monitor the sampler IF output (A15J101, SAMPLER IF) with a synthesized spectrum analyzer such as an 8568A/B or 8566A/B.

25. The sampler IF should measure between 46 MHz and 86 MHz at −15 dBm to +2 dBm. If the signal frequency or amplitude is incorrect, refer to "Unlocked Offset PLL" in this chapter.

26. Set jumper A14J23 in the NORMAL position. Reconnect W32 to A15J101.

Check FM loop sense (steps 27-34)

27. Set jumper A14J23 in the TEST position.

28. Set the spectrum analyzer to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

29. Connect an RF signal-generator output to A14J501. Set the signal generator to the following settings:

    Frequency .... 56 MHz
    Amplitude .... 0 dBm

30. Monitor A14J17 pin 1 with a DVM or oscilloscope. Connect ground to A14J17 pin 6.

31. As the signal generator frequency is increased to 76 MHz, the voltage at A14J17 pin 1 should change from approximately +12 V to −12 V.

32. Set the signal generator to the following settings and repeat step 30.

    Frequency .... 56 MHz
    Amplitude .... −15 dBm

33. If the voltage monitored in step 30 is correct with a 0 dBm output but not with −15 dBm output, suspect the limiting amplifier function block AE.

34. Place jumper A14J23 in the NORMAL position and reconnect W32 to A14J501.

Check YTO FM coil driver and main loop error voltage driver (steps 35-40)

35. To troubleshoot the YTO FM coil driver, refer to step 6 of "first LO Span Problems (2.01 MHz to 20 MHz)."

36. Steps 36 through 40 verify that the YTO-loop error voltage is reaching the FM coil. The main loop error voltage driver has a gain of either 1.5 or 15; the analyzer firmware controls the gain during the locking process. The error voltage is read by the ADC on the A3 interface assembly. U324D calibrates out any offsets from true ground. A14U326A inverts the sense of the YTO loop to lock the YTO on lower sampler-sidebands (YTO frequency (sampler frequency $\times$ sampler harmonic)). The fractional N frequency indicated in the FREQ DIAGNOSE menu will be negative when locking to lower sidebands. Refer to function blocks E, M, and N of A14 frequency control schematic in the *8560 E-Series Spectrum Analyzer Component Level Information Component Level Information*.

Set the spectrum analyzer to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

37. Remove jumper A14J23 and connect a dc power supply to A14J23 pin 2. Connect ground to A14J23 pin 3. Set the dc power supply to +7.5 Vdc.

38. Verify the nominal test-point voltages listed in Table 11-8 on page 565.

39. Change the input voltage to –7.5 volts and re-verify that the voltages listed in Table 11-8 on page 565 are the same except for a change in polarity.

40. Change the **CENTER FREQ** to 678.8 MHz with the SPAN remaining 0 Hz. This will change the switch setting of U326A and invert the voltages listed in Table 11-8 on page 565.

Table 11-8   **Voltages in FM Coil and Main Loop Drivers**

Measurement Points	Voltages
A14U405 pin 6	+2.8 Vdc
A14U322 pin 2	0 Vdc
A14J17 pin 4	>+10 Vdc

Check main coil coarse and fine DACs (steps 41-44)

41. The main coil coarse and fine DACs correct any initial pretune errors in the YTO main coil. The DACs adjust the FM-coil current to zero before any sweep begins. Refer to function block J of A14 frequency control schematic.

> Center frequency .... 300 MHz
> Span .... 0 Hz
> Trigger .... Single, EXT
> (with no external trigger connected)

Set the spectrum analyzer to the settings listed below. This sets both DACs to 128 (the DAC setting range is 0 to 255).

42. Press **SAVE**, **PWR ON STATE** and turn off the spectrum analyzer.

43. Place jumper A14J23 in the TEST position and turn on the spectrum analyzer.

Check main coil tune DAC (steps 45-49)

44. Verify the voltages listed in Table 11-9 on page 567.

Table 11-9   **Main Coil Coarse and Fine DACs Voltages**

Measurement Points	Voltages
A14J17 pin 2	–5 Vdc
A14J17 pin 3	–5 Vdc
A14J17 pin 5	+5 Vdc

45. Place jumper A14J23 in the NORMAL position.

46. Set the spectrum analyzer to the following settings:

Center frequency .... 300 MHz
Span .... 0 Hz

47. Place jumper A14J23 in the TEST position.

48. Measure the output of the main coil tune DAC (A14J18 pin 3) with a DVM. Refer to function block E of A14 frequency control schematic.

49. If the spectrum analyzer center frequency is 300 MHz, the voltage at A14J18 pin 3 should measure –3.35 V ±0.25 V. The voltage may also be determined from the following equation:

V = –(first LO Frequency –2.95 GHz) × 2.654 V/GHz

50. The voltage at A14U330 pin 2 should measure –3.4 V ±0.2 Vdc. This represents a current setting the YTO to approximately 2.95 GHz.

51. Return jumper A14J23 to the NORMAL position.

Unlocked Fractional N PLL

Operation

The fractional N oscillator is used in the 8563E as a reference for the first LO phase locked loop. It provides the 1 Hz start-frequency resolution for the first LO, and is the means by which the first LO is swept in LO spans of 2 MHz or less (fractional N spans). The prescaler, fractional N divider, and the postscaler are preset at power-on.

The PLL operates to produce an output frequency in the range of 60 MHz to 96 MHz selectable in 1 Hz increments. The output frequency can be swept (increasing or decreasing) over a selectable 100 Hz to 2 MHz range.

To determine the fractional N frequency for any given center frequency, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. The FRAC N FREQ frequency displayed is the frequency that will be measured at A14J304 with the 8563E in zero span.

Confirming an Unlocked Condition

1. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz

2. Connect A14J304 FRAC N TEST to the input of a synthesized spectrum analyzer and view the fractional N PLL output at 66.7 MHz.

NOTE

If a synthesized spectrum analyzer is not available, connect A14J304 to the input of a 20 dB gain amplifier, such as an 8447E. Connect the output of the amplifier to the input of a frequency counter.

---

3. If the fractional N oscillator measures a stable 66.7 MHz, the fractional N PLL is probably locked.

4. Check the two LEDs that are visible through the shield on A14. If either LED is lit, the fractional N PLL is not locked.

5. If either LED on A14 is lit, and no error message is displayed, check FC MUX U305. Refer to function block AH of A14 frequency control schematic.

6. If neither LED is lit, but the output frequency is wrong by more than 1 MHz, check the postscaler, function block AV.

7. Check that the postscaler is dividing properly. The frequency at A14J304 should be equal to the frequency at A14TP4 divided by either 5, 6, or 7. Refer to . To keep the divide number at a constant value set the spectrum analyzer to:

    Span .... 0 Hz
    Trigger .... Single, EXT

    (with no external trigger connected)

Table 11-10   **Postscaler Divide Numbers**

Divide Number	D11	D10	D9	Input Range (MHz) (A14J304)	Output Range (MHz) (A14TP4)
7	0	0	1	840 to 973	60.0 to 69.5
6	0	1	0	834 to 987.96	69.5 to 82.33
5	0	1	1	823.2 to 960	82.33 to 96.0

If the output frequency is wrong by less than 1 MHz, the phase locked loop is not unlocked but still requires repair. Continue with the "Fractional N Oscillator PLL" section.

Fractional N PLL

The fractional N PLL provides a synthesized frequency in the range of 60 MHz to 96 MHz. The 800 MHz to 1020 MHz voltage controlled oscillator (VCO) in the loop is divided down to lock with the 2.5 MHz reference. Simultaneously, the VCO is divided by two and then by either 5, 6, or 7 to generate the 60 MHz to 96 MHz output.

The prescaler (function block AR) supplies the clock signal for the fractional divider and is required for the fractional divider to operate. At the start of a fractional N sweep, the fractional divider is set to a value for the start frequency and a sweep rate. It then sweeps for as long as HSCAN is high. Use the following procedure to troubleshoot unlocked loop problems or problems of locking to the wrong frequency (by less than 1 MHz):

1. Check the two LEDs on A14 frequency control assembly. If either LED is lit, the fractional N phase locked loop is not locked.

2. The 10 MHz reference is required for fractional N operation. It is divided by four to 2.5 MHz in the reference divider circuitry, block AN. It is used to lock the divided voltage controlled oscillator (VCO) frequency. Check that the 10 MHz reference is present at A14J301. The 10 MHz reference is derived from the 600 MHz reference on the A15 RF assembly.

3. Change the spectrum analyzer from the fractional N span to 0 Hz.

4. Check the frequency at A14TP1. It should equal the value found by pressing **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **RAW OSC FREQ**.

5. Check the tune voltage at R240 in function block AQ.

6. Look up the expected problem area in Table 11-11 on page 570 with the information from steps 4 and 5. Go to the appropriate troubleshooting steps.

Table 11-11   **Unlocked Fractional N Troubleshooting Areas**

Measured VCO Frequency Relative to Expected Value	Tune Voltage				
	Below −4 V	About −3.3 V	Between −2 V and +10 V	About +11 V	Above +12.5 V
Measured > expected	VCO clamp	VCO	Divider or integrator	Divider or integrator	VCO clamp
Measured < expected	VCO clamp	Divider or integrator	Divider or integrator	VCO	VCO clamp
Measured, not oscillating	VCO clamp	VCO	VCO	VCO	VCO clamp

7. VCO clamp troubleshooting: Q131, Q132 and the associated components should limit the tune voltage at R240 to about ±11 V. If the integrator (its output voltage is on TP13) tries to produce a voltage outside this range, excess current is shunted through CR131 and Q131 for positive excursions or CR132 and Q132 for negative excursions. The bases of these transistors should be at about ±9.6 V for proper operation.

8. VCO troubleshooting: Check the dc biases in the VCO function block. The bias voltages, for some points in the VCO, are indicated in Figure 11-8 on page 571.

9. Divider and integrator troubleshooting: Measure the frequency of the pulses at TP6 in block AO. Look up the expected problem area in Table 11-12 on page 572 and go to the appropriate troubleshooting steps.

Figure 11-8   VCO Bias Voltages

sz139e

Table 11-12   **Divider and Integrator Troubleshooting**

Measured VCO Frequency Relative to Expected Value	TP6 Frequency			
	zero	<2.5 MHz	2.5 MHz	>2.5 MHz
Measured > expected	Dividers	Dividers	Dividers	Det or integrator
Measured < expected	Both	Det or integrator	Dividers	Dividers

10. Divider troubleshooting:

a. Check the frequency at A14TP2. It should be equal to the frequency at A14TP1 divided by two.

b. The signal at A14TP3 should be above –14 dBm.

c. Use an analog oscilloscope to view the signal at A14TP5. Adjust the scope triggering to view the divide-by-16 signal. The frequency at this point will be varying as the prescaler changes its divide number to either 16, 17, 20, or 21. The prescaler uses 16 as the divide number most frequently. The frequency displayed on the oscilloscope should equal the frequency from TP2 divided by 16.

d. Use an oscilloscope to view the signal at pin 8 of U112. Its average frequency should be given by:

$f = f(A14TP5) \times 80 \text{ MHz/RAW OSC FREQ}$

where: f(A14TP5) is the frequency measured at TP5, and RAW OSC FREQ comes from step 4.

If the frequency is in error, the fractional divider, block AS, is not functioning. Check that FRAC N RUN on U113 pin 39 is high.

e. Use an oscilloscope to verify that the signals at N_in (U112 pin 8) and N_out (TP6) are identical except for a sub-microsecond delay.

11. Detector and integrator troubleshooting:

   a. Check the phase detector output on TP11 in block AO. If F_ref is higher in frequency than TP6 (reclocked VCO/N), then the average voltage at TP11 should be positive by 0.05 V to 10 V. If F_ref is lower, TP11 should be –0.05 V to –10 V.

   b. The polarity of the output of the loop gain (block AP, TP12) should be the same as the polarity of the input (TP11). The integrator op amp (U106) output (TP13) should try to go very positive (about +12 V) if its average input (TP12) is positive. If its average input is negative, it should try to go very negative (about –12 V). If its average input is zero and it is functioning correctly, it may take on any output voltage between –12 V and +12 V.

Frequency Span Accuracy Problems

The spectrum analyzer employs lock-and-roll tuning to sweep the first LO for spans greater than 2.0 MHz. The first LO is locked to the start frequency immediately after the previous sweep has been completed. The first LO is then unlocked, and, when a trigger signal is detected, the first LO sweeps (rolls).

When there is a considerable delay between the end of one sweep and the beginning of the next, the actual first LO start frequency may differ from the locked start frequency. This start frequency drift will be most noticeable in a 2.01 MHz LO span (the narrowest FM coil span). This drift is not noticeable in either free run or line trigger modes.

The sweep is generated by different oscillators in the synthesizer section depending on the desired span of the first LO (this is not necessarily the same as the span setting of the analyzer, due to harmonic mixing). Refer to Table 11-13 on page 574 for a listing of sweep-signal destinations versus first LO spans.

Sweeping the fractional N oscillator results in sweeping the YTO FM coil. There is a one-to-one relationship between the fractional N oscillator frequency span and the span of the first LO. The fractional N oscillator sweep is generated digitally. The oscillator is always synthesized, rather than employing lock and roll tuning.

Table 11-13   **Sweep Signal Destination versus Span**

First LO Span	Sweep Signal Destination
>20 MHz	A11 YTO main coil
2.01 MHz to 20 MHz	A11 YTO FM coil
≤2 MHz	None Fractional N oscillator sweeps without a sweep ramp signal.

Determining the First LO Span

The span of the first LO depends on the spectrum analyzer harmonic-mixing number. Use the following steps to determine the first LO span:

1. Read the span setting displayed on the spectrum analyzer.

2. Determine the harmonic-mixing number from the information in .

Table 11-14 **Harmonic Mixing Number versus Center Frequency**

Center Frequency	Harmonic Mixing Number
9 kHz to 2.9 GHz	1
2.75 GHz to 6.46 GHz	1
5.86 GHz to 13.2 GHz	2

3. Use the following equation to determine the first LO span used.

$$\text{First LO Span } = \frac{\text{Display Span Setting}}{\text{Current Band Harmonic Mixing Number}}$$

4. Refer to to determine the circuit associated with the span.

Confirming Span Problems

1. If all first LO spans or only first LO spans of 2.01 MHz or above are affected, perform .

    *   On the spectrum analyzer press **CAL**, **REALIGN LO &IF**, and retest all spans.

    *   If the YTO adjustment has sufficient range and only LO spans of 2.01 MHz or above are faulty, test YTO linearity by performing step c.

    *   Test the span in question at different center frequencies in the same band. If the span accuracy changes significantly (2% or more), suspect the A11 YTO.

2. If only first LO spans of 2 MHz or less are faulty, suspect the A14 fractional N PLL.

3. If there are several spans in the main coil and FM coil ranges affected, suspect the A14 span attenuator.

YTO Main Coil Span Problems (LO Spans >20 MHz)

For YTO main coil spans, the YTO is locked at the beginning of the sweep and the sweep ramp is summed into the main coil tune driver.

1. Perform "7. YTO Adjustment" on page 87. If the YTO adjustments cannot be performed, continue with step 2.

2. Set the spectrum analyzer to the following settings:

   Start frequency .... 10 MHz
   Stop frequency .... 2.9 GHz

3. Verify that a –1.2 V to –4.8 V ramp (approximately) is present at A14U331 pin 2.

4. If this ramp is not present, troubleshoot the main/FM sweep switch. See function block H of A14 frequency control schematic.

5. Measure the output of the main coil tune DAC at A14J18 pin 3. At the frequency settings of step 2, this should be –2.48 V. If the voltage is not –2.48 V, troubleshoot the main coil tune DAC. See function block E of A14 frequency control schematic.

YTO FM Coil Span Problems (LO Spans 2.01 MHz to 20 MHz)

In YTO FM coil spans, the YTO loop is locked and then opened while the sweep ramp is summed into the FM coil. The FM coil sensitivity is corrected by changing the sensitivity of the FM coil driver.

1. Perform "7. YTO Adjustment" on page 87. If the YTO adjustments cannot be performed, continue with this procedure.

2. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 20 MHz
   Sweep time .... 50 ms

3. Check for the presence of a 0 V to –10 V sweep ramp at A14J15 pin 14 (input to the main/FM sweep switch). Refer to function block H of A14 frequency control schematic.

4. Check for the presence of a 0 V to +5 V sweep ramp at A14U405 pin 6 (YTO FM coil driver). Refer to function block M of A14 frequency control schematic.

5. Check the state of the Main/FM sweep switches as indicated in Table 11-15 on page 577.

6. The rest of the procedure troubleshoots the YTO FM coil driver.

   Refer to function block M of A14 frequency control schematic.

Table 11-15   **Settings of Sweep Switches**

Switch	Switch State	Switch Control Line (Pin #)	Control Line State (TTL)
U318A	Closed	1	High
U318B	Open	8	Low
U318C	Closed	9	Low
U318D	Open	16	High

7. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Trigger .... SINGLE, EXT

   a. On the spectrum analyzer, press **SAVE**, **SAVE STATE**, **STATE 0**.

   b. Remove jumper A14J23 and connect a dc voltage source to A14J23 pin 2. Connect the voltage source ground to A14J23 pin 3.

   c. Connect a microwave frequency-counter or another spectrum analyzer to the spectrum analyzer first LO OUTPUT (front panel output).

   d. Set the dc-voltage source output for 0 Vdc and note the 1st LO frequency.

   e. Set the dc-voltage source output for +10 Vdc. The first LO frequency should momentarily increase approximately +15.6 MHz.

   f. The voltage at A14U332 pin 2 should be approximately 19% of the voltage at A14J23 pin 2.

   g. If the first LO frequency did not change in step e, press **LINE** to turn spectrum analyzer off and disconnect W10 from A14J3.

h. Place a jumper between A14J3 pins 9 and 10. Place a 50 Ω, 3 watt resistor across A14J3 pins 5 and 6 (resistor, part number 0811-1086). Press **LINE** to turn spectrum analyzer on.

i. On the spectrum analyzer, press **RECALL**, **STATE**, **STATE 0**.

j. If the voltage at U332 pin 2 is correct with A14J3 pins 9 and 10 shorted, but was incorrect with W10 connected, the YTO FM coil is probably open; replace the A11 YTO.

k. Replace jumper A14J23.

Fractional N Span Problems (LO Spans ≤2 MHz)

If the fractional N spans are inaccurate or non-existent, but the fractional N PLL is locked to the correct frequency and other spans are correct, there may be a problem with the HSCAN signal. Check that HSCAN is present at the fractional divider, U113 pin 41 in function block AS. HSCAN comes from the A3 interface assembly and goes to the sweep generator circuitry in function block A and to fractional N.

First LO Span Problems (All Spans)

1. Set the spectrum analyzer to the following settings:

Center frequency	300 MHz
Span	2 MHz
Resolution BW	1 MHz
Video BW	1 MHz
Sweep time	50 ms

2. Check that there is 0 V to +10 V ramp of 50 ms duration at A14J15 pin 15.

3. If a scan ramp is not present, refer to "Sweep Generator Circuit" on page 585.

4. If there is a 0 to −10 V ramp at A14J15 pin 14, the fault is probably in the Main/FM sweep switch. See function block H of A14 frequency control schematic.

5. Check that there is a 0 V to +10 V ramp at U325 pin 1. The spectrum analyzer ADC obtains information about the sweep from this node.

Check span attenuator (steps 6-13)

6. Continue with step 7 to check the span attenuator. See function block L of A14 frequency control schematic.

7. With the spectrum analyzer set to the settings in step 1, monitor A14U323 pin 6 with an oscilloscope. A 0 V to −10 V ramp should be present.

8. Change the spectrum analyzer span to 1 MHz and check for a 0 V to −5 V ramp at U323 pin 6.

9. Change the spectrum analyzer span to 400 kHz and check for a 0 V to −2 V ramp at U323 pin 6.

10. Set the spectrum analyzer to the following settings:

Start frequency .... 10 MHz
Stop frequency .... 2.9 GHz
Sweep time .... 80 ms

11. Monitor A14J15 pin 14 for a 0 V to −7.5 V ramp. Switches U317A, U317B, and U317D should be open and U317C should be closed.

12. Change the spectrum analyzer SPAN to 365 MHz and check for a 0 mv to −1.0 V ramp at A14J15 pin 14. Switch U317C should be open and U317B closed.

13. Change the spectrum analyzer SPAN to 36.5 MHz and check for a 0 mV to −100 mV ramp at A14J15 pin 14. Switch U317B should be open and U317A closed.

Check current source (steps 14-21)

14. Check the sweep generator current source with the following steps (function block A of A14 frequency control schematic).

15. Set the spectrum analyzer to the following settings:

Center frequency .... 300 MHz
Span .... 1 MHz
Sweep time .... 50 ms

16. Use a DVM to monitor the voltage at A14J18 pin 4. The voltage should measure approximately −8.45 Vdc.

17. Set the spectrum analyzer sweep time to 100 ms. The voltage at J18 pin 4 should measure approximately −4.21 Vdc.

18. Set the spectrum analyzer sweep time to 200 ms. The voltage at J18 pin 4 should measure approximately −2.1 Vdc.

19. The analog switches and comparators should be set as listed in Table 11-16 on page 580.

20. Check that U312D opens when the sweep time is set to 2 seconds.

21. Check that U312B and U312C close when the sweep time is set to 20 seconds.

Table 11-16   **Settings for Switches and Comparators**

Sweep Time	Switch U312B	Switch U312C	Switch U312D	Comparator U319A Pin 1	Comparator U319B Pin 7
200 ms	Open	Open	Closed	High	High
2 s	Open	Open	Open	High	High
20 s	Closed	Closed	Open	High	High

First LO Span Problems (Multiband Sweeps)

During multiband sweeps, the sweep ramp at A14J15 pin 15 should go from 0 V to +10 V for each band or portions of a band covered. See function block A of A14 frequency control schematic in the *8560 E-Series Spectrum Analyzer Component Level Information* binder. However, the scan ramp at A14U325A pin 1 is scaled according to the percentage of the total span that the band is covering. See function block B of A14 schematic. Also, the sum of the individual ramps is 10 V. Figure 11-9 on page 580 illustrates both sweep and the scan ramp for a 0 GHz to 13.2 GHz span with instrument preset conditions.

Figure 11-9   **8562E/EC Sweep and Scan Ramps**
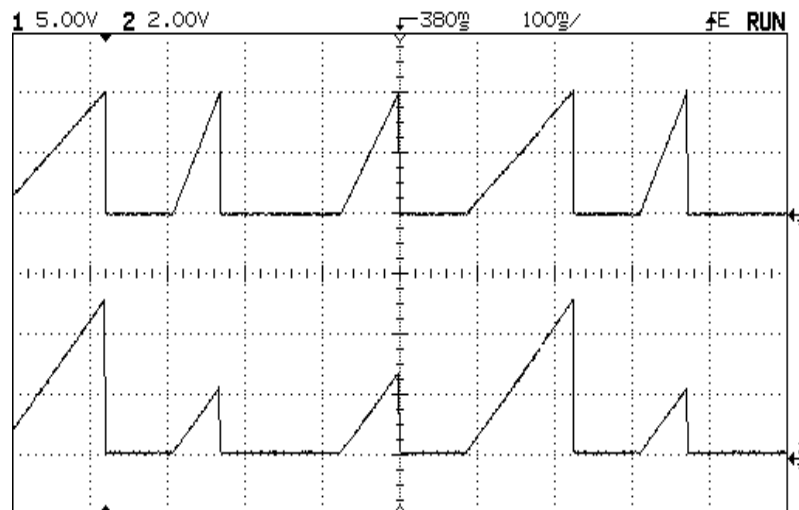
Phase Noise Problems

System phase noise can be a result of noise generated in many different areas of the spectrum analyzer. When the spectrum analyzer is functioning correctly, the noise can be observed as a function of the distance away (the offset) from the carrier frequency. The major contributor to system noise can be characterized as coming from specific circuit areas depending upon the offset frequency.

Some very general recommendations can be made for identifying which circuitry is the cause of the noise at certain offsets. The recommendations below apply with a center frequency of 1 GHz.

Table 11-17   **Settings for Switches and Comparators**

Carrier Frequency Offset	Major Contributor (when working correctly)
100 Hz	Reference (OCXO or TCXO)
1 kHz	600 MHz reference PLL
3 kHz	Fractional N PLL
10 kHz to 150 kHz	Offset lock loop or YTO loop
>150 kHz	YTO

Phase Noise in Locked versus Unlocked Spans

Input a signal to the spectrum analyzer. Set the center frequency to the input signal frequency, set the span to 2 MHz, and plot the display. This plots the system noise for a locked sweep. Plot the display again with a span of 2.01 MHz (lock and roll sweep).

The crossover point of the noise floor of the two plots is typically at an offset of about 50 kHz, for a functioning instrument.

If the crossover point is shifted out to a higher offset frequency, suspect the YTO loop circuitry.

If the crossover point is shifted in to a lower offset frequency, suspect the offset or fractional N loop circuitry.

Reference versus Reference PLL Phase Noise

If the problem seems to be in the frequency reference or reference PLL circuitry, measure the noise with internal and external references. If there is no difference, suspect the circuitry associated with the SAWR A15U701.

Fractional N versus Offset PLL or YTO PLL Phase Noise

If the spectrum analyzer has excessive noise at >1 kHz offset, measure the noise with center frequencies of 100 MHz and 2.5 GHz.

If the measurements are equal, suspect the fractional N circuitry and the YTO loop circuitry on the A14 frequency control assembly.

If the measurements differ by 2 dB to 5 dB, with the 2.5 GHz measurement at a higher noise level, suspect the offset lock loop circuitry.

Fractional N PLL Phase Noise

Check the noise on the 5 V regulators on A14, particularly the regulator in the reference divider circuitry A14U121. Refer to function block AN on the A14 frequency control assembly schematic.

- The noise level of the voltage regulator should be <1 mV. The typical noise level is 40 μV RMS between 10 Hz and 100 kHz.

- A coaxial probe with very little unshielded tip area should be used to avoid picking up radiated 60 Hz. Check that your measurement is valid by probing ground on the circuit and verifying that the measured value is well under the 1 mV threshold that indicates a defective regulator.

There can also be phase noise problems if the loop gain is incorrect. See function block AP for loop gain troubleshooting information.

Sampler and Sampler IF

The A15U100 sampler creates and mixes harmonics of the sampling oscillator with the first LO. The resulting sampler IF (60 MHz to 96 MHz) is used to phase-lock the YTO. The sampler IF filters unwanted products from the output of A15U100 and amplifies the IF to a level sufficient to drive the YTO loop. When the IF is between 78 and 87 MHz, PIN diodes switch a 120 MHz notch filter in the sampler IF section.

1. Set the spectrum analyzer to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz

2. Disconnect W32 from A15J101.

3. Connect the input of a power splitter to A15J101. Connect W32 to one of the splitter outputs. Connect the other splitter output to the input of another spectrum analyzer.

4. If a 66.7 MHz signal, greater than −15 dBm, is not displayed on the other spectrum analyzer, set a microwave source to the following settings:

   Frequency .... 4.2107 GHz
   Amplitude .... −5 dBm

5. Connect the microwave source to A15U100J1. A 66.7 MHz signal at approximately 0 dBm should be displayed on the other spectrum analyzer.

6. Use an active probe/spectrum analyzer combination to measure the signal at the following test points:

A15TP101	66.7 MHz, −8 dBm
A15TP201	296 MHz, +9 dBm

7. If a correct signal is seen at A15TP201 but the signal at A15TP101 is wrong, proceed as follows:

    * Use an oscilloscope to measure the signals at the following test points:

      A15J400 pin 1 +0.8 Vdc to +1.6 Vdc (≤0.5 Vp-p variation)

      A15J400 pin 3 −0.8 Vdc to −1.6 Vdc (≤0.5 Vp-p variation)

    * If these levels are wrong, perform the "Power and Sampler Match Adjustments" in the sampler oscillator adjustment procedure. Refer to Chapter 2 , "Adjustment Procedures."

    * If adjusting the sampler match does not bring the signal at A15TP101 within specification when the signal at A15TP201 is correct, the A15U100 sampler is defective.

8. The sampler IF signal at A15J101 is 60 MHz to 96 MHz at −10 dBm to +5 dBm. If the signal at A15TP101 is correct, but the signal at A15J101 is wrong, the fault lies in the sampler IF circuitry. Continue with the following steps.

9. Set the 8563E to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

10. Set a microwave source to the following settings:

    Frequency .... 4.2107 GHz
    Amplitude .... −5 dBm

11. Connect the microwave source to A15U100J1.

12. Measure the signal at U103 pin 1 using an active probe/spectrum analyzer combination.

13. If a 94.7 MHz signal, approximately −14 dBm, is present, but the signal at A15J101 is low, suspect U103.

14. When U104 pin 3 is at TTL low, U104 pin 6 should near −15 Vdc and PIN diodes CR101, CR102, and CR103 should be reverse-biased.

15. Set 8563E to the following settings:

    Center frequency .... 89.3 MHz
    Span .... 0 Hz

16. Check that U104 pin 3 is at a TTL high and U104 pin 6 is greater than +7 V. PIN diodes CR101, CR102, and CR103 should all be turned on with about 7 mA of forward current.

17. Disconnect the power splitter and reconnect W32 to A15J101.

Sweep Generator Circuit

The sweep generator circuitry generates a ramp from 0 to 10 volts during the sweep time. The available sweep times range from 50 μs to 2,000 seconds. The sweep times are generated in two different ranges, a 50 μs to 30 ms range and a 50 ms to 2,000 second range. The 50 μs to 30 msec range is only needed for analog zero span sweeps.

The sweep generator is controlled with an 8-bit latch and the control signal HSCAN. The latch, U308, controls the sweep rate. HSCAN determines when to reset the scan ramp and when to let it sweep.

Operation of the 50 ms to 2,000 second range will be described using a 50 ms sweep time as the example. For a 50 ms sweep time, Q1 shorts out C16. The D to A converter U307, has zero output current. U334A is a buffer with zero offset, because there is no current coming out of U307. The buffering of U334 makes the base-emitter voltages on Q3A and Q3B the same. These two transistors are matched, so their collector currents should be identical when their base-emitter voltages are identical. The emitter current of Q3B is 200 μA, therefore the emitter current of Q3A is 200 μA and the sweep ramp is generated by C14. The sweep time is given by the formula:

$$sweeptime \ = \ capaci\tan ce(C14)\frac{\Delta V}{current}$$

The DAC setting is increased for longer sweep times. This increases the current sunk by the DAC output U307 pin 4, which increases the emitter voltage on Q3A, decreasing the base-emitter voltage drop. Q3A acts as an exponentiator and reduces its collector current, creating a slower sweep ramp.

For the shorter sweep times, 50 μs to 30 ms, Q1 is opened putting C16 in series with C14. This changes the effective capacitance from 1 μF to 1,000 pF, or a reduction of 1,000 to 1.

The HSCAN signal uses Q2 to reset the ramp. Q2 shorts the integrator and sets its output nominally to ground.

Figure 11-10   Simplified Synthesizer Section
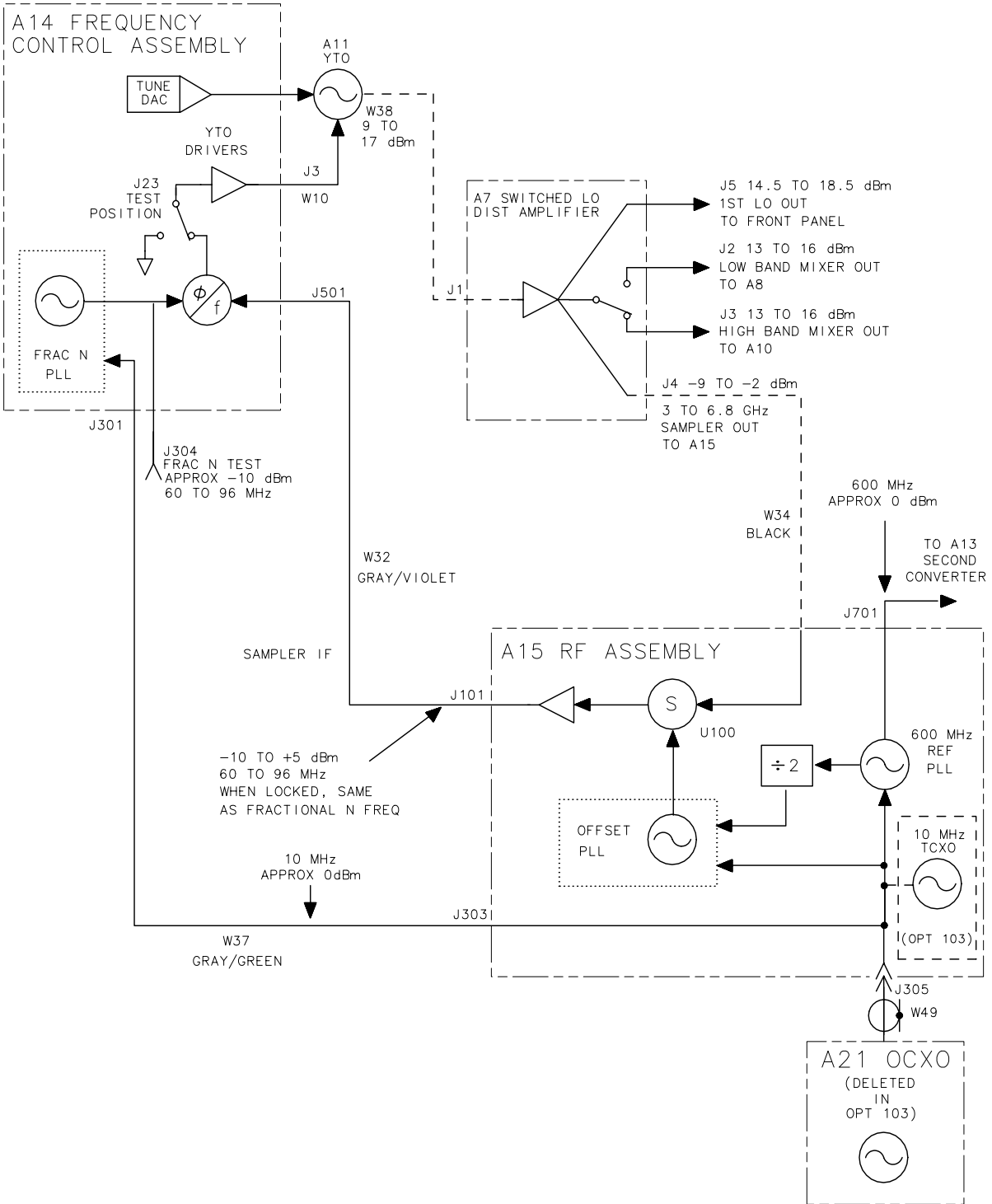
Figure 11-11   Simplified A14 Assembly Block Diagram
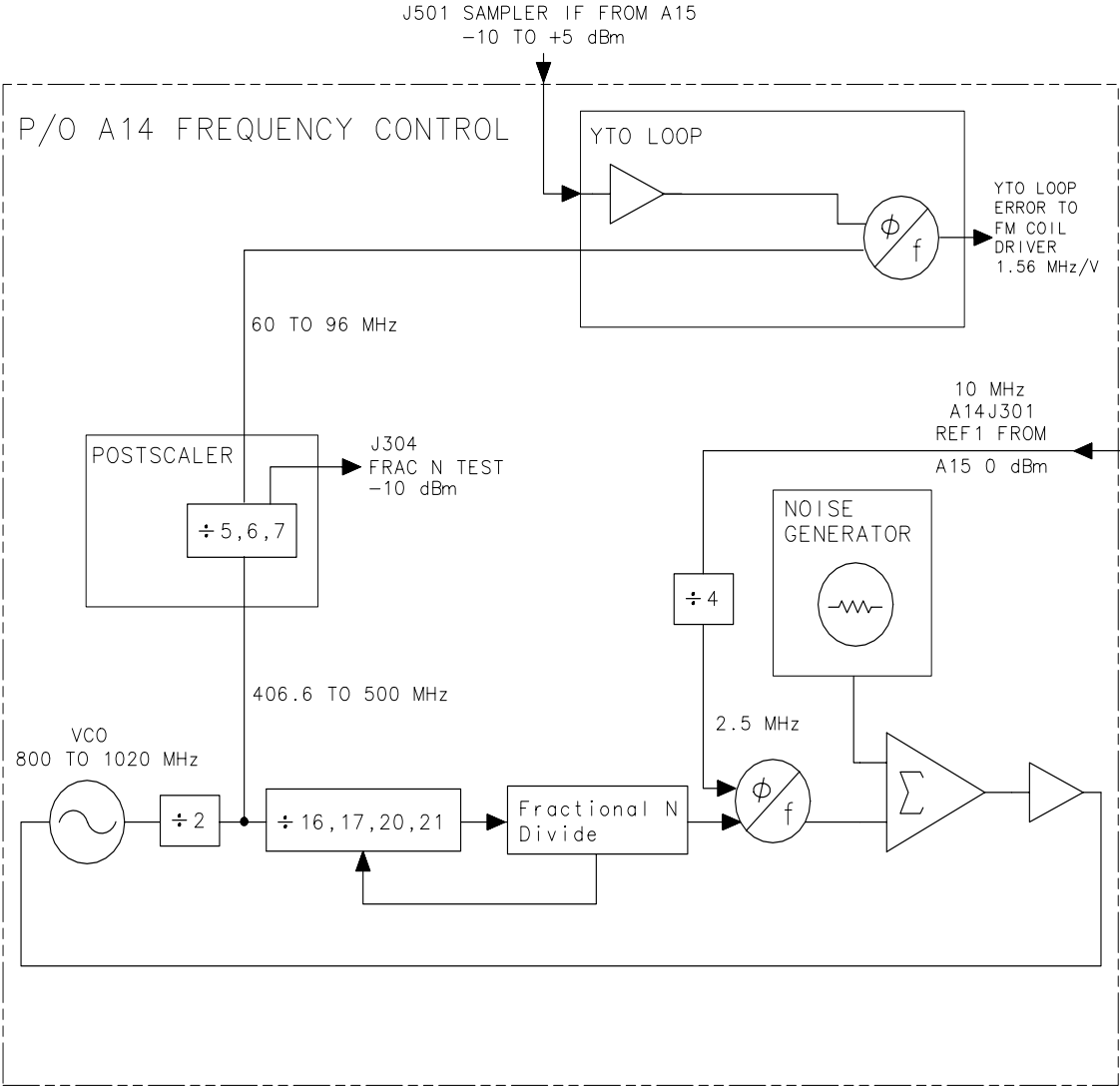
sp135e

Figure 11-12   **Simplified A15 Assembly Block Diagram**
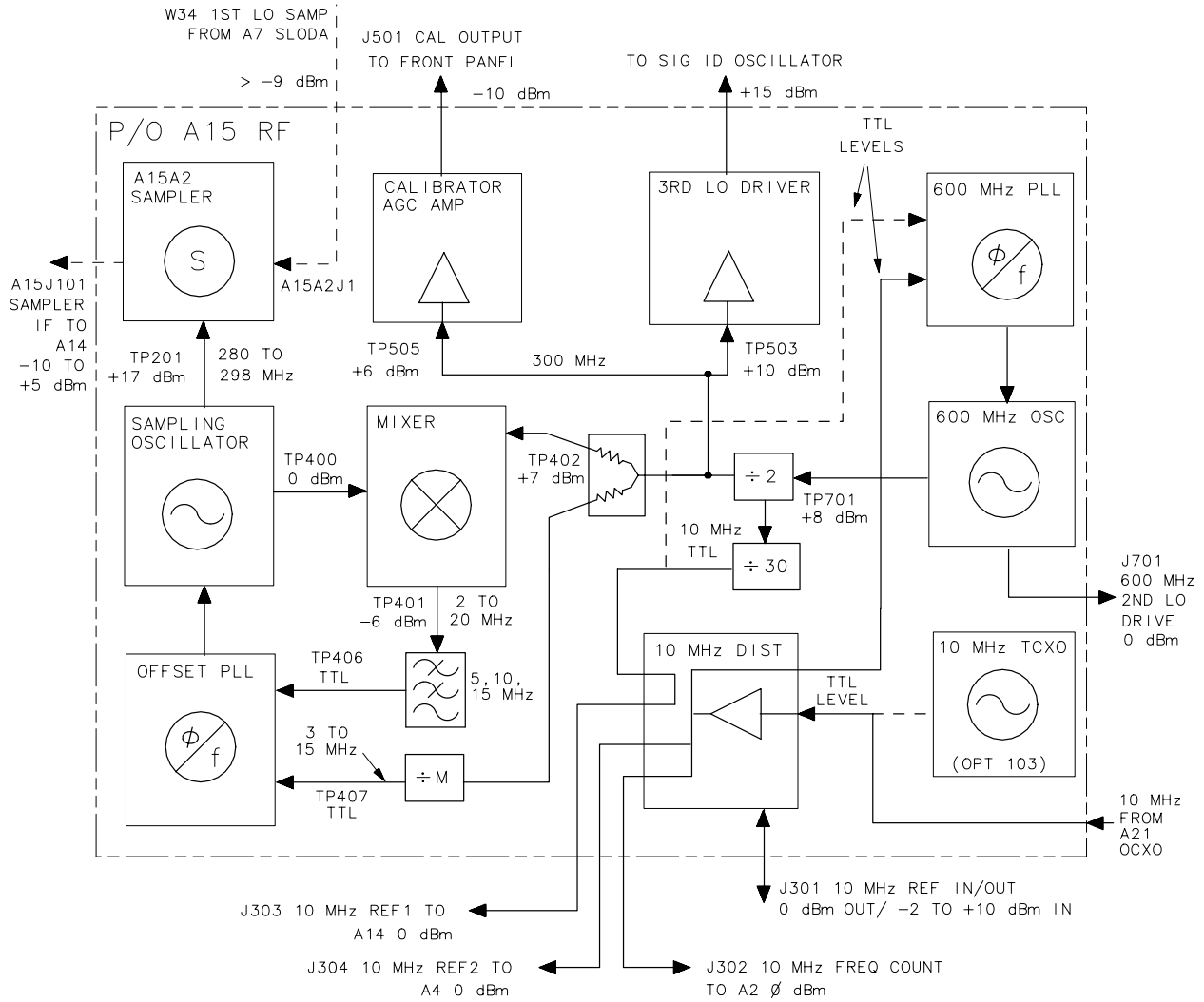
si122e

A21 OCXO

The spectrum analyzer uses an oven-controlled crystal oscillator (OCXO). It is deleted in Option 103 and replaced by a temperature-compensated crystal oscillator (TCXO), located on the A15 RF assembly. Connectors J305 and J306 on the A15 RF assembly are located where the TCXO would be installed in an Option 103. The oven in the OCXO is powered only when the spectrum analyzer is powered on; there is no standby mode of operation. The OCXO oscillator operates only when the internal frequency reference is selected. Control line HEXT (High = EXTernal frequency reference) is inverted by A15U303B to generate LEXT. (Refer to the A15 RF assembly schematic diagram, block M, sheet 2 of 4.) LEXT is sent to the OCXO via A15J306 pin 4. When LEXT is low, the oscillator in the OCXO will be turned off.

Replacement OCXOs are factory adjusted after a complete warmup and after the specified aging rate has been achieved. Thus, readjustment should typically not be necessary after OCXO replacement, and is generally not recommended.

If adjustment is necessary, the spectrum analyzer must be on continuously for a minimum of 24 hours immediately prior to oscillator adjustment to allow both the temperature and frequency of the oscillator to stabilize. Failure to allow sufficient stabilization time could result in oscillator misadjustment.

Check operation of the A21 OCXO as follows:

1. Disconnect W49 (Coax 82) from A15J305. Connect the output of W49 to the input of another spectrum analyzer.

2. Check that the fundamental frequency is 10 MHz and that the power level is 0 dBm ±3 dB. Also check that the harmonics are at least −25 dBc. Excessive harmonics can generate spurious responses on the fractional N oscillator on the A14 frequency control assembly.

3. If the OCXO has no output, check A15J306 pin 1 for +15 Vdc. Check A15J306 pin 4 for a TTL-high level.

4. If A15J306 pin 4 is at a TTL-low level, press **AUX CTRL** and **REAR PANEL**. Press **10 MHz EXT INT** until INT is underlined. A15J306 pin 4 should read a TTL-high level. Press **10 MHz EXT INT** until EXT is underlined. A15J306 pin 4 should read a TTL-low level.
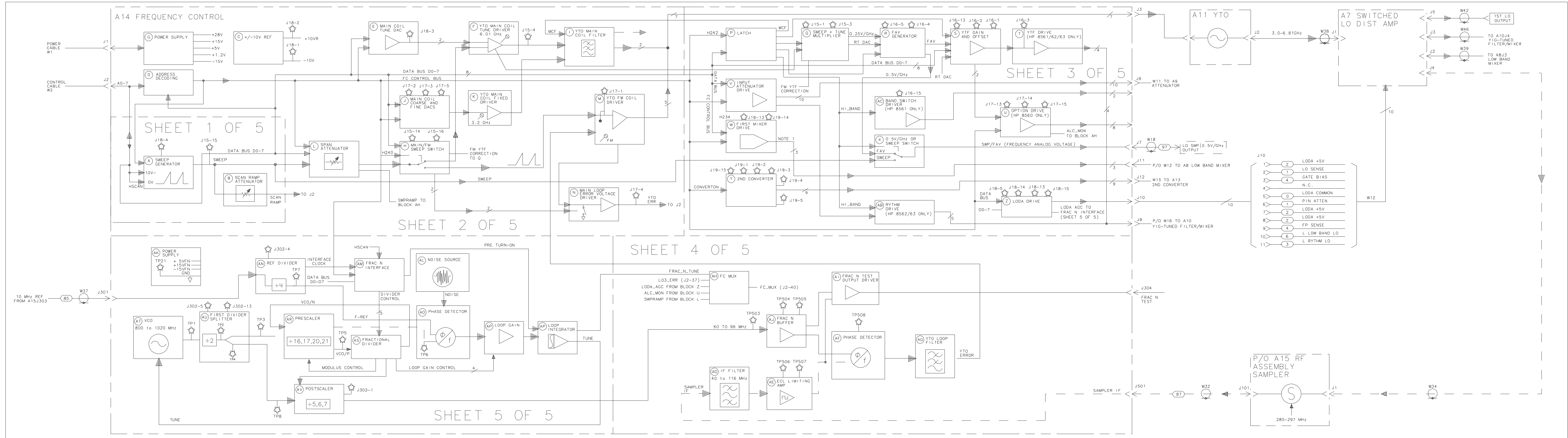
FIGURE 11-14. RF ASSEMBLY BLOCK DIAGRAM

12   RF Section

Introduction

The RF Section converts the input signal to a 10.7 MHz IF (Intermediate Frequency). See the detailed block diagram, Figure 12-8 on page 627.

NOTE   The block diagrams for the A14 and A15 assemblies are located in Chapter 11 , "Synthesizer Section."

CAUTION   All of the RF assemblies are extremely sensitive to Electrostatic Discharge (ESD). For further information regarding electrostatic cautions, refer to "Electrostatic Discharge" on page 32.

CAUTION   Use of an active probe, such as an 85024A, with another spectrum analyzer is recommended for troubleshooting the RF circuitry. If an 1120A Active Probe is being used with a spectrum analyzer, such as the 8566A/B, 8569A/B and the 8562A/B, having dc coupled inputs, either set the active probe for an ac coupled output or use a dc blocking capacitor (11240B) between the active probe and the spectrum analyzer input. Failure to do this can result in damage to the analyzer or to the probe.

Troubleshooting Using the TAM

Refer to Chapter 7 , "General Troubleshooting," for information on enabling the TAM for use with the 8562E/EC Spectrum Analyzer.

When using Automatic Fault Isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 12-1 on page 599 to locate the manual procedure.

Table 12-2 on page 600 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 12-1 on page 598 illustrates the location of the A15 test connectors.

Figure 12-1 **A14 and A15 Test Connectors**
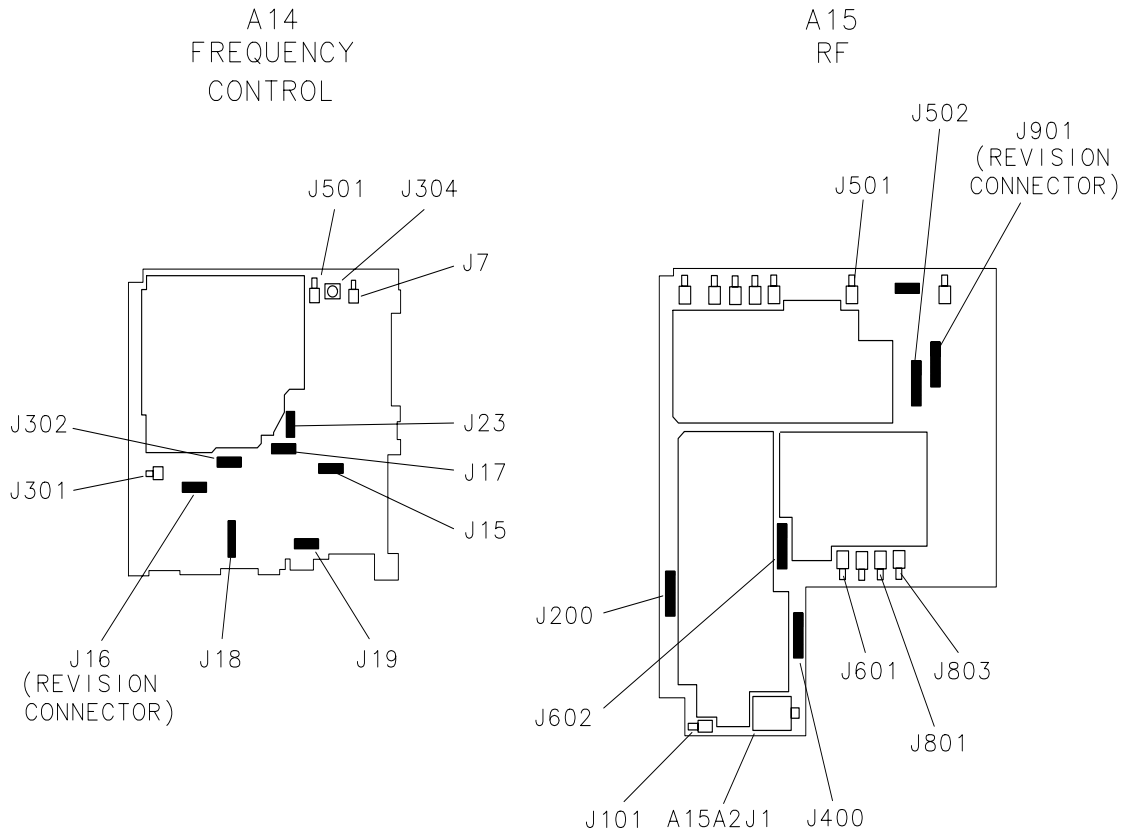
sp128e

Table 12-1   **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check 2nd IF Amplifier	Third Converter
Check 2nd IF Distribution	Third Converter
Check 10.7 MHz IF Out of Double Balanced Mixer	Third Converter
Check 300 MHz CAL OUTPUT	Calibrator Amplitude Adjustment in Chapter 2
Check A7 First LO Distribution Amplifier	A7 SLODA (Switched LO Distribution Amplifier)
Check A8 Low Band Mixer	A8 Low Band Mixer
Check A9 Input Attenuator	A9 Input Attenuator
Check A13 Second Converter	A13 Second Converter
Check A13J2 INT 2nd IF	A13 Second Converter *(steps 1 to 6)*
Check A14 Latch	Control Latch for Band-Switch Driver
Check A15 Control Latches	Control Latches
Check A15J601 10.7 MHz	Third Converter Output
Check External 10 MHz Reference Operation	10 MHz Reference *(steps 5 to 11)*
Check Gain of Flatness Compensation Amplifier	Third Converter
Check INT 10 MHz Reference Operation	10 MHz Reference *(steps 1 to 4)*
Check LO Feedthrough	Low Band Problems *(steps 1 to 3)*
Check LO Power	Low and High Band Problems *(steps 4 to 9)*
Check PIN Switches in SIG ID Oscillator (Opt 008)	SIG ID Oscillator (Opt 008 Only)
Check Second Converter Control	A13 Second Converter
Check SIG ID Oscillator (Opt 008)	Signal ID Oscillator Adjustment in Chapter 2
Check SIG ID Oscillator Operation (Opt 008)	SIG ID Oscillator (Opt 008 Only)
Check Third Converter	Low and High Band Problems *(step 10)*

Table 12-2 **TAM Tests versus Test Connectors**

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A14J16	YTF Offset DAC YTF Gain and Offset Input YTF Gain DAC YTF Drive Band Switch Driver	MS6 MS2 MS1 MS3 MS8
A14J17	Main Coil Coarse DAC	MS3
A14J18	LODA Drive	MS5, MS6, MS7, MS8
A14J19	Second Conv PIN Switch Second Conv Mixer Bias Second Conv Drain Bias Second Conv Doubler Bias Second Conv Driver Bias First Mixer Drive Switch First Mixer Drive DAC	MS8 MS1 MS3 MS4 MS5 MS7 MS6
A14J302	Revision	MS7
A15J400	IF AMP/Limiter Bias	MS6
A15J502	Third LO Tune Voltage 3rd LO Driver Amp	MS3 MS1, MS8
A15J602	SIG ID Collector Bias RF Gain Control Test	MS7 MS1, MS3
A15J901	Revision External Mixer Switch Signal ID Switch External Mixer Bias	MS3 MS1, MS8 MS5, MS6 MS7

Low Band Problems

1. Disconnect all inputs from the front-panel INPUT 50Ω connector.

2. Set the 8562E/EC to the following settings:

   Center frequency .... 0 Hz
   Span .... 1 MHz
   Input attenuator .... 0 dB

3. The LO feedthrough amplitude observed on the display should be between −6 and −30 dBm.

The marker will not PEAK SEARCH on the LO Feedthrough when in a non-zero span. To measure the LO Feedthrough amplitude with the markers, set the SPAN to 0 Hz and **CENTER FREQ** to 0 Hz. Press **MKR** ON.

4. If the LO feedthrough amplitude is within limits, but signals are low, the RF path following the A8 mixer is probably operating properly.

5. If the LO feedthrough amplitude is higher than −5 dBm (signal will be "clipped" at top of screen) and signals are low in amplitude, suspect a defective A8 mixer assembly.

6. Perform the steps located in "Control Latch for Band-Switch Driver" on page 612.

7. Check A13 second converter mixer diode bias at A14J19 pin 1. The bias voltage should be between −150 and −800 mVdc.

8. Troubleshoot the signal path. Refer to the power levels listed on Figure 12-8 on page 627, 8562E RF Section Troubleshooting Block Diagram.

High Band Problems

1. Perform the steps located in .

2. Troubleshoot the signal path. Refer to the power levels listed in , 8562E RF Section Troubleshooting Block Diagram.

Low and High Band Problems

1. On the 8562E/EC, press **PRESET** and **REALIGN LO &IF**. If any error messages are displayed, refer to "Error Messages" on page 319.

2. Perform "15. External Mixer Amplitude Adjustment (Non-Option 327)" on page 111. If this adjustment cannot be completed, perform the steps located in "Third Converter" on page 618.

3. Perform the "First LO OUTPUT Amplitude" performance test. (Refer to the *8560 E-Series Spectrum Analyzer Calibration Guide* or use TAM functional test.)

4. If the performance test fails, perform "8. LO Distribution Amplifier Adjustment" on page 90. If the adjustment fails, set the 8562E/EC to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz

5. Place the jumper on A14J23 in the TEST position. Remove W38 from the input of A7.

6. Use a power meter or another spectrum analyzer to measure the output of A11 YTO. The power should be between +2 dBm and +13 dBm.

7. Reconnect W38 to A7. Place the jumper on A14J23 in the NORM position.

8. If ERR 334 (unlevelled output) is present and the A11 YTO power output is correct, the A7 drive circuit may be defective. Refer to "A7 LO Distribution Amplifier" on page 604.

9. Troubleshoot the signal path. Refer to the power levels listed on Figure 12-8 on page 627, 8562E RF Section Troubleshooting Block Diagram.

10. Check Third Converter as follows:

   a. On the 8562E/EC, press **PRESET** and set the controls as follows:

      Center frequency .... 300 MHz
      Span .... 0 Hz

   b. Inject a −28 dBm, 310.7 MHz signal into A15J801.

   c. If a flat line is displayed within 2 dB of the reference level, but the External Mixer Amplitude Adjustment fails, troubleshoot the A15 RF Assembly.

A7 LO Distribution Amplifier

NOTE   YTO unlock errors may occur if the power delivered to the A15U100
sampler is less than –9.5 dBm. Frequency response will be degraded in
both internal and external mixing modes if the output power is low or
unlevelled.

CAUTION   Connecting or disconnecting the A7 bias with the 8562E/EC LINE
switch on will destroy the A7 assembly. Always press **LINE** to turn the
8562E/EC off before removing or reinstalling W12 to either the A7 or
A14J10.

NOTE   `Err 334` may be displayed if the LO OUTPUT connector on the front
panel is not properly terminated into a 50Ω termination.

Figure 12-2   **A14J10, Solder Side of A14 (Ignore Pin Numbers on Mating
Connector)**
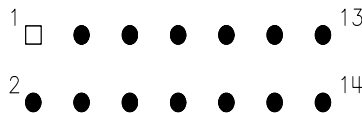
sm632e

1. Press **LINE** to turn the spectrum analyzer off. Disconnect W12 from
   A14J10.

2. Connect a jumper between A14J10 pin 5 and A14J19 pin 6. Connect
   a jumper between A14J18 pin 13 and A14J18 pin 1. See Figure 12-2
   on page 604.

3. Connect the positive lead of a DVM to A14J18 pin 14 and the
   negative lead to A14J18 pin 6.

4. Press **LINE** to turn the spectrum analyzer on.

5. The voltage measured on the DVM should be more negative than
   –9.4 Vdc.

6. Move the jumper from A14J18 pin 1 to A14J18 pin 2. The voltage
   measured on the DVM should be more positive than +12.3 Vdc.

7. If the voltages do not meet the limits listed in steps 5 and 6,
   troubleshoot the A14 frequency control assembly.

8. Connect the positive DVM lead to A14J10 pin 1.

9. The measured voltage should be approximately +5 Vdc. If the voltage is not +5 Vdc, troubleshoot the A14 frequency control assembly.

10. Connect the positive lead of a DVM to A14J18 pin 15. The voltage should measure within ±10 mV of the Gate Bias voltage listed on the A7 label.

11. If this voltage is not within the correct range, refer to "8. LO Distribution Amplifier Adjustment" on page 90.

12. If the voltage varies between 0 Vdc and −2 Vdc, adjust the Gate Bias for a DVM reading within ±10 mV of the Gate Bias voltage listed on the A7 label. If the voltage does not vary between 0 Vdc and −2 Vdc, troubleshoot the A14 Frequency Control Assembly.

13. Disconnect the jumper from A14J19 to A14J10. Press **LINE** to turn the spectrum analyzer off. Reconnect W12 to A14J10. Press **LINE** to turn the spectrum analyzer on.

14. If the DVM reading changes significantly, the A7 is probably defective.

A8 Low Band Mixer

1. Connect the 8562E/EC CAL OUTPUT to the INPUT 50Ω connector.

2. Set the 8562E/EC as follows:

    Center frequency .... 300 MHz
    Span .... 0 Hz
    Input attenuation .... 10 dB

3. Check to see that A8 is receiving the –5 V and –4 V supply voltages from A14 via W12.

4. Using another spectrum analyzer, check for approximately –21 dBm (300 MHz) at the input of A8. (This level can easily be measured at the output of FL1 by disconnecting W45 from FL1.)

5. If the level at the input of A8 is less than –25 dBm, suspect FL1 low-pass filter, A10 RYTHM, or A9 input attenuator. Refer to power levels shown on Figure 12-8 on page 627, 8562E RF Section Troubleshooting Block Diagram.

6. Check for approximately –30 dBm (3.9107 GHz) at the output of A8. (This level can easily be measured at the output of FL2 by disconnecting W57 from FL2.)

7. If the level at the output of A8 is less than –35 dBm, suspect A8 low band mixer or FL2 low-pass filter.

A9 Input Attenuator

1. Perform the "Input Attenuator Switching Uncertainty" performance test in Chapter 2, "Using Performance Tests," of the *8560 E-Series Spectrum Analyzer Calibration Guide*.

2. If there is a step-to-step error of approximately 10 dB or more, continue with step 3.

3. On the spectrum analyzer, press **AMPLITUDE**, and **ATTEN AUTO MAN** until MAN is highlighted.

4. Step the input attenuator from 0 dB to 70 dB. A "click" should be heard at each step. The absence of a click indicates faulty attenuator drive circuitry. It will be necessary to use the DATA keys to enter an input attenuator setting of 0 dB (the step key will not allow selecting 0 dB input attenuation).

5. Monitor the pins of A14U420 with a logic probe or DVM while setting the input attenuator to the values listed in Table 12-3 on page 608.

6. If one or more logic levels listed in the tables is incorrect, disconnect W11 from A14J6 and repeat step 4 checking only pins 3, 5, 11, and 13 of A14U420. Pins 4, 6, 10, and 12 should all read low TTL levels.

7. If one or more logic levels listed in the tables is incorrect with W11 disconnected, troubleshoot the A14 frequency control assembly.

8. If all logic levels are correct, the A9 input attenuator is probably defective.

NOTE

The logic levels listed in Table 12-3 on page 608 show the default ac usage (pin 5 low, pin 6 high). DC usage (pin 5 high, pin 6 low) is not shown.

Table 12-3   **8562E/EC Attenuator Control Truth Table**

8562E/EC	A14U420 Pin Number							
ATTEN Setting	3	4	5	6	10	11	12	13
(dB)	20 dB	20 dB	DC	AC	40 dB	40 dB	10 dB	10 dB
0	high	low	low	high	low	high	low	high
10	high	low	low	high	low	high	high	low
20	low	high	low	high	low	high	low	high
30	low	high	low	high	low	high	high	low
40	high	low	low	high	high	low	low	high
50	high	low	low	high	high	low	high	low
60	low	high	low	high	high	low	low	high
70	low	high	low	high	high	low	high	low

A13 Second Converter

CAUTION
The A13 assembly is extremely sensitive to Electrostatic Discharge (ESD). For further information regarding electrostatic cautions, refer to "Electrostatic Discharge" on page 32.

1. Connect the 8562E/EC CAL OUTPUT to the INPUT 50Ω connector.

2. Set the 8562E/EC to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Input attenuation .... 10 dB

3. Disconnect W35 (coax 92) from A13J2.

4. Connect a test cable from A13J2 to the input of another spectrum analyzer.

5. Tune the other spectrum analyzer to 310.7 MHz. The signal displayed on the other spectrum analyzer should be approximately −38 dBm.

6. Connect the positive lead of a DVM to A14J19 pin 15.

7. Set the 8562E/EC **CENTER FREQ** to 3 GHz.

8. The DVM should measure between −2.0 Vdc and −3.5 V dc. If the voltage measures outside this limit, perform the following steps:

   a. Set the spectrum analyzer **LINE** switch OFF, disconnect W13 from A14J12, and set the **LINE** switch ON.

   b. Wait for the power-on sequence to finish and then set the spectrum analyzer settings to the following:

      Center frequency .... 3 GHz
      Span .... 0 Hz

   c. If the DVM measures −15 Vdc ±0.2 V, the A13 second converter is probably defective. If the DVM measures outside this limit, the A14 frequency control assembly is probably defective.

9. Set the **LINE** switch OFF and reconnect W13 to A14J12.

10. Remove the test cable from A13J2 and reconnect W35 to A13J2.

11. Disconnect W33 (coax 81) from A13J4 and connect W33 through a test cable to the input of another spectrum analyzer.

12. Tune the other spectrum analyzer to a center frequency of 600 MHz.

13. If a 600 MHz signal is not present, or its amplitude is less than −5 dBm, the fault is probably on the A15 RF assembly.

14. Reconnect W33 to A13J4.

15. Connect the positive lead of a DVM to A14J19 pin 15 and the negative lead to A14J19 pin 6.

16. If the DVM does not measure between +14.0 Vdc and +15.0 Vdc, perform the following:

   a. Press **LINE** to turn spectrum analyzer off and disconnect W13 from A14J12.

   b. Press **LINE** to turn spectrum analyzer on and set the spectrum analyzer to the following settings:

      Center frequency .... 300 MHz
      Span .... 10 MHz

   c. The voltage should measure +15 Vdc ±0.2 V. If the voltage measures outside this limit, the A14 frequency control assembly is probably defective.

   d. Press **LINE** to turn spectrum analyzer off. Reconnect W13 to A14J12, and press **LINE** to turn spectrum analyzer on. Set the 8562E/EC to the following settings:

      Center frequency .... 300 MHz
      Span .... 0 Hz

17. Move the positive lead of a DVM to A14J19 pin 1. The voltage should measure between −150 mVdc and −800 mVdc. If the voltage measures outside this limit, the A13 Second Converter is probably defective.

A14 Frequency Control Assembly

The block diagrams for the A14 and A15 assemblies are located in Chapter 11 , "Synthesizer Section."

LODA Drive

Refer to function block Z on the A14 Frequency Control Schematic Diagram (sheet 3 of 5) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

1. Set the 8562E/EC to the following settings:

   Center frequency .... 300 MHz
   Span .... 2 MHz

2. On the 8562E/EC, press **SGL SWP** and measure the signal power at the output of A7 (see item **(1)** of Figure 12-3 on page 612).

3. If the output power is low, the output voltage of A14U429B at A14J18 pin 14 (item **(2)** of Figure 12-3 on page 612) should be above 0 V. If the output power is high, the voltage should be more negative than −10 V. If the voltages do not measure as indicated, check that the voltages at A14J18 pins 5 and 13, item **(4)**, are consistent with the operational amplifier output.

If a TAM is available, use Manual Probe Troubleshooting to make measurements on A14J18 pins 5, 13, and 14. These voltages are referred to as AMP CNTL, LO SENSE, and PIN ATTEN respectively.

4. If the voltages measure as indicated in step 3, measure the A11 YTO output. (See item **(3)** of Figure 12-3 on page 612.)

5. If all measurements are within limits, refer to "A7 LO Distribution Amplifier" in this chapter.

Figure 12-3   A7 First LO Distribution Amplifier Drive


```
A7 1ST LO DISTRIBUTION
AMPLIFIER
```

A11
YTO

+2 TO +13 dBm

J1

③

J4   SAMPLER OUT −9 TO −2 dBm
J3   HI BAND +13 TO +16 dBm*
J2   LO BAND +13 TO +16 dBm*
J5   1ST LO OUT 14.5 TO 18.5 dBm
     (A7J3 FOR HP 8561E)

①

SCHEMATIC
3 OF 5

```
P/O A14 FREQUENCY
CONTROL
```

②

REF VOLTAGE
−.1 TO −.25 VOLT

5 +
   U429B   7
6 −

④

AS V INCREASES
A7 OUTPUT INCREASES

* ONLY ONE 1ST MIXER OUT
  (A7J2) FOR 8561E.
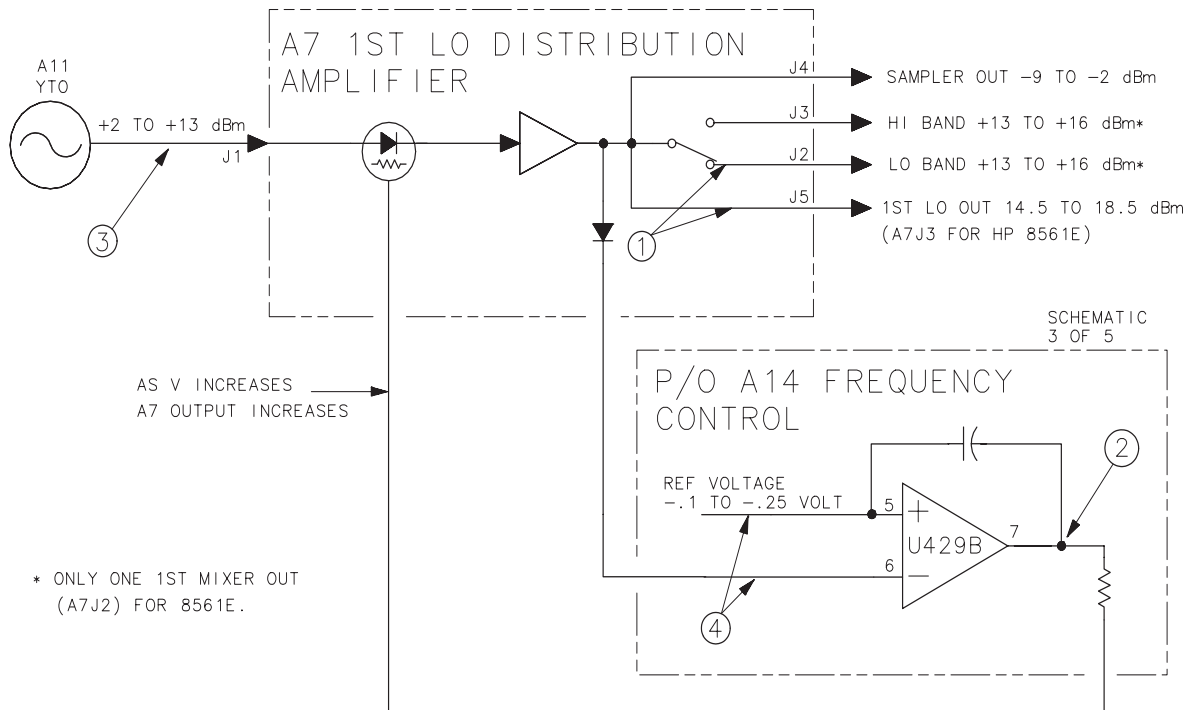
sm66e

Control Latch for Band-Switch Driver

Refer to function block P on A14 Frequency Control Schematic Diagram
(sheet 3 of 5) in the *8560 E-Series Spectrum Analyzer Component Level
Information*.

1. Connect the positive lead of a DVM to A14U417 pin 14 and the
    negative lead to A14J18 pin 6.

2. Set the 8562E/EC to the following settings:

    Center frequency .... 300 MHz
    Span .... 0 Hz

3. The voltage should measure approximately 0 Vdc (TTL low).

4. Set the 8562E/EC center frequency to 3 GHz.

5. The voltage should measure approximately +5 Vdc (TTL high).

YTF Driver Circuit

The YTF driver circuitry consists of the Sweep + Tune Multiplier, FAV (Frequency Analog Voltage) Generator, YTF Gain and Offset, and YTF Drive. Refer to function blocks Q, R, S, and T on A14 Frequency Control Schematic Diagram (sheet 3 of 5). The FAV Generator generates the 0.5 V/GHz signal. The YTF driver circuitry can be half-split by checking the rear panel 0.5 V/GHz output.

NOTE   The rear-panel output changes according to the external-mixer mode selected. The preselected external-mixer mode must not be selected while executing this procedure.

The Sweep + Tune Multiplier takes tune information (YTO start frequency) and sweep (based on LO span) and multiplies it so that it is correct for the appropriate YTF band.

C31 of the FAV Generator holds the YTF steady during retraces between multiband sweeps. Switch U415C and R94 provide the YTF de-hysteresis pulse. A de-hysteresis pulse is activated at the end of spans greater than 1 MHz. In high band, amplifier U402A provides an offset voltage to account for the 310.7 MHz offset (U415A open) between the desired harmonic of the YTO frequency and the center frequency. In low band, switch U415A is closed to account for the 3.9107 GHz first IF offset between the YTO frequency and the center frequency. This signal is 0.5 V/GHz of tuned frequency and is available at the rear panel.

1. On the 8562E/EC, press **PRESET**, and set the controls to the following settings:

    Start frequency .... 0 Hz
    Stop frequency .... 13.2 GHz

2. On the 8562E/EC, press **AUX CTRL**, **REAR PANEL**, and **.5 V/GHz (FAV)**.

3. Monitor the signal from the rear-panel LO SWP | FAV OUTPUT connector with an oscilloscope. The waveform should resemble Figure 12-4 on page 614.

4. Set the spectrum analyzer controls as follows:

    Start frequency .... 8 GHz
    Stop frequency .... 10 GHz

5. Monitor A14J15 pin 1 with an oscilloscope. The waveform should resemble Figure 12-5 on page 615.

6. If the ramp is not correct, confirm the operation of the Main Coil Tune DAC and Sweep Generator. Refer to "Unlocked YTO PLL" on page 558 steps 36 through 40 and "Sweep Generator Circuit" on page 585.

7. Set the 8562E/EC to the following settings:

    Center frequency .... 5 GHz
    Span .... 0 Hz

8. Monitor A14J15 pin 3 with a DVM. For a center frequency of 5 GHz, the voltage should measure −1.33 Vdc ±0.2 Vdc. Use the following formula to calculate the voltage:

$$V_{(J15 \text{ pin } 3)} = \frac{-0.25\,\text{V}}{\text{GHz}}(\text{freq in GHz}) - 0.078\,\text{V}$$

Figure 12-4   8562E/EC Rear-Panel LO SWP Output
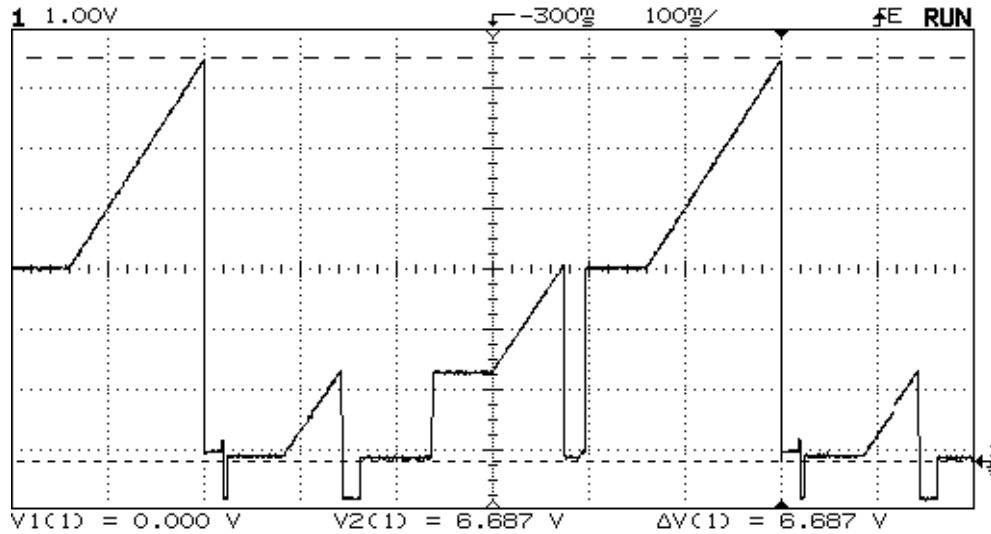
Figure 12-5   8562E/EC Signal at A14J15 Pin 1
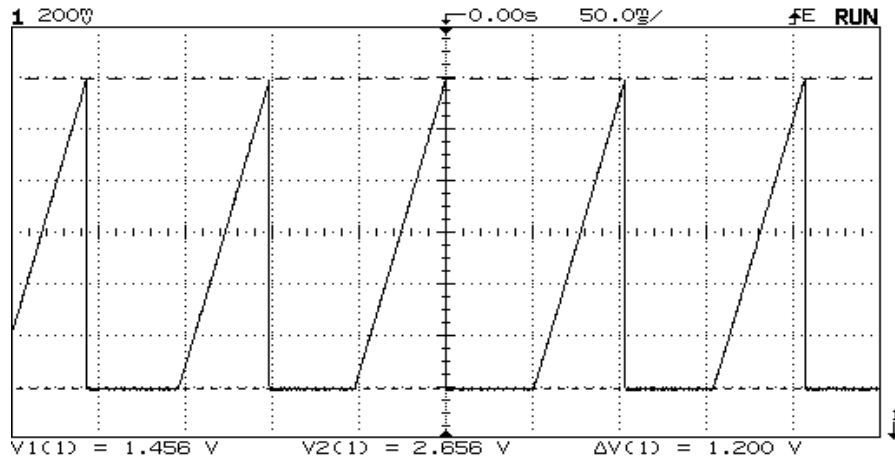
9. Check the voltage at A14J15 pin 3 with the spectrum analyzer center frequency set to the frequencies listed in Figure 12-4 on page 615. The following table lists the voltage that should be measured at A14J15 pin 3, the settings for the three switches (U416 in function block Q), and the gain through the Sweep + Tune Multiplier.

Table 12-4   Sweep + Tune Multiplier Values

N[†]	Center Frequency	A14J15 Pin 3 (V dc)	U416A	U416B	U416C	Gain*
1	5 GHz	−1.33	Open	Closed	Closed	× −0.208
2	10 GHz	−2.58	Open	Closed	Open	× −0.417
* Measured from A14J15 pin 1 to A14J15 pin 3.						
† N is the harmonic mixing mode.						

10. Move the WR PROT/WR ENA jumper on the A2 Controller assembly to the WR ENA position.

11. Set the 8562E/EC to the following settings:

Center frequency .... 5 GHz
Span .... 0 Hz

12. On the 8562E/EC, press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **PRESEL ADJ**, and **PRESEL OFFSET**.

13. Connect a DVM to A14J16 pin 13.

14. Set the DAC to values from 0 to 255 to yield DVM readings from 0 V to −10 V respectively.

15. Move the jumper on A14J14 from the NORM to the OPT position.

16. Connect the DVM to A14J16 pin 1.

17. Press **PRESEL SLOPE**.

18. Set the DAC to values from 0 to 255 to yield DVM readings from 0 V to +10 V respectively.

19. Move the jumper on A14J14 from the OPT to the NORM position.

20. On the 8562E/EC, press **CAL** and **REALIGN LO &IF**.

21. Connect the DVM to A14J16 pin 3.

22. Change the center frequency in 1 GHz steps and confirm that the voltage changes by 266 mV/GHz.

23. Move the WR PROT/WR ENA jumper on the A2 Controller assembly to the WR PROT position.

A15 RF Assembly

NOTE The block diagrams for the A14 and A15 assemblies are located in Chapter 11 , "Synthesizer Section."

Confirming a Faulty Third Converter

1. Perform the "IF Input Amplitude Accuracy" performance test in the *8560 E-Series Spectrum Analyzer Calibration Guide*. This exercises most of the third converter.

2. If the performance test fails, perform the "15. External Mixer Amplitude Adjustment (Non-Option 327)" on page 111.

3. If adjustment cannot be made, disconnect W35 (coax 92) from A15J801.

4. On the 8562E/EC, press **PRESET** and set the controls to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz

5. Connect a signal generator to A15J801.

6. Set the signal generator to the following settings:

   Frequency .... 310.7 MHz CW
   Power .... −28 dBm

7. If a flat line is displayed within 2 dB of the reference level and the performance test passed, troubleshoot microcircuits A7, A8, A9, and A13.

8. If a flat line is displayed within 2 dB of the reference level and the performance test failed, troubleshoot the A15 RF assembly.

9. Disconnect the signal generator from A15J801 and reconnect W35.

Confirming Third Converter Output

1. Connect the 8562E/EC CAL OUTPUT to the INPUT 50Ω connector.

2. Set the 8562E/EC to the following settings:

   Center frequency .... 300 MHz
   Span .... 0 Hz
   Input attenuation .... 10 dB

3. Press **SGL SWP**, **CAL**, **IF ADJ OFF**.

4. Disconnect W29 (coax 7) from A15J601.

5. Connect a test cable from A15J601 to the input of another spectrum analyzer.

6. Tune the other spectrum analyzer to 10.7 MHz. The signal displayed on the other spectrum analyzer should be approximately −15 dBm.

7. Remove the test cable from A15J601 and reconnect W29 to A15J601.

Third Converter

Refer to function blocks A, B, C, D, and E on A15 RF Section Schematic Diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The 3rd converter consists of the 2nd IF distribution, 2nd IF amplifier, double balanced mixer, 10.7 MHz bandpass filter, and flatness compensation amplifier. The 2nd IF distribution switches between two possible 2nd IF inputs: the internally generated 2nd IF, or the external mixing IF INPUT. A variable dc bias can be applied to the IF INPUT for external mixers which require such bias. The selected input is fed to the 2nd IF Amplifier. This amplifier consists of four stages of gain and two stages of SAW filters for image frequency rejection.

The flatness compensation amplifier consists of two fixed-gain stages and two stages of variable gain. This provides an overall adjustable gain of 4 dB to 30 dB. This gain is adjusted during an spectrum analyzer sweep to compensate for front-end conversion-loss versus frequency. Perform the following steps to test the amplifier gain:

The 10.7 MHz bandpass filter provides a broadband termination to the mixer while filtering out unwanted mixer products.

1. On the 8562E/EC, press **AUX CTRL**, then **INTERNAL MIXER**.

2. In the 2nd IF distribution (function block A), diode CR802 should be forward biased and diode CR801 should be reverse biased.

3. Disconnect W35 (coax 92) and connect a signal source to A15J801. Set the source to the following settings:

> Frequency .... 310.7 MHz
> Amplitude .... −30 dBm

CAUTION

For troubleshooting, it is recommended that you use an active probe, such as an 85024A, and another spectrum analyzer. If an 1120A active probe is being used with a spectrum analyzer having dc coupled inputs, such as the 8566A/B, 8569A/B and the 8562A/B, either set the active probe for an ac-coupled output, or use a dc-blocking capacitor between the active probe and the spectrum analyzer input. Failure to do this can result in damage to the spectrum analyzer or the probe.

4. Use an active probe with another spectrum analyzer to measure the signal at A15TP601 (function block C). The signal should measure −17 dBm ±4 dB confirming the operation of the 2nd IF Amplifier.

5. Use an active probe with another spectrum analyzer to measure the 300 MHz signal into the LO port of the third mixer. The signal should measure at least +20 dBm.

6. Measure the power of the mixer 10.7 MHz IF output. The signal level should be approximately −22 dBm.

7. Move the WR PROT/WR ENA jumper on the A2 controller assembly to the WR ENA position.

8. While measuring the 10.7 MHz IF output signal at the mixer, adjust the signal source until the level of the 10.7 MHz IF is −40 dBm.

9. On the 8562E/EC, press **SGL SWP**, **CAL**, **IF ADJ OFF**, **MORE 1 OF 2**, and **FLATNESS**. Increase the gain of the flatness compensation amplifiers to maximum by entering 0 using the data keys. This sets the gains in the flatness compensation amplifiers to their maximum values.

10. Connect the other spectrum analyzer to A15J601 and measure the 10.7 MHz IF signal level. The signal should measure greater than −10 dBm. If the signal level is incorrect, continue with step 13.

11. Enter 4095 into the 8562E/EC Flatness Data. The signal level at A15J601 should measure less than −36 dBm. This sets the gain of flatness compensation amplifiers to a minimum. If the signal level is incorrect, continue with step 13.

12. Check that the gain stages are properly biased and functioning.

13. Check the attenuator stages and flatness compensation control circuitry.

    a. For minimum gain (flatness data equals 4095), RF GAIN (A15U909 pin 10) should be at –1.6 Vdc and the current through each section as measured across R667 or R668 should be about 7 mA.

    b. For maximum gain (flatness data equals 0), RF GAIN (A15U909 pin 10) should be at approximately 0 Vdc and the current through each attenuator section should be close to 0 mA.

CAUTION   As long as the flatness data just entered is not stored, the previously-stored flatness data will be present after the power is cycled.

14. Move the A2 controller assembly WR PROT/WR ENA jumper to the WR PROT position.

15. Reconnect the cable to A15J801.

Flatness Compensation Control

Refer to function block G on A15 RF Section Schematic Diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The Flatness Compensation Control consists of a buffer amp (U909C) and two identical voltage-to-current converters (U909B and U909D). The thermistor RT901 in the buffer amp provides temperature compensation for the PIN diodes in the gain stages and the SAW filters. The gain of the Flatness Compensation Amplifiers is driven to a minimum by the REDIR line going low during Automatic IF Adjustment.

Control Latches

Refer to function block H on A15 RF Section Schematic Diagram (sheet 1 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

The control latches control the PIN Switch Drivers illustrated in Function Block I.

1. Connect the positive lead of a DVM to A15J901 pin 15 (HEXTMIX). Connect the negative lead to A15J901 pin 6. The measured signal controls the switching between internal and external IF signals.

2. On the 8562E/EC, press **AUX CTRL** and **EXTERNAL MIXER**. The voltage on the DVM should measure approximately +5 Vdc (TTL high).

3. On the 8562E/EC, press **AUX CTRL** and **INTERNAL MIXER**. The voltage on the DVM should measure approximately 0 Vdc (TTL low).

4. Connect the positive lead of a DVM to A15J901 pin 13 (LSID). The signal measured turns on the SIG ID oscillator.

5. On the 8562E/EC, press **SIG ID ON** (if present), **SGL SWP**.

6. Subsequent pushes of **SGL SWP** should cause the signal measured on the DVM to toggle between TTL high and low levels.

7. Connect an oscilloscope probe to A15U902 pin 7 (LRDIR) and the probe ground lead to A15J901 pin 6. The signal measured controls the flatness compensation circuit.

8. On the 8562E/EC, press **PRESET** and set the **SPAN** to 1 MHz.

9. Set the oscilloscope for the following settings:

   Amplitude scale .... 2 V/div
   Sweep time .... 20 ms/div

10. The waveform should be at a TTL high during part of the retrace period and a TTL low during the sweep (about 50 ms).

SIG ID Oscillator (Option 008)

Refer to function block F on A15 RF Section Schematic Diagram (sheet 4 of 4) in the *8560 E-Series Spectrum Analyzer Component Level Information*.

SIG ID is available only with Option 008. The SIG ID Oscillator provides a shifted third LO (approximately 298 MHz) to distinguish true signals from false signals (such as image or multiple responses). When the 8562E/EC is set to **SIG ID ON**, the SIG ID Oscillator turns on during alternate sweeps.

1. Set the 8562E/EC to the following settings:

   Trigger .... single sweep
   SIG ID .... on

2. Use an active probe with another spectrum analyzer to measure the signal level at A15X602.

3. On the 8562E/EC, press **SGL SWP**. With each press of **SGL SWP**, the analyzer alternates between the following two states:

   State 1:

   A15J901 pin 13 (LSID)   TTL low

   SIG ID Oscillator   ON

   Signal at A15X602   298 MHz ±50 kHz (at least +1 dBm)

State 2:

A15J901 pin 13 (LSID)	TTL high
SIG ID Oscillator	OFF
3rd LO Driver Amplifier	Provides LO for Double Balanced Mixer

4. With the SIG ID Oscillator on, measure the frequency at A15X602 with a frequency counter and an active probe.

5. On the 8562E/EC, press **SGL SWP** until A15J901 pin 13 is at TTL low. Diodes CR603 and CR605 should be forward biased and CR604 should be reverse biased (approximately 6 Vdc reverse bias). Diodes CR501 and CR502 should be forward-biased, disabling the 3rd LO Driver Amplifier.

6. The voltage at the R622/R623 node should measure approximately −5 Vdc, biasing Q604 on.

7. If oscillator bias voltages are correct, place a 100 Ω resistor across SAWR U602 input and output. If the SAWR has failed, this will provide the equivalent loss of a correctly functioning SAWR, and the circuit will begin to oscillate.

10 MHz Reference

The spectrum analyzer 10 MHz reference consists of 10 MHz OCXO (Option 103: TCXO) with associated TTL level generator and distribution circuitry. The OCXO (or TCXO) and TTL level generator are turned off when an external 10 MHz reference is used. Also, with the analyzer set to EXTernal frequency reference, U304A output (low) forces the output of U304D to stay high. This allows U304B to control the outputs of U303B, U304C, and U303D. In INTernal frequency reference, U304D controls the outputs of these three NAND gates, and the output of U304B is held high.

Check the 10 MHz reference by performing the following steps:

1. Set the 8562E/EC 10 MHz reference to internal by pressing **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.

2. Use a spectrum analyzer to confirm the presence of a 10 MHz signal at the following test points:

A15J303	≥−10 dBm
A15J304	≥−10 dBm
A15J301	≥−2 dBm

3. Check for a 1.3 Vp-p waveform at A15J302 using an oscilloscope (see Figure 12-6 on page 624).

4. Check that the signal at A15J301 is 10 MHz ±40 Hz (with Option 103 TCXO reference) using a frequency counter. If necessary, perform the appropriate 10 MHz reference adjustment.

5. If there is no problem with INTernal 10 MHz reference operation, check EXTernal 10 MHz reference operation as follows.

6. Set the 8562E/EC 10 MHz reference to external by pressing **10 MHz EXT**.

7. Connect a 10 MHz, –2 dBm, signal to the rear-panel 10 MHz REF IN/OUT connector.

8. Check the signals at A15J301, A15J302, A15J303, and A15J304 according to the procedure in steps 2 through 4.

9. If the signals are correct in EXTernal operation, but not in INTernal operation, the problem lies in A21 OCXO (or Option 103 TCXO), its voltage reference, or the TTL level generator. Check these areas as follows:

   a. On the spectrum analyzer, press **10 MHz INT**.

   b. Check U305 pin 3 for approximately +12 Vdc (Option 103 only).

   c. Check for a 10 MHz sine wave greater than or equal to 1 V p-p at J305 (standard 8562E/EC), or at U302 pin 3 with an oscilloscope (Option 103).

10. If the signal at U304 pin 13 is correct (see Figure 12-7 on page 624), but there is a problem with the signals at A15J301, A15J302, A15J303, or A15J304, suspect U303 or U304 in the 10 MHz Distribution circuitry.

Figure 12-6   10 MHz Reference at A15J302
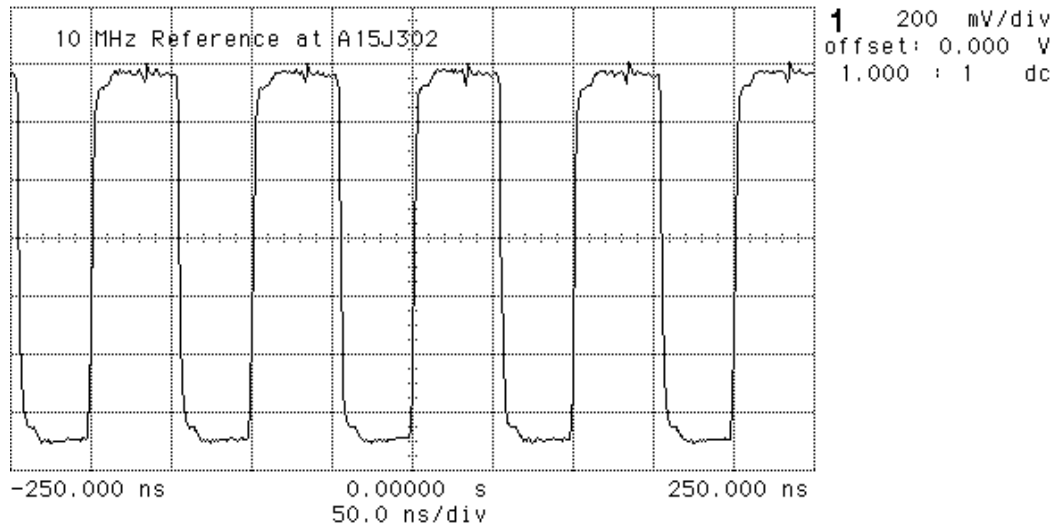
Figure 12-7   10 MHz TTL Reference at U304 Pin 13
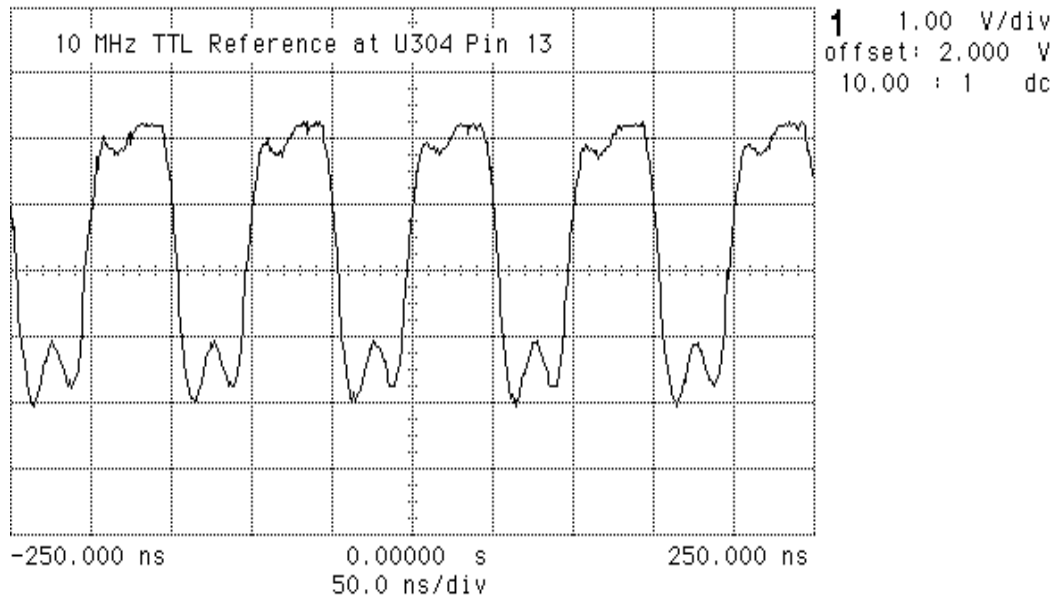
Table 12-5 on page 625 lists the RF Section mnemonics shown in Figure 12-8 on page 627, and provides a brief description of each.

Table 12-5 **RF Section Mnemonic Table**

Mnemonic	Description
TUNE+, TUNE–	YTF Tune Signal (SYTF or RYTHM)
HTR+, HTR–	YTF Heater Power
MAIN COIL+, MAIN COIL–	YTO Main Coil Tune Signal
FM+, FM–	YTO FM Coil Tune Signal
LO SENSE	LO Amplitude Sense Voltage
LEVEL ADJUST	LO Amplitude Adjustment Voltage (PIN ATTEN)
GATE BIAS	LODA Gate Bias Voltage
HEXTMIXB	External Mixer: +12V=EXT MIX −12V=INT MIX
HSIGIDOFFA	SIG ID Oscillator ON: +12V=SIG ID OFF −8V=SIG ID ON
PIN SW	PIN Diode Switch Control (SYTF or RYTHM LO Band/HI Band)
PIN DIODE SWITCH	PIN Diode Switch Control For 2ND Conv. IF Output
MIXER BIAS	Detected Voltage on 2ND Converter Mixer Diode
RFGAIN	Voltage to Control Gain of Flatness Comp. Amps.
RFGAIN1 and RFGAIN2	Currents to Drive PIN Diodes in Flatness Comp. Amps.
L10dB A, L40dB B, L20dBC, LDC D	Control Lines to Set Attenuator Sections A, B, C, and D to Attenuate Position (Active Low)*
10dB A, 40dB B, 20dB C, LAC D	Control Lines to Set Attenuator Sections A, B, C, and D to Attenuate Position (Active High)*
* Section D of the input attenuator is a dc blocking capacitor which is switched in or bypassed by the LDC D and LAC D control lines.	

HP 8562E AND 8562EC RF SECTION BLOCK DIAGRAM

FIGURE 12-8. HP 8562E/EC RF SECTION, TROUBLESHOOTING BLOCK DIAGRAM
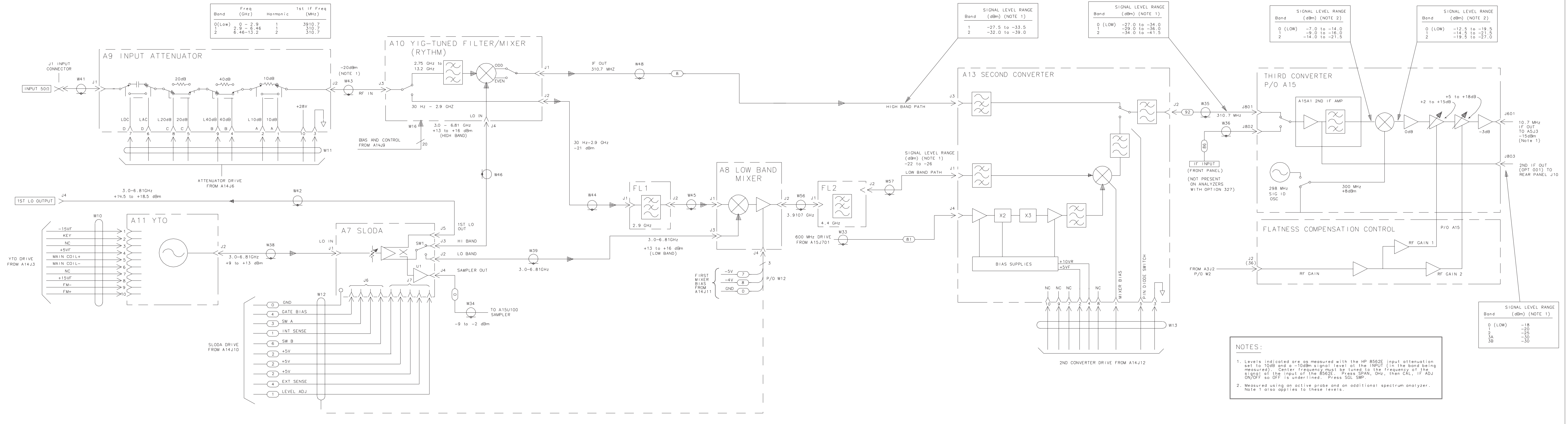
13 **Display/Power Supply Section**

Introduction

The Display/Power Supply chapter consists of the following sections:

WARNING

The A6 power supply in 8560 E-series and 8560 EC-series instruments, and the A6A1 high voltage assembly in 8560 E-series instruments, contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before servicing these assemblies. Failure to follow this precaution can represent a shock hazard which may result in personal injury.

The voltage potential at A6A1W3, in 8560 E-series instruments, is +9 kV. If the cable must be disconnected, always disconnect it at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument. See procedure 2 in Chapter 3.

Do not discharge the CRT second anode in 8560 E-series instruments directly to ground, with the A6A1 high voltage cable connected. This can damage the A17 CRT driver assembly. Always discharge through a high resistance, such as a high voltage probe.

Always use an isolation transformer when troubleshooting either the A6 power supply or the A6A1 HV module. When using an isolation transformer, connect a jumper between A6TP101 and A6TP301. This connects the circuit common to earth ground. Remove this jumper when the isolation transformer is not used.

LCD Display (8562EC)

The display section of 8562EC instruments contain the A17 display driver, the A17A1 inverter board, the A18 LCD (liquid crystal display), and the A6 power supply. The A6 power supply is explained in the power supply section which begins on page 590. Figure 13-1 on page 632 illustrates the LCD block diagram.

Figure 13-1   Simplified Section Block Diagram
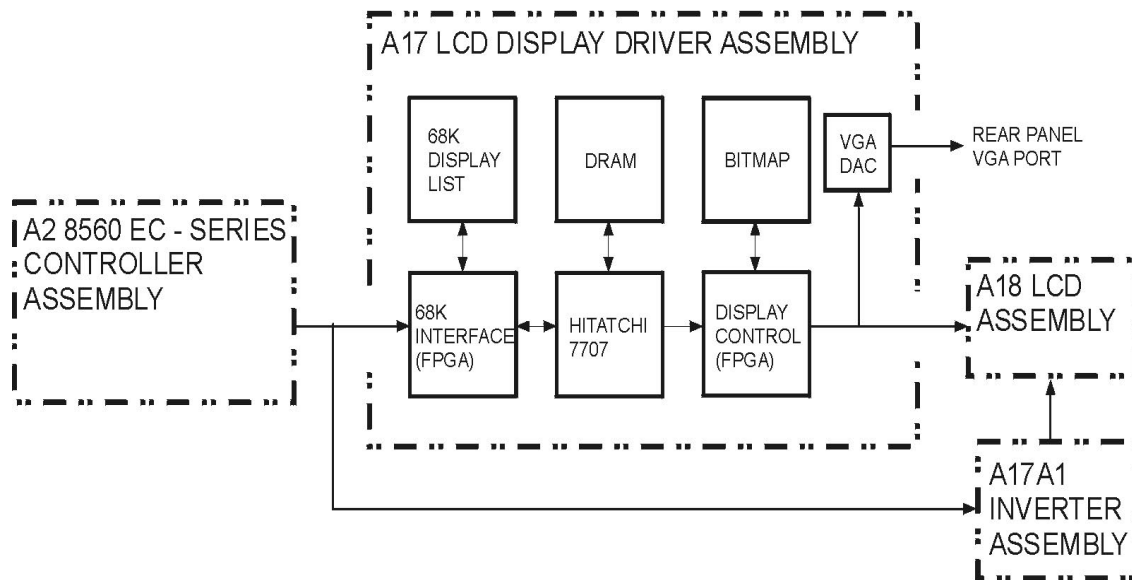
sj136c

Overview of A17 Display Driver Board

The A17 display driver board monitors the 8560 EC-series controller board, copies display instructions to local memory, creates a bitmap from the data, and generates the signals needed to drive the LCD display and a VGA monitor. The display driver consists of a Hitatchi 7707 processor, an FPGA, DRAM, SRAM, a filter circuit, and a video DAC.

The FPGA is connected to the address bus, data bus, and the display memory control signals on the controller board. The FPGA monitors the control signals and determines when the Hitatchi 7707 processor writes to display memory. When this occurs, the FPGA makes a duplicate of this information on the display driver board. The other main function of the FPGA is to provide the signals necessary to drive a TFT LCD display and a standard VGA monitor.

The processor reads display information received from the controller board, creates a bitmap, and copies the bitmap into SRAM. The FPGA outputs this information to the LCD and VGA displays. The DRAM is used by the processor to run its program. The filter circuit provides the clock signals that are needed to run the display driver board. The video DAC converts the digital color information that goes to the LCD to analog signals; these signal drive the RGB color lines on the VGA port.

Troubleshooting the LCD Display

There are no adjustments for intensity or focus of the LCD.

Blank Display

1. If the LED above the front-panel LINE switch is lit, most of the A6 power supply is functioning properly.

2. Carefully check the voltages on the front-panel PROBE POWER jack. Be careful to avoid shorting the pins together. See Figure 13-2 on page 633.

3. Check that the fan is operating. If the PROBE POWER voltages are correct, and the fan is turning, the A6 power supply is probably working properly.

4. If all of the power supply indicators along the outside edge of the A2 controller assembly are lit, the A6 power supply is probably working properly.

5. Connect a VGA monitor to the VGA port on the rear of the instrument. If the display is still blank, suspect the A2 controller, a loose cable, or the display driver.

6. If the LED is not lit, or the fan is not working, or the probe power voltages are not correct, or the power supply indicators on the edge of the A2 controller assembly are not working properly, proceed to the section on troubleshooting the power supply on page 653.

7. Open the left side of the instrument (see procedure A2 on page 166). Make voltage measurements at pins 1, 2, 3, 4, 5, 41, 42, 43, 44, and 45 on J8 of the A2 controller (see Figure 13-3 on page 635). These pins should measure 5V ±0.25V. If any of these measurements is out of tolerance suspect the A2 controller board or the power supply. If the voltages for these pins are correct, make the same measurements at the identical pins on J1 of the A17 display driver board. If these measurements are correct, suspect the A18 LCD assembly or the A17A1 inverter board. If these measurements are not correct, suspect the A17 LCD driver or A17A1 inverter board.

Figure 13-2   **Probe Power Socket**
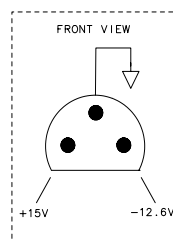
Dim Display

1. If the display is dim, suspect the backlights, which are inserted into the LCD assembly from the backlight assembly. Always replace both backlights at the same time. See the procedure for replacing the backlights, that is located in procedure 2A on page 175.

Troubleshooting using the VGA port

1. Connect a VGA monitor to the rear VGA port of the instrument (the VGA port is always active and requires no user interaction).

2. Observe the display.

   If the display on the VGA monitor is working correctly, the problem is probably caused by the LCD, or by a cable problem. Proceed to step 1 in "Troubleshooting using part substitution" on page 634.

   If the display on the VGA monitor shows the same symptom(s) you have seen on the instrument's LCD, the problem is probably caused by the A2 controller board, the display driver, or by a cable problem. Proceed to step 2 in "Troubleshooting using part substitution" on page 634.

Troubleshooting using part substitution

1. Disconnect the power cord, turn the instrument off, and open the left side. Ensure that W60, W61, W62, W63, and W64 are tight. Reconnect the power cord and check the instrument to see whether the problem is corrected. If not, proceed to step 2.

2. Disconnect the power cord and turn the instrument off. Replace W60, the ribbon cable that connects the A2 board to the display driver board. Reconnect the power cord and check the display to see whether the problem is corrected. If not, proceed to step 3.

3. Disconnect the power cord and turn the instrument off. Replace W61, the 10 MHz reference cable that connects the A2 board to the display driver board. Reconnect the power cord and check to see whether the problem is corrected. If not, proceed to step 4.

4. Disconnect the power cord and turn the instrument off. Remove and replace (see procedure 2A on page 152) the A17 display driver board. Reconnect the power cord and check the instrument to see whether the problem is corrected. If not, proceed to step 5.

5. Remove and replace (see procedure 5 on page 172) the A2 controller board. Check to see whether the problem is corrected. If not, proceed to step 6.

6. Disconnect the power cord and turn the instrument off. Remove and replace (see procedure 2A on page 152) the A18 LCD. Reconnect the power cord and check the instrument to see whether the problem is corrected.

Figure 13-3   **Location of +5V supply pins on J1 of A17 and J8 of A2**

GND SX	● 80	● 79	addrmsx2
addrmsx 3	● 78	● 77	GND SX
addrmsx 6	● 76	● 75	addrmsx 7
GND SX	● 74	● 73	addrmsx 10
addrmsx 11	● 72	● 71	GND SX
NC	● 70	● 69	NC
6ND SX	● 68	● 67	NC
NC	● 66	● 65	GND SX
NC	● 64	● 53	NC
GNDSX	● 62	● 61	DATAMSX 2
DATAMSX 3	● 60	● 59	GND SX
DATAMSX 6	● 58	● 57	DATAMSX 7
GND SX	● 56	● 55	DATAMSX 10
DATAMSX11	● 54	● 53	GNSD SX
DATAMSX 14	● 52	● 51	DATAMSX 15
GND SX	● 50	● 49	NC
_RESETMSX	● 48	● 47	GND SX
NC	● 46	● 45	+5V BKLTSX
+5VBKLTSX	● 44	● 43	+5VBKLTSX
+5VBLKTSX	● 42	● 41	+5VSX
addrmsx 1	● 40	● 39	GND SX
addrmsx 4	● 38	● 37	addrmsx 5
gnd sx	● 36	● 35	addrmsx 8
addrmsx 9	● 34	● 33	GND SX
ddrmsx 12	● 32	● 31	addrmsx 13
GND SX	● 30	● 29	NC
NC	● 28	● 27	GNDSX
NC	● 26	● 25	NC
GND SX	● 24	● 23	DATAMSX
DATAMSX 1	● 22	● 21	GND SX
DATAMSX 4	● 20	● 19	DATAMSX 5
GND SX	● 18	● 17	DATAMSX 8
DATAMSX 9	● 16	● 15	GND SX
DATAMSX 12	● 14	● 13	DATAMSX 13
GND SX	● 12	● 11	LMUX-INSX
EN1SX	● 10	● 9	GND SX
NC	● 8	● 7	NC
GND SX	● 6	● 5	+5VBKLTSX
+5V BKLTSX	● 4	● 3	+5VBKLTSX
+5V BKLTSX	● 2	● 1	+5VSX

sj114c

Figure 13-3 shows A2J8 connections on 8560 EC-Series Instruments. Lines 2 –5 and 42 – 44 supply +5V to the two LCD backlights. Lines 1 and 41 supply +5V to the A17A1 Inverter board. Lines 1 – 6 and 41 – 44 are identical on A17J1.

CRT Display (8562E)

The CRT display section contains the A6 power supply, A6A1 HV module, A17 CRT driver, and A18 CRT. The A6 power supply and A6A1 HV module are explained in the section on the power supply which begins on page 590. Figure 13-4 on page 637 illustrates the section block diagram.

WARNING
The A6 power supply and A6A1 high voltage assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before servicing these assemblies. Failure to follow this precaution can represent a shock hazard which may result in personal injury.

The voltage potential at A6A1W3 is +9 kV. If the cable must be disconnected, always disconnect it at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument. See procedure 2 in Chapter 3.

Do not discharge the CRT second anode directly to ground, with the A6A1 high voltage cable connected. This can damage the A17 CRT driver assembly. Always discharge through a high resistance, such as a high voltage probe.

Always use an isolation transformer when troubleshooting either the A6 power supply or the A6A1 HV module. When using an isolation transformer, connect a jumper between A6TP101 and A6TP301. This connects the circuit common to earth ground. Remove this jumper when the isolation transformer is not used.

Figure 13-4 Power Supply and CRT Block Diagram
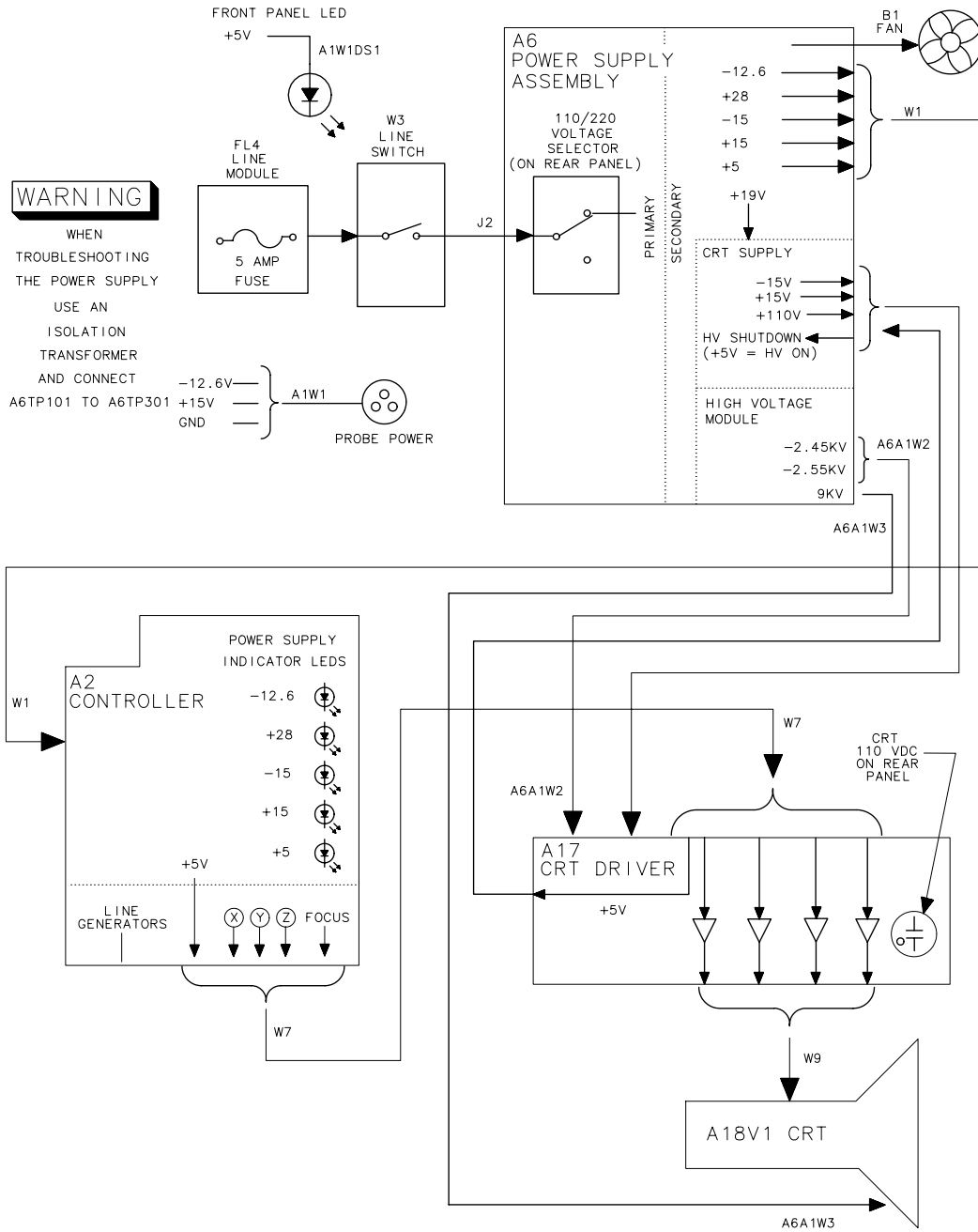
Troubleshooting Using the TAM

When using automatic fault isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 13-1 on page 638 to locate the manual procedure.

Table 13-2 on page 639 lists assembly test connectors associated with each manual probe troubleshooting test. Figure 13-5 on page 639 illustrates the location of A17 test connectors.

Table 13-1   **Automatic Fault Isolation References**

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check A2 Controller	Blanking Signal
Check All Power Supply Outputs	Dead Power Supply *(steps 1-5)*
Check Buck Regulator	Dead Power Supply *(steps 13-23)*
Check Buck Regulator Control Circuitry	Dead Power Supply *(steps 11-21)*
Check High-Voltage Supplies	High Voltage Supplies
Check Input Rectifier	Dead Power Supply *(steps 6-7)*
Check Intensity Adjustments	Intensity Problems *(steps 1-4)*
Check Kick Start/Bias Circuitry	Dead Power Supply *(steps 8-10)*
Check Low-Voltage Supplies	Low Voltage Supplies

Figure 13-5   A17 Test Connector
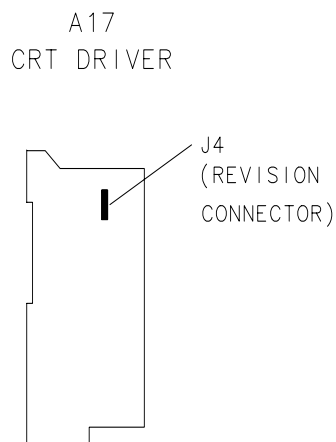
Table 13-2   TAM Tests versus Test Connectors

Connector	Manual Probe Troubleshooting Test	Measured Signal Lines
A17J4	Revision	MS5
	Constant current Source	MS1
	Intensity input	MS7
	Intensity offset	MS7
	Blanking control	MS8
A2J201	10 V reference test	MS4
	Switch drive test	MS3
	Buffered X &Y DAC outputs	MS2, MS7
	X line generator test	MS6
	Y line generator test	MS1
	Intensity offset output	MS8
A2J202	Revision	MS1
	X, Y, &Z output offset	MS3, MS4, MS7
	X output amplifier	MS7
	Y output amplifier	MS3
	Blanking test	MS4
	Focus DAC test	MS2

Blank Display (Using the TAM)

Use the following procedure if the instrument display is blank. This procedure substitutes a GPIB printer for the display.

1. Connect the printer to the 8562E spectrum analyzer and set the printer address to the value required by the TAM. This is usually 1.

2. All of the power-supply indicator LEDs along the edge of the A2 controller assembly should be lit.

3. The rear panel CRT +110 VDC ON indicator should also be lit.

4. Connect the TAM probe cable to A2J11.

5. Press **MODULE**, **SOFT KEY #3**, ▼, and **SOFT KEY #1**. (The top soft key is #1.)

6. The yellow LED next to A2J11 should blink approximately ten times. If the LED fails to blink correctly, troubleshoot the digital section of the A2 controller assembly.

7. Move the probe cable to A2J202. Press **SOFT KEY #1** and wait 5 seconds.

8. Press **SOFT KEY #4**. The results should be sent to the printer.

9. Move the probe cable to A2J201, press **SOFT KEY #1** and wait 5 seconds.

10. Press **SOFT KEY #4**. The results will be sent to the printer.

11. If a failure is indicated in any of these tests, the fault lies on the A2 controller assembly. to obtain more information:

    a. Press the down arrow key one less time than the test number. (For example, press it twice for the third test on the list.)

    b. Press **SOFT KEY #3**, then **SOFT KEY #4**, and when the printout is complete, **SOFT KEY #6**.

12. If no failures were indicated in testing the A2 controller, move the probe cable to A17J4.

13. Press **SOFT KEY #1** and wait 5 seconds.

14. Press **SOFT KEY #4**. The results will be sent to the printer.

15. If no failure is indicated in the printout, check the high-voltage supplies as described "High Voltage Supplies (8562E)" on page 657.

Blank Display

1. If the LED above the front panel LINE switch is lit, most of the A6 power supply is functioning properly.

2. Carefully check the voltages on the front panel PROBE POWER jack. Be careful to avoid shorting the pins together. See Figure 13-6 on page 641.

3. Check that the fan is operating. If the PROBE POWER voltages are correct, and the fan is turning, the A6 power supply is probably working properly.

4. If the CRT +110 VDC ON LED on the rear panel is lit, the high-voltage supplies should also be operating. (The high-voltage supplies will be turned off if the HV SHUT_DOWN line is low.) The A6 power supply feeds +5 V to the A2 controller through W1. The A2 assembly distributes this +5 V to the A17 CRT driver through W7. A17 sends +5 V back to A6 as the HV SHUT_DOWN signal on W8. As a result, A2, A17, W1, W7, and W8 must all be in place for the high-voltage supplies to operate.

5. If all of the power supply indicators along the outside edge of the A2 controller assembly are lit, the A6 power supply is probably working properly.

Figure 13-6   **Probe Power Socket**
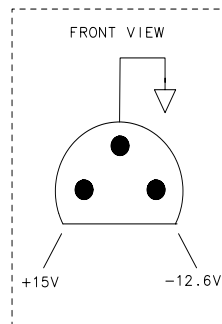
6. Press **FREQUENCY**, 1, **GHz**.

7. Allow the analyzer to warm up for at least 1 minute.

8. While observing the display, press **LINE** to turn the spectrum analyzer off. If a green flash appears on the display, the CRT is probably working properly; troubleshoot either the A2 controller or the A17 CRT driver.

9. If a flash does not appear on the display, the A2 controller, A6A1 HV module, A17 CRT driver, or A18V1 CRT might be at fault.

Blanking Signal

1. Connect an oscilloscope probe to A2J202 pin 3. Connect the oscilloscope ground lead to TP3. Set the oscilloscope to the following settings:

    Sweep time .... 2 ms/div
    Vertical scale .... 1 V/div

2. If a 4 Vp-p signal is not observed, the A2 controller assembly is faulty.

3. Repeat steps 1 and 2 with the oscilloscope probe on A2J202 pin 14.

4. Set the oscilloscope to the following settings:

    Sweep time 1µs/div
    Vertical scale .... 2 V/div

5. Connect the positive probe lead to A2J202 pin 15. This is the blanking output.

6. TTL-level pulses should be observed. If the signal is either always high or always low, the display will be blanked; suspect the A2 controller assembly.

7. If the signals on A2J202 pins 3, 14, and 15 are correct, troubleshoot the A17 CRT driver.

Display Distortion

The 8562E uses a vector display. The graticule lines, traces, and characters are composed of a series of straight lines ("vectors") placed end-to-end. If the vectors do not begin and end at the proper points, the display appears distorted, but in focus. Symptoms range from characters appearing elongated and graticule lines not meeting squarely, to an entirely unreadable display.

1. If the spectrum analyzer is in external frequency reference mode (an "X" is displayed along the left side of the display), ensure that an external 10 MHz reference is supplied. Otherwise the 16 MHz CPU clock will be off-frequency, causing distortion.

2. Use the CRT ADJ PATTERN to check for distortion. Press **CAL**, **MORE 1 OF 2**, and **CRT ADJ PATTERN**. If vector distortion (described above) occurs, perform "2. Display Adjustment (8562E)" on page 62 to test the function of the A2 controller assembly.

3. If there is distortion along with slight focus degradation, but the graticule lines meet (not necessarily squarely), the A17 CRT driver, CRT, DDD/TRACE ALIGN adjustments, or cable connections might be at fault.

4. If the A2 controller assembly is not part number 08563-60017, perform the "16 MHz PLL Adjustment" in Chapter 2. If the 16 MHz CPU clock is off-frequency, the display will be distorted.

5. Perform "2. Display Adjustment (8562E)" on page 62. Isolate the problem to either the X or Y axis by noting the behavior of the adjustments. If the line generator or fast zero-span portion of the adjustment fails, troubleshoot the A2 controller assembly.

6. If the adjustments do not remedy the problem, press **LINE** to turn the spectrum analyzer off and place the A17 CRT driver in the service position.

7. Distortion confined to one axis (vertical or horizontal only), indicates a faulty X or Y deflection amplifier on the A17 assembly. Use the alternate good deflection amplifier for obtaining typical voltages. (There is enough symmetry in a typical display that the voltages should be similar between these circuits.)

8. Monitor the waveforms at A17TP11 and A17TP14 (or TP12 and TP13). The 50 to 100 Vp-p ac component of the waveforms at the X and X (or Y and Y) outputs should be mirror images of each other. The dc average should be 55 V.

9. The appropriate POSN adjustment (A17R57 or A17R77) should change the dc component of both X and X (or Y and Y) outputs in opposite directions.

10. The appropriate GAIN adjustment (A17R55 or A17R75) should change the ac component in both outputs by the same amount.

11. If the display is a single dot, check the base of A17Q18 for −10.3 V ±0.3 V. Verify the signals at TP11, TP14, TP12, and TP13.

12. If signals are correct and cables to the CRT are good, suspect the CRT.

Focus Problems

Focus problems may be due to a defective A18V1 CRT, the A17 CRT driver (especially the grid level shifter section), or the A2 controller focus control circuitry. Focus problems may also be due to improper adjustments, improper connections, or absence of high voltage.

Although A17 grid level shifter (function block D) is the leading cause of A17 focus problems, function blocks C, E, F, and H generally have less effect on focus, but may cause poor focus that is a function of screen position, length of line, or intensity.

1. Connect the positive lead of a DVM to A2J202, pin 2. Connect the negative lead to A2J202 pin 6.

2. Use the knob to change the focus DAC value from 0 to 255.

3. If the DVM reads near 0 Vdc with the focus set to 0, and near −10 Vdc with the focus set to 255, the A2 focus control circuitry is working properly.

4. Perform "2. Display Adjustment (8562E)" on page 62. Note that A17R34 COARSE FOCUS has the greatest effect on focus. Adjustment A17R93 ASTIG and A17R92 DDD have a lesser effect, and A17R21 Z FOCUS, A17R26 X FOCUS and front panel adjustment (press **DISPLAY**, **MORE 1 OF 2**, **FOCUS**, and turn knob) have less effect on focus.

5. If the focus of some areas of the screen are worse than normal, continue with step 11. If no part of the screen can be brought to sharp focus, continue with step 6. (CRTs have some normal focus variation across their face.)

6. Turn off the analyzer and place A17 in the service position. Connect the ground lead of a high-voltage probe (34111A) to the chassis, and use it with a DVM to measure A17J7(10).

7. The nominal A17J7(10) voltage is −1600 Vdc, but the CRT will function if this voltage is within 200 V of −1600 Vdc.

8. Adjusting A17R34 COARSE FOCUS should vary the A17J7(10) voltage by 150 V. If these voltages are correct, suspect the CRT.

9. Check the A6A1 high voltage module cathode supply output at A17TP16 using a high voltage probe. If the cathode voltage is −2450 V ±250 V, check the focus grid level shifter.

10. If the cathode voltage is not correct, check the A6A1 high voltage module and its connections.

11. Connect an oscilloscope probe to A17TP9. This signal corrects the focus for the X position of the CRT beam, and for intensity level. It also provides the front panel focus adjusting voltage.

12. Press **DISPLAY**, **MORE 1 OF 2**, and **FOCUS**. While turning the front panel knob, verify the dc level of the signal at TP9 adjusts about 30 Vp-p.

13. Verify that the front panel intensity adjustment, when used with the A17R21 Z FOCUS, changes the peak-to-peak voltage at TP9 by 25 V. Access the intensity adjustment by pressing **DISPLAY**, **INTENSITY**, and turning the front panel knob.

14. Set front panel intensity to minimum. Set A17R21 Z FOCUS and A17R26 X FOCUS fully counterclockwise. Verify that the peak-to-peak voltage at TP9 is about 40 Vp-p (due to X-dynamic focus circuit).

15. If circuit operation seems correct, the A18V1 CRT is probably at fault.

Intensity Problems

Intensity problems, or absence of display, can be due to the A17
assembly intensity amplifier (function block A), intensity grid level
shifter (function block B), CRT (A18V1), interconnections, or lack of
proper supplies or inputs to A17.

1. On the 8562E spectrum analyzer, press **DISPLAY** and **INTENSITY**.

2. Rotate the front panel knob (RPG), and check that the intensity
   changes from dim, but readable, to bright.

3. If the intensity function does not function properly, troubleshoot the
   A2 controller assembly.

4. Perform the preliminary and Z-axis portions of "2. Display
   Adjustment (8562E)" on page 62. Verify that A17R11 CUTOFF
   functions properly. If A17R11 CUTOFF does not function properly,
   place the A17 CRT driver in the service position.

5. Verify that blanking pulses are present at A17TP2 using an
   oscilloscope. The pulses should be normal TTL levels, approximately
   1 μs wide and 4 or 7 μs apart. If the blanking pulses are not correct,
   check the BLANKING output of the A2 controller assembly and
   cable W7.

6. If blanking pulses are present, check A17TP10 with the oscilloscope.
   The TP10 signal should vary with the front panel intensity
   adjustment, and be approximately 55 Vp-p maximum. The signal
   will be composed of both blanking pulses and varying intensity
   levels for the lines being drawn.

   • If a proper signal is not present at A17TP10, check A17Q1, Q2,
     CR1, and CR2.

   • If the TP10 signal does not vary with the front panel intensity
     adjustment, check the signals at A17TP4 and A17TP1. Both
     signals should vary with the front panel intensity adjustment.
     The TP4 signal should be up to 4 Vp-p, and the TP1 signal should
     be up to approximately 12 Vp-p.

WARNING **The A17 CRT Driver contains lethal voltages with lethal
currents. Use extreme care when servicing this assembly.
Always disconnect the power cord from the instrument before
servicing this assembly. Failure to follow this precaution can
present a shock hazard which may result in personal injury.**

NOTE The following measurements should be made with a high-voltage probe,
such as the 34111A. When using the high-voltage probe, connect the
ground lead securely to the 8562E chassis.

7. Carefully measure the grid voltage at A17J7 pin 6, and the cathode voltage at A17J7 pin 4. The display will work with a cathode voltage of −2450 V ±250 V, provided the grid voltage (A17J7 pin 6) is 30 to 100 V more negative than the cathode. A17R11, CUTOFF, should be able to adjust the voltage difference over a 60 V range to account for tube variations, and achieve proper intensity.

8. If the grid and cathode voltages are correct, turn off the 8562E spectrum analyzer and check A17CR10 with an ohmmeter. If A17CR10 is good, suspect the A18V1 CRT.

9. If the grid and cathode voltages are too low, turn off the power and disconnect W8 from the base of A18V1 CRT, and recheck the grid and cathode voltages.

10. If the grid and cathode voltages are still too low, refer to "CRT Supply Dropping Out (8562E)" on page 658 in this chapter and "1. High Voltage Power Supply Adjustment (8562E)" on page 60.

11. If voltages are correct when the tube is disconnected, the CRT is probably defective.

CAUTION	The pins on the A18V1 CRT bend easily. Be careful not to bend pins when connecting W8 to A18V1.

Power Supply

The power supply section contains the A6 power supply and, in 8562E instruments, the A6A1 HV module. Figure 13-4 on page 637 illustrates the power supply block diagram. Table 13-3 on page 651 lists signal versus pin numbers for power cable W1.

WARNING

The A6 power supply in 8562E and 8562EC instruments, and the A6A1 high voltage assembly in 8562E instruments, contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before servicing these assemblies. Failure to follow this precaution can represent a shock hazard which may result in personal injury.

The voltage potential at A6A1W3, in 8562E instruments, is +9 kV. If the cable must be disconnected, always disconnect it at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument. See procedure 2 in Chapter 3.

Do not discharge the CRT second anode directly to ground, with the A6A1 high voltage cable connected. This can damage the A17 CRT driver assembly. Always discharge through a high resistance, such as a high voltage probe.

Always use an isolation transformer when troubleshooting either the A6 power supply or the A6A1 HV module. When using an isolation transformer, connect a jumper between A6TP101 and A6TP301. This connects the circuit common to earth ground. Remove this jumper when the isolation transformer is not used.

Figure 13-7   Simplified Power Supply Block Diagram
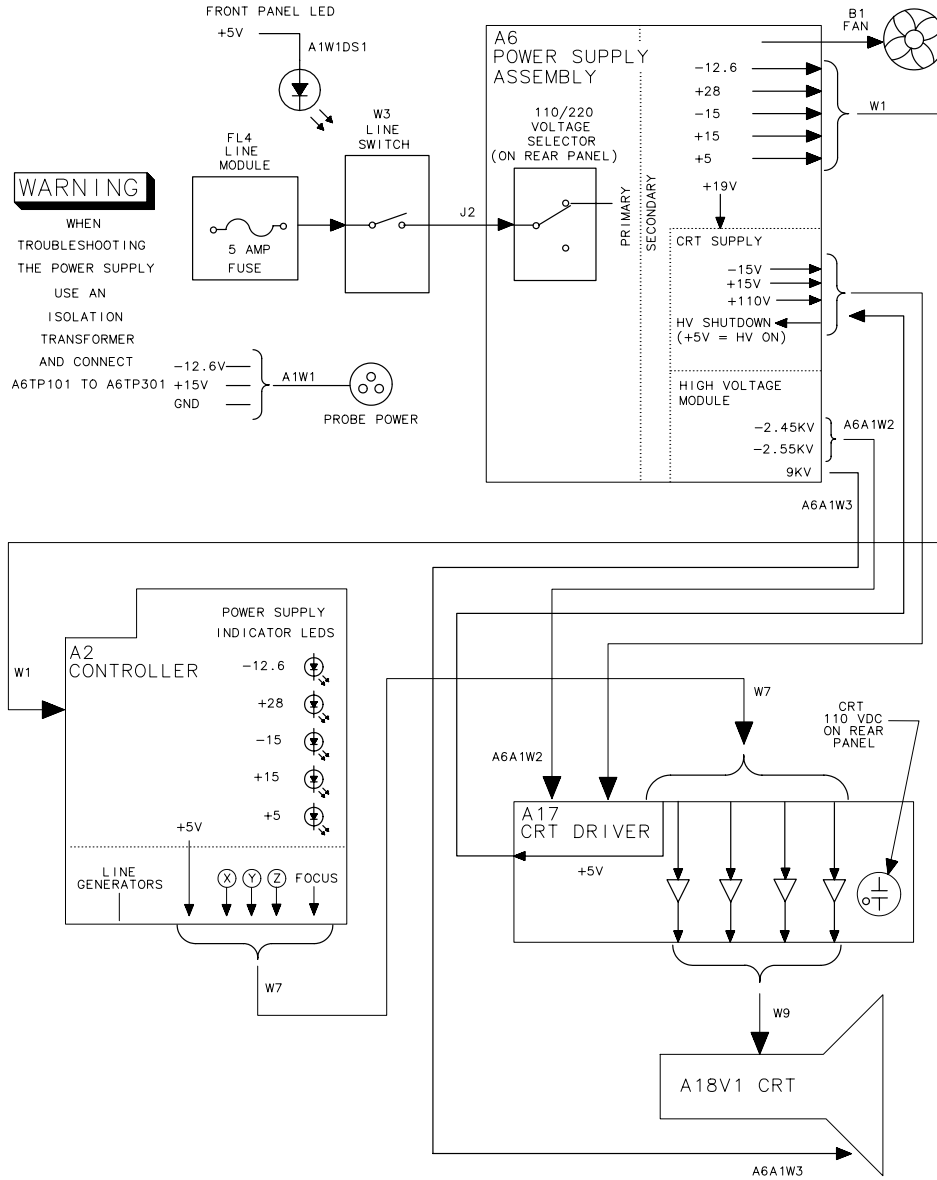
sp141e

The block diagram in Figure 13-7 on page 650 shows the power supply in an 8562E instrument. The power supply in 8562EC instruments is identical except that the CRT and high voltage supplies in an 8562EC are inactive, and are not connected to CRT circuitry.

Table 13-3 **W1 Power-Cable Connections**

Signal	A2J1 (pins)	A3J1 (pins)	A4J1 (pins)	A5J1 (pins)	A6J1- (pins)	A14J1 (pins)	A15J1 (pins)
NC	-	-	-	-	-	-	-
NC	-	-	-	-	-	-	-
A GND	-	3	3	48	3*	3	3
NC	-	-	-	-	-	-	-
NC	-	-	-	-	-	-	-
A GND	-	6	6	45	6*	6	6
NC	-	-	-	-	-	-	-
NC	-	-	-	-	-	-	-
A GND	-	9	9	42	9*	9	9
SCAN RAMP	41	10	-	-	-	10*	-
NC	-	-	-	-	-	-	-
A GND	-	12	12	39	12*	12	12
−12.6 V	38	13	-	-	13*	-	-
−15 V	-	14	14	37	14*	14	14
A GND	-	15	15	36	15*	15	15
−15 V	-	16	16	35	16*	16	16
+15 V	-	17	17	34	17*	17	17
A GND	-	18	18	33	18*	18	18
+15 V	-	19	19	32	19*	19	19
+28 V	-	20	-	-	20*	20	20
+28 V	-	21	-	-	21*	21	21
PWR UP	29	-	-	-	22*	-	-
−15 V	-	23	23	28	23*	23	23
−15 V	-	24	24	27	24*	24	24
+15 V	-	25	25	26	25*	25	25
+15 V	-	26	26	25	26*	26	26
+5 V	-	27	27	24	27*	27	27
+5 V	-	28	28	23	28*	28	28
+5 V	-	29	29	22	29*	29	29
+5 V	-	30	30	21	30*	30	30
D GND	20	31	31	20	31*	-	31
D GND	19	32	32	19	32*	-	32
A GND	18	33	33	18	33*	33	33
A GND	17	34	34	17	34*	34	34
D GND	16	35	35	16	35*	35	35
D GND	15	36	36	15	36*	36	36
D GND	14	37	37	14	37*	37	37
D GND	13	38	38	13	38*	38	38
+5 V	12	39	-	-	39*	-	-
+5 V	11	40	-	-	40*	-	-
+5 V	10	41	-	-	41*	-	-
+5 V	9	42	-	-	42*	-	-
+5 V	8	43	-	-	43*	-	-
+5 V	7	44	-	-	44*	-	-
+28 V	6	45	-	-	45*	-	-
LINE TRIGGER	-	46	-	-	46*	-	-
* Indicates signal source.							

Table 13-3   W1 Power-Cable Connections

Signal	A2J1 (pins)	A3J1 (pins)	A4J1 (pins)	A5J1 (pins)	A6J1- (pins)	A14J1 (pins)	A15J1 (pins)
+15 V	4	47	-	-	47*	-	-
+15 V	3	48	-	-	48*	-	-
−15 V	2	49	49	-	49*	-	-
−15 V	1	50	50	-	50*	-	-
* Indicates signal source.							

Troubleshooting Using the TAM (8562E only)

When using automatic fault isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 13-1 on page 638 to locate the manual procedure.

Table 13-4   Automatic Fault Isolation References

Suspected Circuit Indicated by Automatic Fault Isolation	Manual Procedure to Perform
Check A2 Controller	Blanking Signal
Check All Power Supply Outputs	Dead Power Supply *(steps 1-5)*
Check Buck Regulator	Dead Power Supply *(steps 13-23)*
Check Buck Regulator Control Circuitry	Dead Power Supply *(steps 11-21)*
Check High-Voltage Supplies	High Voltage Supplies
Check Input Rectifier	Dead Power Supply *(steps 6-7)*
Check Intensity Adjustments	Intensity Problems *(steps 1-4)*
Check Kick Start/Bias Circuitry	Dead Power Supply *(steps 8-10)*
Check Low-Voltage Supplies	Low Voltage Supplies

A6 Power Supply Assembly

8562E and 8562EC spectrum analyzers uses a switching power supply operating at 40 kHz to supply the low voltages for most of the analyzer hardware. In the 8562E, the power supply also provides a 30 kHz switching supply (CRT supply) for the high voltages used by the CRT display used in E-series instruments. The CRT supply will be treated as a separate supply since the remainder of A6 must be operating for the CRT supply to operate.

Kick starting occurs when there is a fault either on the power supply or on one of the other assemblies. The power supply will try to start by generating a 200 ms pulse ("kick") every 1.5 seconds. A kick-starting power supply often appears to be dead, but the fan will make one or two revolutions and stop every 1.5 seconds.

Dead Power Supply

1. Use an isolation transformer and connect a jumper between A6TP101 and A6TP301.

2. Connect the negative lead of a DVM to A6TP301.

3. Check TP308 for +5 V.

4. Check TP302 for +15 V.

5. Check TP303 for −15 V.

6. Check TP304 for +28 V.

7. Check TP305 for −12.6 V.

8. Measure the voltage at TP108 to verify the output of the input rectifier. The voltage should be between +215 Vdc and +350 Vdc.

9. If it is not within this range, check the rear panel fuse, input rectifier, input filter, and the rear panel line voltage selector switch.

10. Measure the voltage at TP206 to verify the output of the kick-start/bias-circuitry. The voltage should be approximately +14 Vdc. Test point 206 is on pin 1 of U203.

11. If there is no voltage at TP206, check TP210 for pulses 200 ms wide with an amplitude of 14.7 V. If there are no pulses present, the kick-start circuitry is probably defective. If the pulses are low in amplitude (about 1 V), Q201 is probably shorted.

12. If there are pulses at TP206, or there are pulses at TP210, but not at TP206, the buck regulator control circuitry is probably faulty.

13. Disconnect the power cord from the 8562E spectrum analyzer.

14. Connect the positive output of a current-limited dc power supply to the cathode of A6CR201 (TP206) and the ground to A6TP201.

15. Set the current limit of the power supply to about 500 mA and the voltage to 12 Vdc.

16. Make sure a jumper is connected from A6TP101 to A6TP301. This independently powers the buck regulator control circuitry.

17. Connect a jumper from the output of a +12 Vdc power supply to the end of A6R202 physically nearest A6C211.

18. Connect a jumper from +12 Vdc to the end of C207 nearest C209.

19. If the current draw exceeds approximately 50 mA, suspect a short in the buck regulator control circuitry or a shorted CR201.

20. Check TP204 for an 80 kHz sawtooth (4 Vp-p).

21. Check TP203 and TP207 for 40 kHz square (12 Vp-p). If the waveforms at either TP203 or TP207 are bad, one of the FETs in the DC-DC Converter is probably defective.

22. Check TP105 and TP106 for a 12 Vp-p sawtooth waveform that is flattened at the bottom. If the waveform is a squarewave, the FET to which the test point is connected has failed or shorted.

23. Check TP202 for 80 kHz pulses (12 Vp-p).

24. Short TP401 to TP102. Check TP103 for a waveform similar to that in .

25. If the waveform at TP202 is correct but the waveform at TP103 is bad, suspect either Q102 or CR106.

Figure 13-8   **Buck Regulator Waveform**
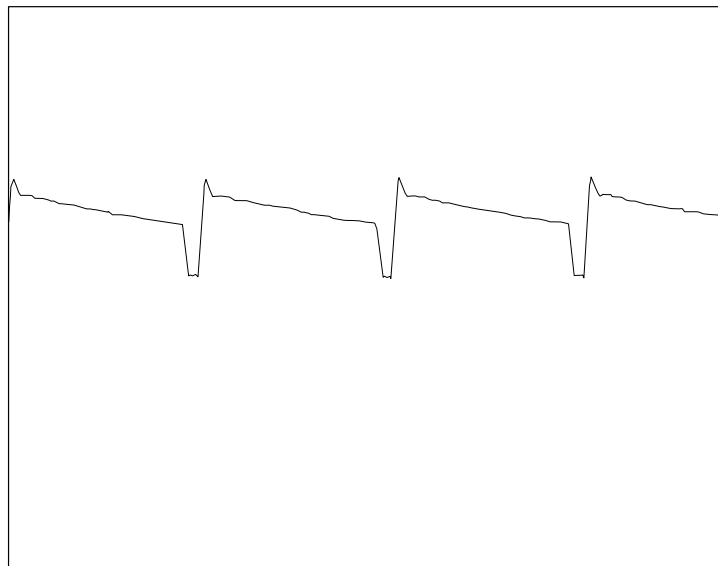
s k 1

Line Fuse Blowing

1. If the line fuse blows with the LINE switch in the off position, suspect either the input filter or the power switch cable assembly.

2. If the line fuse blows when the 8562E/EC spectrum analyzer is turned on, disconnect the power cord and lift the drain of A6Q102 from TP108. If the line fuse still blows, suspect CR102 through CR105.

3. If the fuse is not burned out, check A6TP108 for a voltage of between +215 V and +350 V.

4. If the voltage at TP108 is correct, disconnect the power cord. Wait 60 seconds for the high voltage to discharge. Remove and check A6Q102.

5. If Q102 is shorted, Q103, Q104, CR106, and CR108 are also probably shorted. If Q102 is working properly, measure the resistance between TP102 and TP101 (positive ohmmeter lead to TP102).

6. If the resistance is less than 1 kΩ, suspect either Q103 or Q104 in the DC-DC Converter.

Supply Restarting Every 1.5 Seconds (Kick Start)

See function blocks G, H and L of A6 power supply schematic diagram in the component-level information binder.

If there is a short on the power supply or on one of the other assemblies, the power supply will attempt to "kick start." (Every 1.5 seconds the supply will attempt to start, but will be shut down by a fault condition.) The kick start and bias circuits provide power for the control circuitry during power-up. The kick start circuitry is an RC oscillator which emits a 200 ms pulse every 1.5 seconds. These pulses switch current from the Input Rectifier through Q201 to charge C201. When the power supply is up, a winding on T103 provides power to the control circuitry. This voltage is high enough to keep Q201 turned off.

1. Monitor the waveforms at TP206 and TP208 simultaneously on an oscilloscope.

2. If the signal at TP208 goes high before the signal at TP206 goes low, an overcurrent condition has been detected. Suspect a short in the secondary (output rectifier, voltage regulators, or another assembly).

Low Voltage Supplies

1. Connect the negative lead of a DVM to A6TP301.

2. Check A6TP302 for +15 Vdc.

3. Check A6TP303 for −15 Vdc.

4. Check A6TP304 for +28 Vdc.

5. Check A6TP305 for −12.6 Vdc.

6. Check A6TP308 for +5 Vdc.

7. If the voltages measured above are correct but the power supply LEDs on the A2 controller assembly are not lit, check W1.

8. If the voltages are low, disconnect W1 from A6J1 and measure the test point voltages again. Unless a dummy load is connected to the A6 power supply, the voltages should return to their nominal voltages but be unregulated.

9. If the voltages do not return to near their nominal range, the A6 power supply is probably at fault.

10. If the +5 V supply is low, suspect the +5 V regulator or the feedback circuit. To check the feedback circuit, measure the voltage of the +5 V reference (U305 pin 6) and the ±5 V references to the voltage regulators (U306B pin 7 and U306D pin 14).

11. Check output of U306A pin 1. If the feedback circuit is working properly, the output of U306A should be near +13 Vdc.

12. Check output of U302; its output should be high if the feedback circuit is working properly.

High Voltage Supplies (8562E)

1. Press LINE to turn spectrum analyzer off, disconnect the power cord, and remove the power supply shield.

2. Connect the negative lead of a DVM to A6TP401 and positive lead to A6TP405.

3. Press **LINE** to turn spectrum analyzer on.

4. If the voltage displayed on the DVM is approximately +110 Vdc and the rear panel CRT +110 VDC ON indicator is lit, the A6A1 HV module is probably at fault.

NOTE | Ideally, the DVM should read the voltage written on the label of the A6A1 HV module. If necessary, perform "1. High Voltage Power Supply Adjustment (8562E)" on page 60.

5. If the DVM does not read approximately +110 Vdc, measure the voltage on A6U401 pin 10. This is the HV_SHUT_DOWN signal and should be near +5 Vdc.

6. If HV_SHUT_DOWN is low, suspect a bad connection along W8 between the A6 power supply and the 17 CRT driver.

7. If HV_SHUT_DOWN is correct, connect an oscilloscope to A6TP402. Connect the scope probe negative lead to TP401. Set the oscilloscope to the following settings:

> Sweep time .... 10 μs/div
> Vertical scale .... 10 V/div

8. A nearly-sinusoidal waveform, greater than 30 Vp-p, with an approximately +18 Vdc offset, should be observed.

9. If the waveform is a dc voltage near 0 Vdc with narrow, positive- and negative-going pulses, the A6A1 HV module is faulty. If the waveform is a dc voltage near +18 Vdc with narrow, positive- and negative-going pulses, connect the probe to TP403.

10. If the waveform at TP403 is a sawtooth waveform with a 1.8 V amplitude, the A6A1 HV module is faulty.

If the TP403 waveform has pulses similar to those on TP402, the A6 power supply is probably faulty.

CRT Supply Dropping Out (8562E)

See function block K of A6 power supply schematic diagram in the component-level information binder.

The CRT supply is a separate switching supply which provides the +110 Vdc for the A17 CRT driver from a winding on the A6A1 HV module. The CRT supply operates at approximately 30 kHz. The exact frequency is determined by the inductance of the primary winding of A6A1T1 and A6C407. The supply will only operate if the HV_SHUT_DOWN line is high.

If the power supply keeps dropping out, there is probably a short on the A17 CRT driver assembly.

1. Disconnect W8 from A6J4.

2. Connect an IC clip to U401 and connect a jumper between U401 pin 10 and TP308 (+5 Vdc).

3. Connect voltmeter to TP405 and press **LINE** to turn the analyzer on.

4. Check TP405 for a voltage of approximately +110 Vdc. It will probably measure higher since there is no load on the supply.

5. If the voltage at TP405 is correct, suspect a short on A17. If the voltage at TP405 is not correct, check U401 pin 8 for a sawtooth signal. The sawtooth should be flat-topped and about 5 Vp-p at a frequency of about 30 kHz.

6. If the sawtooth is not flat-topped, suspect U402A and its associated circuitry.

7. If the sawtooth is correct, check the base of Q401 for 30 kHz pulses.

8. If the duty cycle is high, but there is no +110 Vdc, suspect the bridge rectifier, CR401 through CR404.

Blanking Signal (8562E)

1. Connect an oscilloscope probe to A2J202 pin 3. Connect the oscilloscope ground lead to TP3. Set the oscilloscope to the following settings:

   Sweep time .... 2 ms/div
   Vertical scale .... 1 V/div

2. If a 4 Vp-p signal is not seen, the A2 controller assembly is faulty.

3. Repeat steps 1 and 2 with the oscilloscope probe on A2J202 pin 14.

4. Set the oscilloscope to the following settings:

   Sweep time .... 1 µs/div
   Vertical scale .... 2 V/div

5. Connect the positive probe lead to A2J202 pin 15. This is the blanking output.

6. TTL-level pulses should be observed. If the signal is either always high or always low, the display will be blanked; suspect the A2 controller assembly.

7. If the signals on A2J202 pins 3, 14, and 15 are correct, troubleshoot the A17 CRT driver.

Buck Regulator Control

See function block H of the A6 power supply schematic diagram in the component-level information binder.

The buck regulator control pulse-width modulates the buck regulator and provides a synchronized signal to the DC-DC converter control circuitry. The buck regulator control has two feedback paths. The first is the output of the buck regulator, which provides coarse regulation. The second is the feedback circuit which samples and compares the +5 Vdc output of the output rectifier.

U202B and associated circuitry senses the output of the input rectifier and will turn off U203 if the voltage at TP108 is less than approximately +170 Vdc. Also, it will not allow U203 to start up until this voltage exceeds +215 Vdc. A low on the output of U202B will also clear the overcurrent latch in the DC-DC converter control circuitry.

Thermal shutdown occurs when RT201, mounted on the main heatsink, reaches a temperature of 100 C. When this occurs, the voltage at U203 pin 13 exceeds 0.6 V and inhibits pulses to the buck regulator.

R203, R204, U211, and associated circuitry provide feedforward for U203. This makes the loop gain independent of input line voltage and cancels 120 Hz ripple by more than 10 dB.

U202C and its associated circuitry permit the power supply to start up at low line voltages at low temperatures. At low line voltages U202C will draw charge away from C206 through R205. This allows the buck regulator to turn on and draw current through the thermistors in the input rectifier. This warms up the thermistors, thereby decreasing their resistance and increasing the voltage at TP108. When the voltage is sufficiently high at TP108, the output of U202C will open and C206 will be allowed to charge normally.

U202A converts the sawtooth at TP204 to a squarewave to drive the DC-DC Converter Control circuitry. The frequency of the sawtooth is determined by the resistance at pin 7 of U203 and the capacitance at pin 8 of U203.

DC-DC Converter Control

See function block I of A6 power supply schematic diagram in the component-level information binder.

The DC-DC converter control circuitry divides the 80 kHz squarewave from U202A and generates two complementary 40 kHz squarewaves to drive the FETs in the DC-DC converter. Also, U202D and its associated circuitry monitor the voltage across sense resistor R116 in the DC-DC converter. When the current through the FETs in the DC-DC converter exceeds 1.8 A, the voltage across R116 will cause the output of U202D to go high. This sets a latch in U204 which turns off U203.

Power Up

See function block M of the A6 power supply schematic diagram in the component-level information binder.

The power up circuitry generates the PWR UP signal, which tells the microprocessor that the supplies are up and stable. PWR UP will go high when the +5 Vdc supply exceeds +4.99 Vdc. PWR UP will go low when this voltage is less than +4.895 Vdc. Once PWR UP is set low, it will stay low for at least 50 ms before going high, even if the +5 Vdc supply exceeds +4.99 Vdc before 50 ms have elapsed.

A17 CRT DISPLAY DRIVER BLOCK DIAGRAM

FIGURE 13-9. A17 CRT DRIVER BLOCK DIAGRAM

POWER SUPPLY ASSEMBLY
BLOCK DIAGRAM

W3
LINE

98
928
91
8
0

A6 POWER SUPPLY BOARD
ASSEMBLY

LINE
CORD

FL4
LINE MODULE

J101-2

J101-1

918

98

A INPUT FILTER

B INPUT
RECTIFIER

TP101

TP108

E P/O A6A2

U101

TP309

LINE
TRIGGER

C BUCK
REGULATOR

TP102
TP103

TP210

G KICK
START/BIAS

TP202
TP204
TP205

L BUCK
REGULATOR
CONTROL

TP206
TP208

TP211

D DC-DC
CONVERTER

TP105
TP106

T103

CURRENT
SENSE

TP209

2

TP203
TP207

I DC-DC
CONVERTER
CONTROL

OVER CURRENT

2

E OUTPUT
RECTIFIERS,
FILTERS,
DOUBLERS

+34V
+17V
-17V
+6.8V
-6.8V

J FEEDBACK
CIRCUIT
(P/O A6A2)

U206

+34V

F VOLTAGE
REGULATORS
(P/O A6A2)

LINE TRIGGER

M VTF SUPPLY

YTF_SENSE

TP403

TP401
GND

+28V MODULATED

K CRT SUPPLY
(Not used in
EC_ Series)

TP402

+17V

DRIVE

GND

+110V

TP404

TP405

TP304
TP308
TP302 TP306 TP305 TP303 TP301

+5V
+28V
+15V
+13V
-12.6V
-15V
GND
-5V

TP307

D POWER UP
(P/O A6A2)

TP37

POWER UP

50

J1

J3-2

J3-1

J4-3

J4-4
J4-5

J4-6

POWER CABLE W1

2 TO B1 (FAN)

5 W8 TO A17 CRT DRIVER
(E-SERIES ONLY)

WARNING
HAZARDOUS
VOLTAGE

HV SHUTDOWN

A6A1W1

J5-4

J5-5

J5-1

J5-2

J5-3

(E-SERIES ONLY)
A6A1 HIGH VOLTAGE
ASSEMBLY

+110V AC

+110V AC

A6A1W3

A6A1W2

6

0

7

9kV POST
ACCELERATOR TO
A18V1

-2.45kV TO A17J6-3

-2.45kV TO A17J6-5

-2.55kV TO A17J6-1

WARNING

CIRCUIT COMMON NOT EARTH GROUND
NODES MAY BE AT A LETHAL POTENTIAL
WITH RESPECT TO EARTH GROUND.
CIRCUIT ≠ EARTH

LINE TO OUTPUT SAFETY
ISOLATION PROVIDED BY
T103, U101, U206

J2-2
J2-4
J2-3
J2-5

s1122c

FIGURE 13-10 A6 POWER SUPPLY BLOCK DIAGRAM

14 Component-Level Information Packets

Introduction

Component-Level Information Packets (CLIPs) contain a parts list, a component-location diagram, and schematic diagrams for selected instrument assemblies. A new CLIP with a new part number is issued whenever an assembly is changed.

Updated or replacement CLIPs may be ordered through your local Agilent Technologies Sales or Service Office. Use the CLIP part numbers provided in Table 14-1 on page 667.

A single volume CLIP set that contains all repairable assemblies for the 8560 E-series and EC-series is also available. Order this CLIP set by using part number 5967-8582.

With the exception of the A2 controller board, the A1A1 keyboard, and the A17 display driver board, the E-series assemblies for which CLIPs have been generated are identical to the same assemblies in EC-series instruments.

Each of the CLIPs in the CLIP set can also be ordered individually.

NOTE   CLIPs may be unavailable for recently introduced assemblies.

Table 14-1 **CLIPs Available for 8562E and 8562EC Spectrum Analyzers**

Board Assembly	Instrument Serial Prefix	Assembly Part Number	CLIP Part Number
A1A1 Keyboard (E-series)	3611A and above	08562-60140	08562-90188*
A1A1 Keyboard (EC-series only)	New Assembly	08563-60162	08563-90222*
A2 Controller Assembly (EC-series only)	New Assembly	08563-90160	08563-90224*
A2 Controller Assembly (E-series only)	3411A through 3741A 3743A and above	08564-60010† 08564-90025	08563-90003 08564-90028*
A3 Interface Assembly (E- and EC-series)	3611A and above	08563-60098	08563-90017*
A4 Log Amplifier/Cal Osc	3611A through 3724A 3728A and above	08563-60076† 08563-60103	08563-90119 08563-90166*
A5 IF Filter	3611A to 3724A00414 3724A00415 and above	08563-60023 08563-60123	08563-90058 08563-90186*
A6 Power Supply	3406A through 3751A 3804A through 3821A 3846A and above	08564-60008† 08564-60028 08564-60031	08564-90004 08564-90032 08564-90039*
A6A2 Power Supply Regulator Board	3818A and above	08564-60030	08564-90034*
A14 Frequency Control	3611A through 3818A 3821A and above	08563-60090† 08563-60135	08560-90152 08563-90202*
A15 RF Board (Option 103) (with SIG ID)	3611A through 3632A 3635A through 3818A 3821A and above	08563-60085† 08563-60092 08563-60133	08563-90128 08563-90163 08563-90200*

† Denotes refurbished board assemblies available. Refurbished board assembly part numbers have 9 as the second digit of the suffix. For example, 08563-69032 is the refurbished part number for board assembly 08563-60032.

‡ Same as for A15 Option 103 with SIG ID. * Denotes current version of assembly.

Table 14-1   **CLIPs Available for 8562E and 8562EC Spectrum Analyzers**

Board Assembly	Instrument Serial Prefix	Assembly Part Number	CLIP Part Number
A15 RF Board (Option 103) (without SIG ID)	3611A through 3632A 3635A through 3818A 3821A and above	08563-60085[†‡] 08563-60092[†‡] 08563-60133	08563-90128 08563-90163 08563-90200*
A15 RF Board (Standard) (with SIG ID)	3611A through 3632A 3635A through 3818A 3821A and above	08563-60086[†] 08563-60093 08563-60134	08563-90129 08563-90164 08563-90201*
A15 RF Board (Standard)	3551A through 3632A 3635A through 3818A 3821A and above	08563-60132 08563-60091[†] 08563-60132	08563-90127 08563-90162 08563-90199*
A16 Fast ADC (Option 007 in E-series instruments only)	3611A and above	08563-60030	08563-90076*
A17 LCD Driver (EC-series)	New Assembly	08563-60161	08563-90221*
A17 CRT Driver (E-series)	3611A through 3738A 3741A and above	08563-60077[†] 08563-60122	08563-90113 08563-90182*
A19 GPIB	3611A and above	08562-60042	08562-90115*

[†] Denotes refurbished board assemblies available. Refurbished board assembly part numbers have 9 as the second digit of the suffix. For example, 08563-69032 is the refurbished part number for board assembly 08563-60032.

* Denotes the current version of assembly.

[‡] Same as for A15 Option 103 with SIG ID.
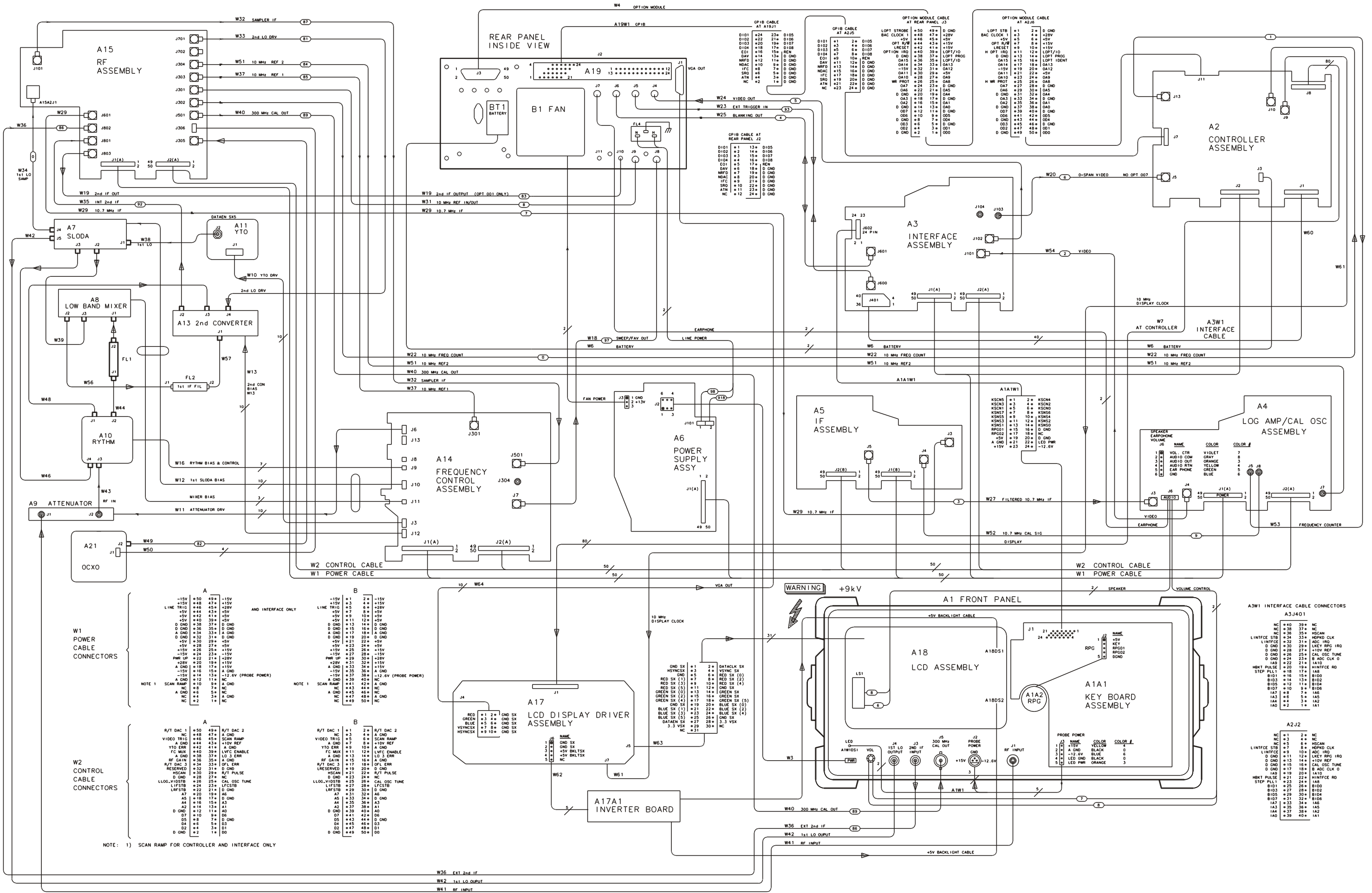
BLOCK DIAGRAM
8562E
INTERCONNECT
W/ OPT 007

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